A two-dimensional analytical-model-based comparative threshold performance analysis of SOI-SON MOSFETs

Sanjoy Deb[1], Saptarsi Ghosh[1], N Basanta Singh[2], A K De[3], and Subir Kumar Sarkar[1, †]

[1]Department of Electronics & Telecommunication Engineering, Jadavpur University, Kolkata-700032, India
[2]Department of Electronics & Communication Engineering, Manipur Institute of Technology, Imphal-795004, India
[3]Department of Electronics & Communication Engineering, National Institute of Technology, Durgapur-713209, India

Abstract: A generalized threshold voltage model based on two-dimensional Poisson analysis has been developed for SOI/SON MOSFETs. Different short channel field effects, such as fringing fields, junction-induced lateral fields and substrate fields, are carefully investigated, and the related drain-induced barrier-lowering effects are incorporated in the analytical threshold voltage model. Through analytical model-based simulation, the threshold voltage roll-off and subthreshold slope for both structures are compared for different operational and structural parameter variations. Results of analytical simulation are compared with the results of the ATLAS 2D physics-based simulator for verification of the analytical model. The performance of an SON MOSFET is found to be significantly different from a conventional SOI MOSFET. The short channel effects are found to be reduced in an SON, thereby resulting in a lower threshold voltage roll-off and a smaller subthreshold slope. This type of analysis is quite useful to figure out the performance improvement of SON over SOI structures for next generation short channel MOS devices.

Key words: silicon-on-insulator; silicon-on-nothing; Poisson's equation; short channel effects; threshold voltage roll-off; subthreshold slope

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1. Introduction

With the emergence of mobile computing and communication, low power device design and implementation have a significant role to play in VLSI circuit design[1]. Continuous device performance improvements are possible only through a combination of device scaling, new device structures and material property improvement[1]. Conventional silicon (bulk CMOS) technology has suffered from fundamental physical limitations in the sub-micron or nanometer region, which has led to alternative device technologies such as silicon-on-insulator (SOI) technology[2]. Short-channel-effects (SCEs) reduction, transistor scalability and circuit performance are improved by using SOI technology, especially ultrathin, fully depleted (FD) SOI MOSFETs[3]. SOI MOSFETs enable high speed applications because of their low parasitic capacitance[4]. The development of SOI MOSFET technology has been limited so far by the difficulty in controlling the silicon film thickness, adjusting the buried oxide layer thickness, shallow source drain series resistances and fringing fields[5−7]. Although different SCEs are highly suppressed in an SOI structure, it is not fully immune to some SCEs[8]. Among the different forms of SCE-related device performance degradation, higher threshold voltage roll-off and subthreshold slope are very important issues[9]. In an effort to overcome these drawbacks, improved SOI structures have been suggested in recent times[10]. Silicon-on-nothing (SON), an innovative SOI structure proposed and developed very recently, enables fabrication of extremely thin silicon (5 to 20 nm) and buried dielectric (10 to 30 nm) super SOI devices, which are capable of quasi-total suppression of SCEs and have excellent electrical performances[11]. In an SON MOSFET, the buried layer of an SOI MOSFET is replaced with an air layer. Among the advantages of fully depleted (FD) SON architecture over FDSOI structures the most significant one is the reduced electrostatic coupling of the channel with the source/drain and the substrate through the buried layer (BL)[12]. Reduced electrostatic coupling through the BL allows for the reduction of the transistor minimal channel length or a relaxation of the requirements regarding Si film thickness[13]. Moreover, since the so-called "nothing" (or air) layer embedded below the Si active film has a lower dielectric permittivity than an oxide, the parasitic capacitances between the source/drain and the substrate are reduced and therefore a higher circuit speed can be expected with SON devices[14]. The thick buried layer can be a drawback of SOI MOSFETs due to a large positive charge accumulating in the thick BL. However, in SON MOSFETs no charge will accumulate in the air gap[15].

To develop a generalized SOI/SON MOSFET analytical model, accurate modeling of different SCEs like drain induced barrier lowering (DIBL) or 2D charge sharing (2DCS) are essential, as these effects need to be incorporated in the analytical model. Also the effects are different for the two structures. Using a 2D Poisson's equation solution, some threshold voltage models of SOI MOSFETs have been proposed[16−20]. The theoretical approach[21] adopted can be extended to develop a generalized threshold voltage model of an SOI/SON MOSFET that incorporates different SCEs, such as DIBL and 2DCS, for comparison of their performances. To incorporate SCE modification in an SON structure, fringing field and substrate bias effects should be carefully modeled as these are the main rea-

† Corresponding author. Email: su_sircir@yahoo.co.in
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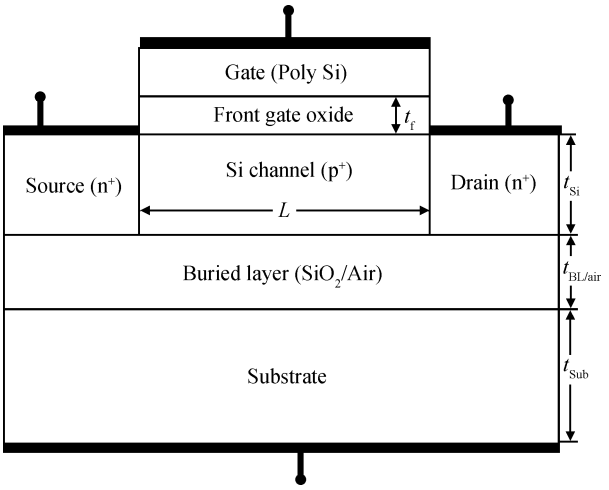

Fig. 1. Generalized SOI/SON MOSFET layered structure.

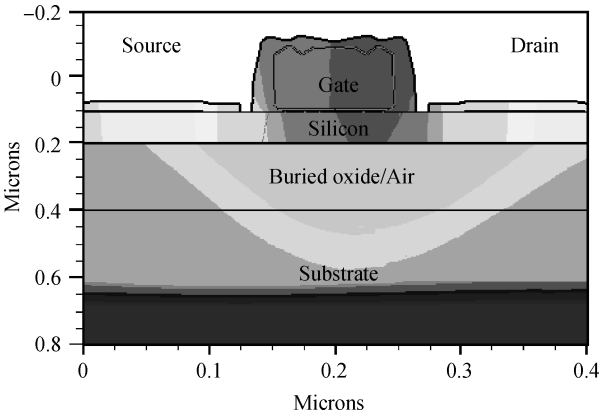

Fig. 2. Generalized SOI/SON MOSFET structure simulated with ATLAS.

sons for SCE modification.

In this work, a generalized 2D analytical threshold voltage model based on the Poisson's equation solution has been developed for a uniformly doped SOI/SON MOSFET. The effects of the fringing field, substrate bias and junction induced 2D field effects are incorporated in the model. The performance of the two devices is investigated and compared in terms of threshold voltage roll-off and subthreshold slope under different operational and structural parameter variations. The results of the analytical simulation are compared with the results from an ATLAS 2D physics based simulator and they are found to be in good agreement, thereby establishing the validity of our analytical model.

2. Analytical modeling

In a short-channel device, potential profiles in and beneath the channel (in the BL) are two-dimensional in nature[22]. Threshold voltage can be calculated by solving the 2-D Poisson's equation in the channel[22–24]. A generalized layered structure of an SOI/SON MOSFET for analytical model formulation is shown in Fig. 1 and the corresponding SILVACO simulated structure is shown in Fig. 2. Let t_f, t_{Si}, $t_{BL/air}$, t_{sub} and L be the thicknesses of gate oxide, silicon channel layer, buried layer/air layer, substrate layer and metallurgical channel length of the device, respectively.

The 2-D Poisson's equation in the two-dimensional channel region of the depleted silicon film body ($0 \leqslant x \leqslant L$, $0 \leqslant y \leqslant t_{Si}$) can be written as[23]

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}}, \tag{1}$$

where $\phi(x, y)$ is the 2-D potential profile in the silicon channel, N_A is the doping concentration of the p-type channel and the substrate and ε_{Si} is the permittivity of silicon. By considering a second-order potential approximation, the 2D potential profile in the channel is written as[16]

$$\phi(x,y) = A_1(x) + A_2(x)y + A_3(x)y^2. \tag{2}$$

At the front and back channel interfaces, uniform electric fields are considered and the surface potentials are abbreviated as $\phi_{sf}(x)$ and $\phi_{sb}(x)$, respectively. The four boundary conditions according to the continuity of electrostatic potential and one-dimensional Gauss's law are given as[22–24]

$$\phi(x,y) = \phi_{sf}(x)|_{y=0}, \tag{3}$$

$$\phi(x,y) = \phi_{sb}(x)|_{y=t_{Si}}. \tag{4}$$

At $y = 0$,

$$\frac{\partial\phi(x,y)}{\partial y} = -E_{sf}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{gs} - \phi_{sf}(x)}{t_f}. \tag{5}$$

At $y = t_{Si}$,

$$\frac{\partial\phi(x,y)}{\partial y} = -E_{sb}(x) = -\frac{\varepsilon_{BL/air}}{\varepsilon_{Si}}\frac{V'_{ss} - \phi_{sb}(x)}{t_{BL/air}}, \tag{6}$$

where $\varepsilon_{BL/air}$ is the dielectric permittivity of silicon dioxide/air, V'_{gs} and V'_{ss} are the effective applied front and back channel voltages. The front and back channel voltages are expressed as $V'_{gs} = V_{gs} - V_{ffb}$ and $V'_{ss} = V_{ss} - V_{bfb}$, where V_{ffb} and V_{bfb} are the front and back channel flat band voltages, respectively. The values of the coefficients $A_1(x)$, $A_2(x)$ and $A_3(x)$ derived by solving Eqs. (2) and (3)–(6) are given as

$$A_1(x) = \phi_{sf}(x), \tag{7}$$

$$A_2(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{gs} - \phi_{sf}(x)}{t_f} = -\frac{c_f}{\varepsilon_{Si}}\left[V'_{gs} - \phi_{sf}(x)\right], \tag{8}$$

$$\begin{aligned} A_3(x) = {} & \left[V'_{ss} + V'_{gs}\left(\frac{c_f}{c_{BL/air}} + \frac{c_f}{c_{BL/air}}\right)\right. \\ & \left.-\phi_{sf}(x)\left(1 + \frac{c_f}{c_{BL/air}} + \frac{c_f}{c_{BL/air}}\right)\right] \\ & \times\left[t_{Si}^2\left(1 + 2\frac{c_f}{c_{BL/air}}\right)\right]^{-1}, \end{aligned} \tag{9}$$

where C_f and $C_{BL/air}$ are the front and back oxide/air capacitances, respectively. Substituting the values of the coefficients in Eq. (2), we get a second-order differential equation of $\phi_{sf}(x)$,

$$\frac{t_{Si}^2\left(1+2\frac{C_{Si}}{C_{BL/air}}\right)}{1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}\frac{d^2\phi_{sf}(x)}{dx^2}-\phi_{sf}(x) + \frac{\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}{1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}(V_{gs}-V_{th})+2\phi_F=0. \quad (10)$$

Solving Eq. (10), the long-channel threshold voltage is obtained as

$$V_{th}^{long}=V_{ffb}+\frac{\left(1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}\right)\times 2\phi_F}{\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}} + \frac{qN_At_{Si}\left(1+2\frac{C_{Si}}{C_{BL/air}}\right)}{2C_{Si}\left(\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}\right)}-\frac{V'_{ss}}{\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}, \quad (11)$$

where $2\phi_F=\frac{K_BT}{q}\ln\frac{N_A}{N_i}$ is the Fermi potential in the silicon film. Setting $\left(\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}\right)\left(1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}\right)^{-1}(V_{gs}-V_{th})+2\phi_F=v'$ and $t_{Si}^2\left(1+2\frac{C_{Si}}{C_{BL/air}}\right)\left(1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}\right)^{-1}=\lambda^2$, Equation (10) becomes:

$$\lambda^2\frac{d^2\phi_{sf}(x)}{dx^2}-\phi_{sf}(x)+v'=0, \quad (12)$$

where λ is the characteristic length associated with the surface potential. Introducing a variable, $\zeta(x)=\phi_{sf}(x)-v'$, Equation (12) can be written as

$$\frac{d^2\zeta(x)}{d^2x^2}-\frac{\zeta(x)}{\lambda^2}=0. \quad (13)$$

Equations (5) and (6) are valid in the front oxide with the assumption of a strict vertical field. Since a lateral field (from the source and drain, which is generally known as the fringing field) as well as a vertical field due to substrate bias[22–24] are present, Eqs. (5) and (6) are not valid in the buried oxide layer. Due to the combined effect of the lateral and vertical fields, V_{ss} will be modified and the modified field is denoted by V_{ss}^{eff}. Since the charge in the buried layer is negligible, the 2-D Laplace's equation in the buried layer charge reduces to

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{qN_B}{\varepsilon_{BL/air}}, \quad 0\leqslant x\leqslant L, t_{Si}\leqslant y\leqslant t_{Si}+t_{ox2}. \quad (14)$$

The relevant boundary conditions are given below:

$$\phi(0,t_{Si})=V_{bi},$$

$$\phi(L,t_{Si})=V_{bi}+V_{ds},$$

$$\phi(x,t_{Si})=\phi_{sb}(x),$$

$$\phi(x,t_{Si}+t_{box})=V_{ss}-V_{bfb},$$

where $V_{bi}=V_T\ln\frac{N_{sd}N_A}{n_i^2}$ is the built in potential. Assuming that the two partial derivatives are weakly coupled, we can write

$$\frac{\partial^2\phi(x,y)}{\partial x^2}\approx-\frac{\partial\phi(x,y)}{\partial y^2}\approx\chi, \quad (15)$$

where χ is an empirical parameter that approaches zero as the channel length increases. By integrating Eq. (15) from $x=0$ to $x=L$, χ can be expressed as

$$\chi=\frac{2}{L^2}\{\phi(L,y)-\phi(0,L)-[\frac{d\phi(x,y)}{dx}|_{x=0}]L\} =\frac{2}{L^2}[kV_{ds}+rE_0L]. \quad (16)$$

where r and k are analytical fitting constants depending only upon the thickness of the BL/air layer. From the boundary conditions it is evident that both of them are $\leqslant 1$ and $E_0=-\frac{d\phi(x,y)}{dx}|_{x=0,y=t_{Si}}$ is the source of the fringing field.

Integrating Eq. (15) from $y=t_{Si}$ to $y=t_{Si}+t_{o2}$ and putting in the value of χ, we get:

$$\frac{d\phi(x,y)}{dx}|_{x=0,y=t_{Si}}=\frac{1}{t_{BL/air}}\left[\frac{kV_{ds}+rE_0L}{L^2}t_{BL/air}^2+V_{ss}-V_{bfb}-\phi_{sb}(x)\right]. \quad (17)$$

From Eqs. (6) and (17), we get:

$$V_{ss}^{eff}=V_{ss}+\frac{t_{BL/air}^2}{L^2}(kV_{ds}+rE_0L). \quad (18)$$

Inserting Eqs. (5) and (6) into Eq. (2), we get the desired relationship between $\phi_{sf}(x)$ and $\phi_{sb}(x)$ which is given as

$$\phi_{sb}(x)=\frac{2C_{Si}+C_f}{2C_{Si}+C_{BL/air}}\phi_{sf}(x)-\frac{C_f}{2C_{Si}+C_{BL/air}}V'_{gs}+\frac{C_{BL/air}}{2C_{Si}+C_{BL/air}}V'_{ss}. \quad (19)$$

The expression of E_0 can be written as

$$E_0=-\frac{d\phi_{sb}(x)}{dx}|_{x=0} =-\frac{2C_{Si}+C_f}{2C_{Si}+C_{BL/air}}\frac{d\phi_{sf}(x)}{dx}|_{x=0} =-\frac{2C_{Si}+C_f}{2C_{Si}+C_{BL/air}}\frac{(V_{bi}+V_{ds}-v')-(V_{bi}-v')\cosh\frac{L}{\lambda}}{\lambda\sinh\frac{L}{\lambda}}. \quad (20)$$

Substituting the value of E_0 in Eq. (18), we get:

$$(V_{ss}^{eff})' = V_{ss} + \frac{t_{BL/air}^2}{L^2}\left\{kV_{ds} - rL\left[-\frac{2C_{Si}+C_f}{2C_{Si}+C_{BL/air}} \times \frac{(V_{bi}+V_{ds}-v')-(V_{bi}-v')\cosh(L/\lambda)}{\lambda\sinh(L/\lambda)}\right]\right\}. \quad (21)$$

The effective back gate bias voltage reduces to V_{ss} for long L and/or thin BL thicknesses i.e. $t_{BL/air}$. Consideration of vertical and lateral field penetration through the BL will modify the threshold voltage expression given by Eq. (11) and it can be written as

$$V_{th}^{eff} = V_{ffb} + \frac{1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}{\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}} \times 2\phi_F + \frac{qN_A t_{Si}\left(1+2\frac{C_{Si}}{C_{BL/air}}\right)}{2C_{Si}\left(\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}\right)} - \frac{(V_{ss}^{eff})'}{\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}, \quad (22)$$

and

$$v' = \frac{1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}{\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}(V_{gs}-V_{th}^{eff}) + 2\phi_F. \quad (23)$$

Similarly Equation (13) will be transformed into

$$\frac{d^2\zeta_{eff}(x)}{dx^2} - \frac{\zeta_{eff}(x)}{\lambda^2} = 0. \quad (24)$$

To encounter the lateral field in the channel, Eq. (24) has been solved with the boundary conditions at the source and drain end, which are given as

$$\zeta_{eff}(x)|_{x=0} = V_{bi} - V'_{eff} = V'_1, \quad (25)$$

$$\zeta_{eff}(x)|_{x=L} = V_{bi} + V_{ds} - V'_{eff} = V'_1. \quad (26)$$

The solution of Eq. (24) can be written as

$$\zeta_{eff}(x) = \frac{V'_1\sinh\frac{L-x}{\lambda} + V'_2\sinh\frac{x}{\lambda}}{\sinh\frac{x}{\lambda}}, \quad (27)$$

and

$$\phi_{sf}(x) = \zeta_{eff}(x) + v' = \frac{V'_1\sinh\frac{L-x}{\lambda} + V'_2\sinh\frac{x}{\lambda}}{\sinh\frac{L}{\lambda}} + v'. \quad (28)$$

Using the condition for the minimum surface potential $\frac{d\phi_{sf}(x)}{dx} = 0$[23, 24], the minimum surface potential point is obtained as

$$x = 0.5\left(L - \lambda\lg\frac{\tanh\frac{L}{2\lambda}-M}{\tanh\frac{L}{2\lambda}+M}\right), \quad \text{where } M = \frac{V'_2-V'_1}{V'_2+V'_1}.$$

The corresponding minimum front surface potential is obtained as

$$\phi_{sf}(x_{min}) = \frac{V'_1\sinh\frac{L-x_{min}}{\lambda} + V'_2\sinh\frac{x_{min}}{\lambda}}{\sinh\frac{L}{\lambda}} + v'. \quad (29)$$

The onset of strong inversion occurs when the channel has just enough inversion charges through the application of a specific gate voltage (namely the threshold voltage). This condition happens when the front surface potential is equal to twice the value of the Fermi potential. Putting $\phi_{sf}(x_{min}) = 2\phi_F$ into Eq. (29), the short channel threshold voltage is obtained as

$$V_{th}^{short} = V_{th}^{eff} + \frac{1}{C_{Si}}\left(\frac{2\phi_F}{C_2} - \frac{C_1}{C_3} - 2\phi_F\right), \quad (30)$$

where

$$C_1 = \frac{V_{bi}\left(\sinh\frac{L-x_{min}}{\lambda}+\sinh\frac{x_{min}}{\lambda}\right) + V_{ds}\sinh\frac{x_{min}}{\lambda}}{\sinh\frac{L}{\lambda}},$$

$$C_2 = \frac{\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}{1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}}.$$

and

$$C_3 = 1 - \frac{\sinh\frac{L-x_{min}}{\lambda}+\sinh\frac{x_{min}}{\lambda}}{\sinh\frac{L}{\lambda}},$$

The subthreshold slope, $SS = [2.3V_T\frac{dV_{gs}}{d\phi_{sf}(x_{min})}]^{-1}$, can be expressed as

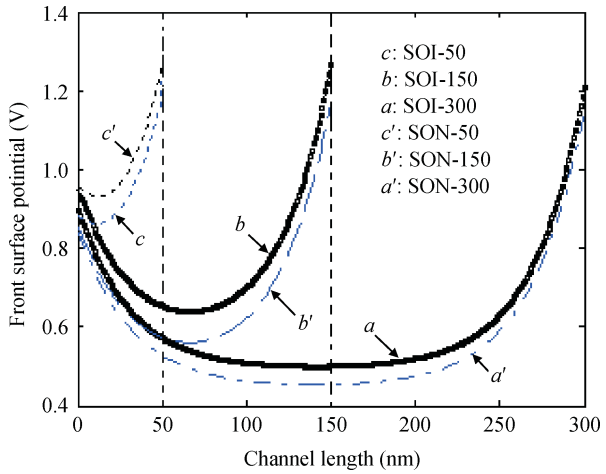

Fig. 3. Variation of the front surface potential along the channel for n-channel SOI/SON MOSFETs with $V_{ds} = 0.5$ V, $t_{gox} = 7$ nm, $t_{Si} = 100$ nm, $t_{BL/air} = 200$ nm, $N_A = 2 \times 10^{17}$ cm^{-3}, $V_{ss} = 1$ V.

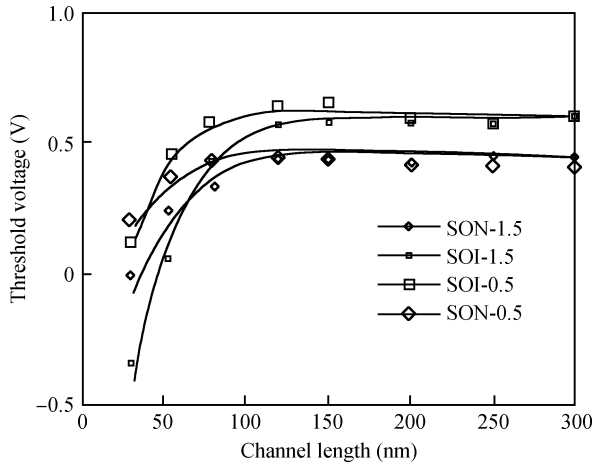

Fig. 4. Variation of threshold voltage with channel length for SOI/SON MOSFETs for $V_{ds} = 0.5$ V and $V_{ds} = 1.5$ V. Other parameters are the same as in Fig. 3 and symbols indicate the ATLAS simulated data.

$$
\begin{aligned}
\mathrm{SS} &= 2.3V_{\mathrm{T}}\frac{\mathrm{d}\phi_{\mathrm{sf}}(x_{\min})}{\mathrm{d}V_{\mathrm{gs}}} \\
&= 2.3V_{\mathrm{T}}\Bigg\{\frac{a_2-1}{a_2-a_1}\exp\sqrt{A_1}x_{\min} - \frac{a_2-a_1-1}{a_2-a_1} \\
&\quad\times\exp\sqrt{A_2}x_{\min} + \Big[K_1\sqrt{A_1}\exp\sqrt{A_1}x_{\min} \\
&\quad - K_2\sqrt{A_2}\exp(-\sqrt{A_2}x_{\min})\Big]\frac{1}{2\sqrt{A_1}}\frac{K_1}{K_2} \\
&\quad\times\frac{K_1\dfrac{a_2-a_1-1}{a_2-a_1} - K_2\dfrac{a_1-1}{a_2-a_1}}{K_1^2}\lg\frac{K_1}{K_2}\Bigg\} \\
&\quad\times\frac{\dfrac{C_{\mathrm{f}}}{C_{\mathrm{BL/air}}}+\dfrac{C_{\mathrm{f}}}{C_{\mathrm{Si}}}}{1+\dfrac{C_{\mathrm{f}}}{C_{\mathrm{BL/air}}}+\dfrac{C_{\mathrm{f}}}{C_{\mathrm{Si}}}},
\end{aligned}
\tag{31}
$$

where

$$A_1 = 1/\lambda^2,\ \ A_2 = \frac{V'_{\mathrm{eff}}}{\lambda^2},$$

$$a_1 = \exp(L\sqrt{A_1}),\ \ a_2 = \exp(-L\sqrt{A_2}),$$

$$K_1 = V_{\mathrm{bi}} + V'_{\mathrm{eff}} - \frac{V_{\mathrm{bi}} + V_{\mathrm{ds}} + V'_{\mathrm{eff}} - (V_{\mathrm{bi}} + V'_{\mathrm{eff}})a_1}{a_2 - a_1},$$

and

$$K_2 = V_{\mathrm{bi}} + V_{\mathrm{ds}} + V'_{\mathrm{eff}} - \frac{V_{\mathrm{bi}} - V'_{\mathrm{eff}}a_1}{a_2 - a_1}.$$

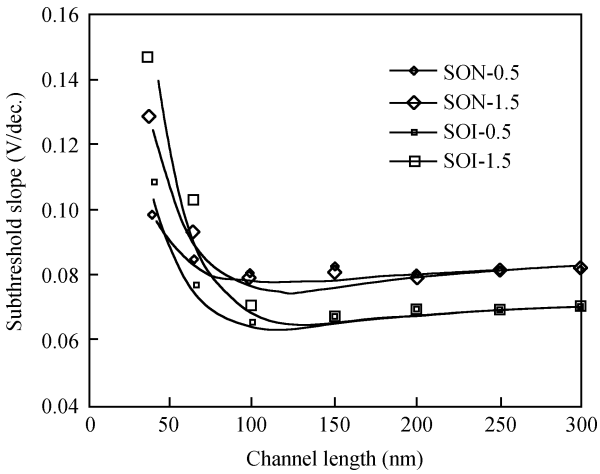

Fig. 5. Variation of subthreshold slope with channel length for SOI/SON MOSFETs for different V_{ds}: 0.5 and 1.5 V. Other parameters are the same as in Fig. 3 and symbols indicate the ATLAS simulated data.

3. Results and discussion

In a bulk MOSFET, the threshold voltage is derived only from the front interface surface potential ϕ_{sf}, neglecting the effect of ϕ_{bf}. However, in a short channel SOI-SON structure, ϕ_{sf} will be strongly influenced by the back interface potential ϕ_{bf}. The lowest dielectric constant material (air) in the box region causes significant modification in ϕ_{bf}, which affects ϕ_{sf}. This modification in ϕ_{bf} is responsible for the considerable performance improvement in the SON over an SOI structure. Neglecting quantum effect, bandgap narrowing and other second- and third- order effects, the threshold voltage performance of an SOI and an SON structure are simulated with a 2D analytical model and the results are verified with the results of the ATLAS physics based simulator.

The front interface surface potentials at different channel positions for three different channel lengths (50, 150 and 300 nm) of a uniformly doped SOI and SON MOSFET are shown

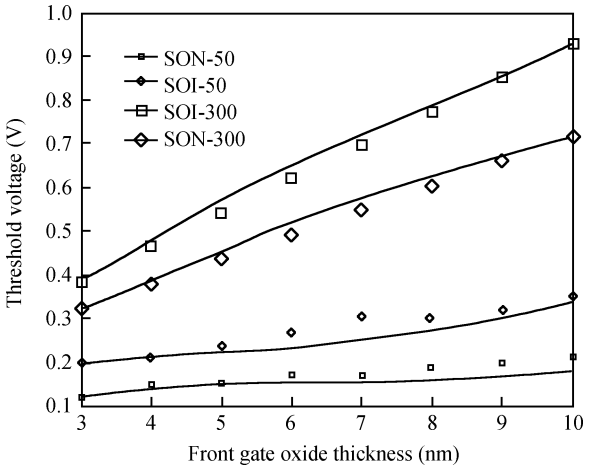

Fig. 6. Threshold voltage variation with t_f channel lengths of 100 nm and 300 nm. $V_{ds} = 1$ V and other parameters and symbols are the same as in Fig. 3.

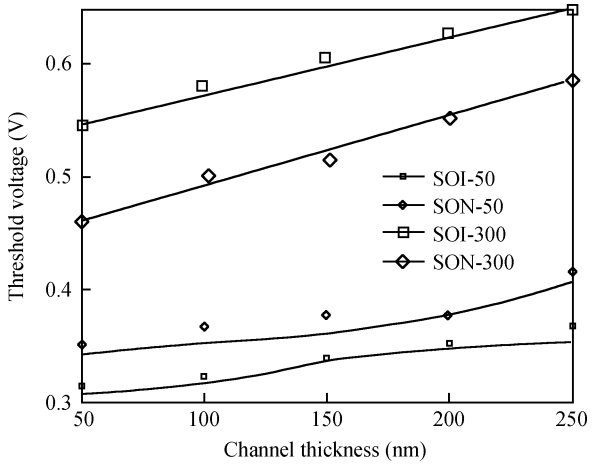

Fig. 8. Threshold voltage variation with t_{Si} for channel lengths of 100 nm and 300 nm, respectively. $V_{ds} = 1$ V and the other parameters and symbols are the same as in Fig. 3.

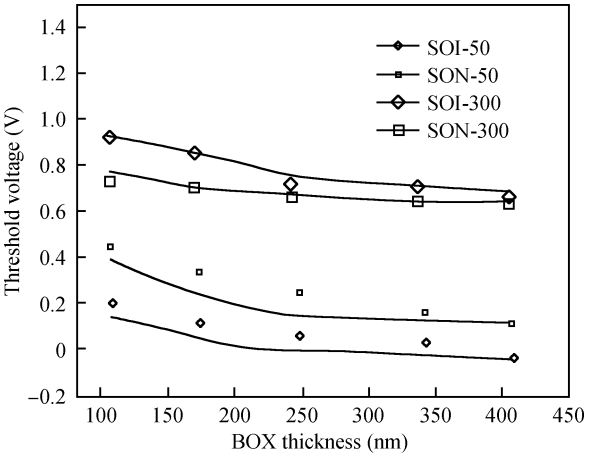

Fig. 7. Threshold voltage variation with $t_{BL/air}$ for channel lengths of 100 nm and 300 nm. $V_{ds} = 1$ V and the other parameters and symbols are the same as in Fig. 3.

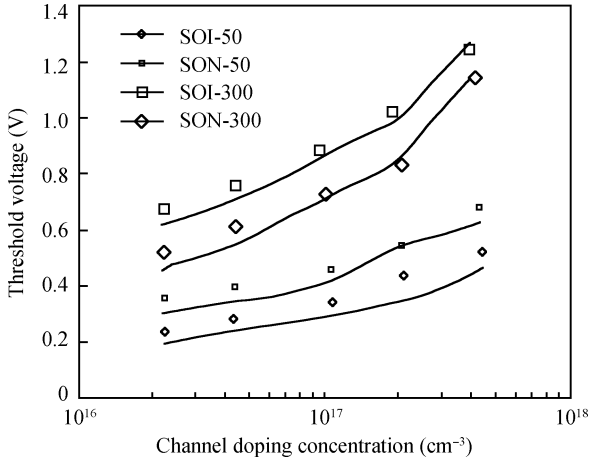

Fig. 9. Threshold voltage variation with N_A for channel lengths of 100 nm and 300 nm, respectively. $V_{ds} = 1$ V and the other parameters and symbols are the same as in Fig. 3.

in Fig. 3. As expected, the potential variation is almost symmetric about the midpoint of the channel for a long channel length (300 nm) for both the SOI and the SON. The minimum value of the surface potential is less for the SON at comparatively higher channel lengths, 300 and 150 nm, but for a lower channel length (50 nm), the SOI has a lower surface potential minima. The minimum value of the surface potential shifts upward as the channel length reduces because of the SCEs and this upward shift of the minimum surface potential is less for the SON structure as compared to the SOI structure. The decrease in channel length not only shifts the minimum surface potential upward but also causes a drift towards the source side because of DIBL or 2DCS effects.

Variation of threshold voltage and subthreshold slope with channel length for SOI and SON MOSFET are shown in Figs. 4 and 5, respectively. Threshold voltage roll-off and subthreshold slope are found to be less in the SON due to a reduced potential coupling ratio ($P_{CR} = \phi_{sf}/\phi_{bf}$) in SON. The higher drain bias initiates higher SCEs, which cause higher threshold voltage roll-off and a higher subthreshold slope.

Variation of threshold voltage with front gate oxide and BL/air thicknesses are plotted in Figs. 6 and 7, respectively. The threshold voltage increases with an increase in t_f for both the short- and long-channel devices due to the reduced control of the front gate voltage over the channel. For the short-channel length device, ϕ_{sf} is strongly influenced by ϕ_{bf}, as a result the rate of increase of the threshold voltage with t_f is less as compared to the long-channel length device. With increasing buried layer thickness, the influence of ϕ_{bf} reduces and as a result the threshold voltage also reduces.

Threshold voltage variation with silicon channel thickness and channel doping concentration are plotted in Figs. 8 and 9, respectively. The threshold voltage increases with channel thickness because the device approaches a bulk value and a higher gate voltage is required to create inversion. The nature of the threshold voltage slope can be explained with different P_{CR} values at 50 nm and 300 nm channel lengths, respectively. The results of the analytical simulation are compared with simulated data from ATLAS and they are found to be in good agreement.

4. Conclusion

A 2D Poisson's solution based generalized threshold voltage model for SOI/SON MOSFETs has been developed and analytical expressions for threshold voltage and sub-threshold slope have been derived. Different short-channel field effects like fringing field, junction induced lateral field and substrate field are incorporated in the analytical threshold voltage model. The performance of the two devices is studied and compared in terms of the threshold voltage roll-off and subthreshold slope, which are very important issues relating to the performance analysis of a short-channel MOSFET. Effects of the variation of different parameters, such as channel length, channel thickness, gate oxide thickness, buried layer thickness and channel doping concentration, on the threshold voltage are also investigated and analyzed to understand the comparative performance of the two structures. The short-channel SON structure shows less threshold voltage roll-off and less subthreshold slope compared to the short-channel SOI structure. The present analysis shows that SON MOSFET technology is able to offer devices with scalability and enhanced performance due to higher immunity against SCEs. SON structures provides scope for further miniaturization of devices for the next generation of CMOS structures.

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