Dry etching of poly-Si/TaN/HfSiON gate stack for advanced complementary metal–oxide–semiconductor devices*

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Abstract: A novel dry etching process of a poly-Si/TaN/HfSiON gate stack for advanced complementary metal–oxide–semiconductor (CMOS) devices is investigated. Our strategy to process a poly-Si/TaN/HfSiON gate stack is that each layer of gate stack is selectively etched with a vertical profile. First, a three-step plasma etching process is developed to get a vertical poly-Si profile and a reliable etch-stop on a TaN metal gate. Then different BCl_3-based plasmas are applied to etch the TaN metal gate and find that $BCl_3/Cl_2/O_2$/Ar plasma is a suitable choice to get a vertical TaN profile. Moreover, considering that Cl_2 almost has no selectivity to Si substrate, BCl_3/Ar plasma is applied to etch HfSiON dielectric to improve the selectivity to Si substrate after the TaN metal gate is vertically etched off by the optimized $BCl_3/Cl_2/O_2$/Ar plasma. Finally, we have succeeded in etching a poly-Si/TaN/HfSiON stack with a vertical profile and almost no Si loss utilizing these new etching technologies.

Key words: TaN metal gate; HfSiON high-k; plasma etching; selectivity; integration

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1. Introduction

As the metal–oxide–semiconductor field-effect transistor (MOSFET) dimension is scaled down to 45 nm nodes and below, a conventional poly-Si/SiO_2 gate stack needs to be replaced by a metal gate/high-k dielectric to reduce direct tunneling leakage current and to eliminate the poly-Si gate depletion effect, the boron penetration effect and Fermi-level pinning[1]. Currently, integration of Hf-based high-k dielectrics, such as HfO_2, HfAlON, HfSiON, and HfLaON, and metal gate electrode materials, such as TaN, TiN, HfN, TaSiN, and Ru, has been widely studied for the next generation of CMOS devices. In order to facilitate their integration, one widely used approach is to insert a thin metal gate layer between a high-k dielectric and poly-Si, resulting in a metal inserted poly-Si stacks (MIPS) structure. However, adoption of these new materials and MIPS structure imposes some integration problems. Among these, dry etching of the MIPS structure is expected to be one of the critical steps in the process integration.

TaN/HfSiON is one of the possible candidates as a metal gate/high-k gate stack in the MIPS structure, but the widely used method for poly-Si/SiO_2 etching does not work for a poly-Si/TaN/HfSiON gate stack because TaN/HfSiON is relatively difficult to etch due to the less volatile halides. There are reports on etching TaN with Cl_2 or Cl_2/Ar[2], Cl_2/SF_6/Ar[3], HBr/Cl_2[4], BCl_3/Ar/O_2[5] and BCl_3/N_2[6]. Also, some studies have already been performed on a Hf-based high-k dielectric[7, 8] and MIPS structure etching[9]. However, none of the aforementioned papers has described the dry etching of the TaN/HfSiON stack capped with poly-Si.

In this article, we focus on the dry etching of a poly-Si/TaN/HfSiON gate stack. First, a dry etching process suitable for the poly-Si in the MIPS structure has been developed. Furthermore, we have investigated different BCl_3-based plasmas for TaN metal gate etching and found an appropriate plasma process to get a vertical TaN profile. Finally, a separate etching strategy for the TaN/HfSiON stack is proposed to attain both a vertical profile and high selectivity to Si substrate.

2. Experiment

For sample preparation, after a standard cleaning process, a SiO_2 interfacial layer of 6–7 Å was grown by rapid thermal oxidation (RTO), then a HfSiON (30 Å) film was deposited onto the SiO_2 interfacial layer by co-sputtering of Hf and Si targets in an Ar/N_2 ambience followed by rapid thermal annealing (RTA) at 900 ℃ for 30 s. After that, a TaN metal gate of 110 or 140 Å was deposited on the HfSiON gate dielectric through reactive sputtering of a Ta target in Ar/N_2 ambient. A wafer was then capped with a 110 nm poly-Si deposited using low pressure chemical vapor deposition (LPCVD) at 610 ℃. The etching of the poly-Si/TaN/HfSiON gate stack was performed with a 65 nm SiO_2 hard mask (HM) deposited by low temperature oxide (LTO) at 500 ℃. The patterning of oxide HM is beyond the scope of this article.

After lithography for the MIPS gate stack, etching of HM and poly-Si were performed in a LAM Rainbow 4520 and 4420, respectively. The LAM Rainbow 4520 and 4420 are both single wafer plasma/RIE etching systems. RF power at 13.56 MHz is applied to the top electrode coil and to the substrate holder to induce plasma and a DC self-bias voltage to the wafer. And a TaN/HfSiON gate stack was patterned using a LAM TCP9600 configured for 150 mm wafers. This is a transformer-coupled plasma (TCP) reactor that allows separate control of the plasma power and substrate bias. The substrate and cham-

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ber wall temperature during the experiments was maintained at 60 ℃.

After etching of the poly-Si/TaN/HfSiON gate stack, the chemical composition of the exposure surface was measured by X-ray photoelectron spectroscopy (XPS), and gate profiles were inspected by scanning electron microscopy (SEM). In addition, blanket TaN wafers were studied by X-ray diffraction (XRD) to determine the poly-Si deposition temperature influence on the TaN crystalline structure.

3. Results and discussion

Introduction of a thin metal layer and high k dielectric in the gate stack not only requires new plasma etch chemistries and approaches to etch these novel materials but also impacts the whole etch process of gate stack. Our strategy to process a poly-Si/TaN/HfSiON gate stack is as follows. First, a poly-Si layer is anisotropically etched and the etching stops on the TaN metal layer; then, a TaN metal gate is vertically etched with a reliable etch-stop on a HfSiON dielectric; finally, the HfSiON dielectric is completely removed with high selectivity to the Si substrate.

In a typical poly-Si gate etching process on a thin gate oxide using $HBr/Cl_2/O_2$ chemistries, the process is composed of four steps, including breakthrough, main etch, soft landing and over etch step. The soft landing is a key step to remove the foot generated at the bottom of the poly-Si gate during the main etch step and to obtain an anisotropic etching profile of poly-Si, since positive charge builds up on the gate oxide and this charge tends to induce an ion trajectory distortion, which in turn can impact the profile control at the bottom of the gate. However, introduction of a metal layer in the gate stack cancels the notching capability of the soft landing step because there is no positive charging on a conductive metal gate layer[9]. So, a three-step etching process using Cl_2/HBr chemistry without a soft landing step has been developed to optimize the poly-Si etching on the metal gate. The first step of etching, breakthrough, is to remove the thin nature oxide on the surface of the unmasked poly-Si area at RF power = 300 W, chamber pressure = 750 mTorr and CF_4 = 100 sccm. The second step of etching, the main etch, is to etch the poly-Si vertically, which is done in a gas mixture of Cl_2/HBr = 80 sccm/ 40 sccm, RF power = 280 W, and chamber pressure = 250 mTorr. The third step of etching, over etch, is to offset the non-uniformity of the main etch and improve selectivity to the underlying metal, which is done in a gas mixture of Cl_2/HBr = 70 sccm/50 sccm, RF power = 130 W, and chamber pressure = 260 mTorr. The optimized three-step poly-Si etching process provides a vertical poly-Si profile and a reliable etch-stop on the TaN metal gate, as shown in Fig. 1.

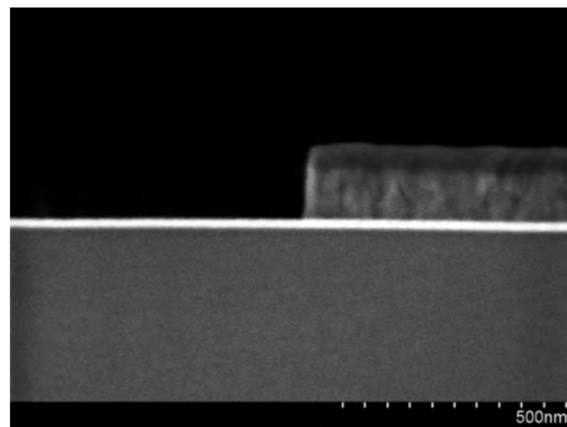
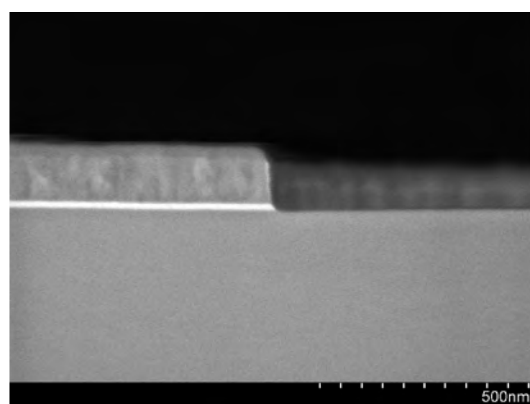


Fig. 1. SEM image of the poly-Si etching profile after etching poly-Si on a TaN metal gate.

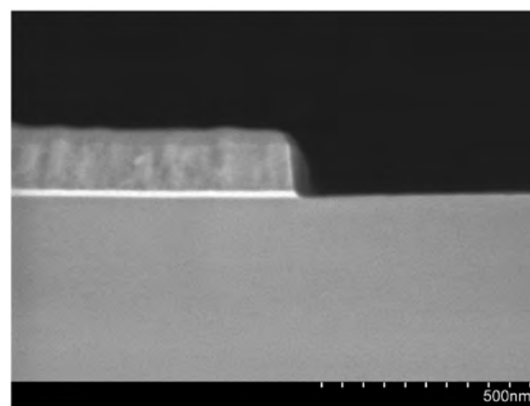
3.1. Poly-Si etching process for MIPS structure

3.2. TaN metal gate etching process

After vertically etching poly-Si and stopping on the TaN metal gate, the next technological step is to optimize the etching of the TaN metal gate. Since BCl_3-based plasma is capable of etching both the TaN metal gate and the HfSiON dielectric with reasonable selectivity over the Si substrate[5, 10], it is also chosen as a promising candidate for the etching of TaN and HfSiON in the MIPS structure. Initially, we evaluated TaN metal gate etching with BCl_3/Ar plasma under different process conditions and found that a "footing" was always observed at the bottom of the gate, indicating that the TaN metal gate had a tapered profile. For example, Figure 2(a) shows a tapered profile of TaN etched in the following conditions: top power of 180 W, bottom power of 150 W, pressure of 4 mTorr, BCl_3 flow of 45 sccm and Ar flow of 15 sccm.



(a)



(b)

Fig. 2. SEM images where TaN (110 Å) in the HM/poly-Si/TaN stack was etched with (a) BCl_3/Ar and (b) BCl_3/N_2/Ar plasma.

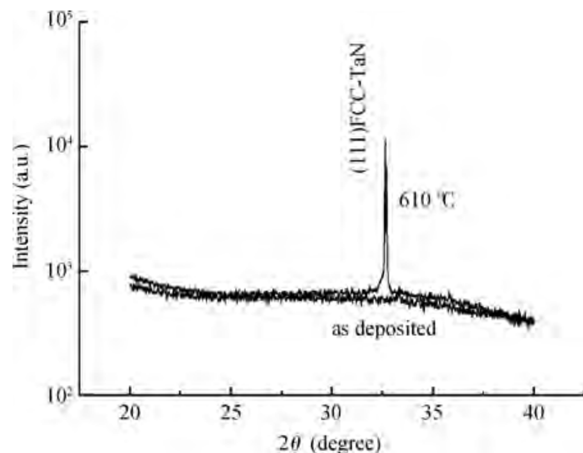
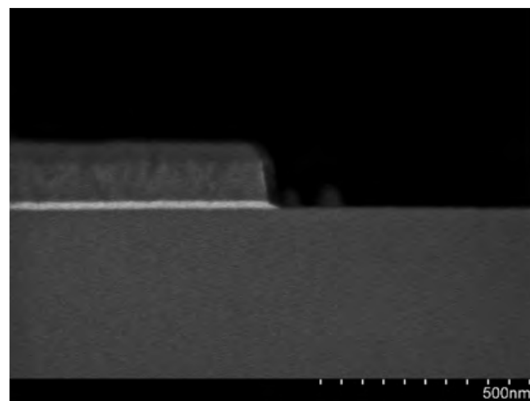


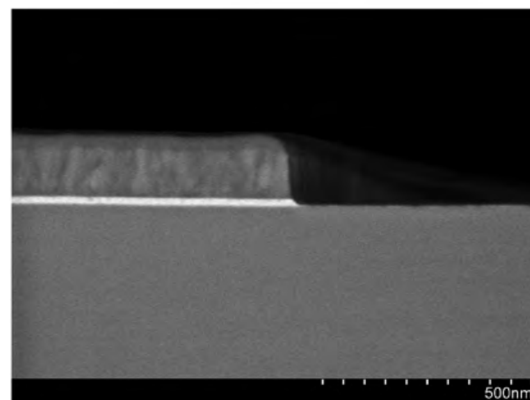
Fig. 3. XRD spectra of the as-deposited TaN and annealed TaN at 610 ℃ in N_2 ambient.

The previous reports of TaN etching indicated that the patterning of TaN in BCl_3 plasma usually obtained a notch profile[5, 6], while profiles of TaN etched with BCl_3/Ar plasma in our experiments were all tapered. One of the factors in the present experiments is that the TaN metal gate was capped with poly-Si and exposed to temperatures as high as 610 ℃ during poly-Si deposition. In order to determine the poly-Si deposition temperature influence on the TaN crystalline structure, XRD spectrum analyses of the deposited TaN and annealed TaN that just went through the thermal budget for poly-Si deposition without actual poly-Si deposition are shown in Fig. 3. It was found that the deposited TaN is amorphous, as no crystalline peaks were found in the XRD spectrum. However, the annealed TaN crystallizes, exhibiting a peak at about 33°, which corresponds to the reported crystalline structure of TaN[11]. Although the polycrystalline structure of TaN may have different etch properties compared with the as-deposited TaN because chlorine is sensitive to the crystallographic orientation of the etched materials, especially for metals, further optimization of the etching process, such as increasing the bottom power making the plasma less selective to different crystallites, could result in a vertical profile of TaN[12]. However, this phenomenon is not observed in our experiments. So, we do not propose that a different crystalline structure of TaN is the reason for the tapered profile of TaN. We hypothesized that a possible reason for the tapered profile of TaN may be accounted for by non-volatile B-related passivation film. One possible passivation layer is BN-like film because B radical species generated from BCl_3 gas preferentially react with N atoms in TaN, leading to the formation of nonvolatile products containing B–N bonds[13]. The other plausible passivation layer is the non-volatile boron–chlorine compounds (BCl_x) deposited from the plasma, as mentioned in Refs. [6, 7].

In order to clarify which factors lead to the tapered profile and to further optimize the etching process of TaN to get a vertical etch profile, we use different additives with BCl_3/Ar plasma, such as N_2, O_2 and Cl_2. Figure 2(b) presents a profile of TaN etched with BCl_3/N_2/Ar plasma under the same conditions as Fig. 2(a) except decreasing the BCl_3 flow to 40 sccm and adding a N_2 flow of 5 sccm. As nitrogen is added to BCl_3/Ar plasma, the etch rate of TaN decreases a little due to a reduction in the Cl ion density, but the profile of TaN shows almost no change compared with the TaN etched by BCl_3/Ar plasma. If the tapered profile of TaN is related to the BN-like passivation film, the addition of N_2 should cause more BN-like passivation film, which will lead to a more sloped profile. So, we propose that the tapered profile of TaN is not attributed to BN-like passivation film deposition and the addition of N_2 to BCl_3/Ar plasma could not improve the profile of TaN in our case.



(a)



(b)

Fig. 4. SEM images where TaN (140 Å) in the HM/poly/TaN stack was etched by BCl_3/O_2/Ar plasma with different O_2 flows. (a) O_2 flow at 2 sccm. (b) O_2 flow at 6 sccm.

Figure 4 shows profiles of TaN etched by BCl_3/O_2/Ar plasma with the following conditions: top power of 300 W, bottom power of 160 W, pressure of 5 mTorr, BCl_3 flow of 45 sccm, O_2 flow of 2 sccm and 6 sccm, and Ar flow of 15 sccm. It was found that the profile of TaN became less sloped as the O_2 flow increased from 2 to 6 sccm and further increasing the O_2 flow to 8 sccm did not change the profile of TaN (not shown here). This phenomenon evidently indicates that the tapered profile of TaN is related to passivation film deposition. When O_2 is added to BCl_3/Ar plasma, oxygen can scavenge boron by forming volatile BO_x and reduce the amount of BCl_x film deposition[7]. However, oxygen can also promote the redeposition of a Ta–Cl–O compound on the sidewall because the Ta–oxygen–halogen compound is more stable and less volatile than the Ta–halogen compound. So, we propose that the profile of TaN may be attributed to the competition of different types of passivation films after a small amount of

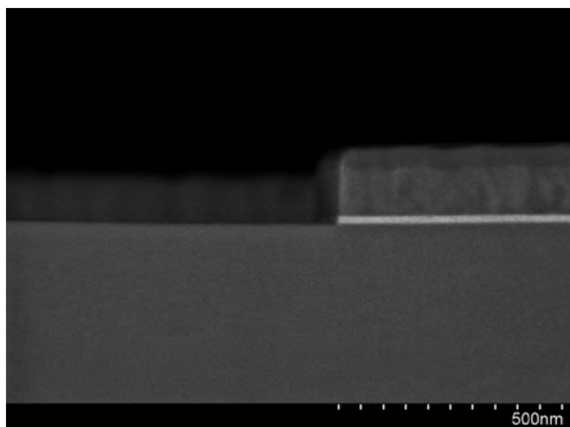


Fig. 5. SEM image where TaN in the HM/poly-Si/TaN stack was etched by $BCl_3/Cl_2/O_2$/Ar plasma under the optimized conditions.

O_2 addition. The dominance of the passivation film shifts from BCl_x film to Ta–Cl–O compound as O_2 flow increases, which causes the change in the TaN profile. The Ta–Cl–O compound becomes the only passivation film as the oxygen concentration increases to a certain extent, making the profile of TaN no longer change. Therefore, we believe that only the addition of O_2 to BCl_3/Ar could not get a vertical profile of TaN either, but the profile could attain some improvement by optimizing the oxygen content by controlling different types of passivation film deposition.

As Cl_2 is added to the BCl_3/Ar plasma, the etching rate of TaN is enhanced and the tapered profile becomes less sloped with increasing ratio of Cl_2/BCl_3. It can be explained that the tapered profile of TaN is caused by passivation film deposition, such as BCl_x, which provides more passivation than Cl radical species etching, so increasing the volume density of the Cl radical and reducing the volume density of B by incorporating Cl_2 into BCl_3-based plasma could produce less passivating and improve the profile of TaN. In addition, a little O_2 is also added to BCl_3/Cl_2/Ar plasma to preserve the poly-Si gate profile during TaN etching and get a slower and more controllable etch rate of TaN. Therefore, the next key step to get a vertical etch profile is to optimize the ratio of BCl_3/Cl_2 and process conditions by finding a proper balance between anisotropic etching by Cl radical and passivation deposition. A vertical etch profile and smooth sidewall were achieved with TaN of 110 Å in the gate stack under the condition that the flow rate ratio of BCl_3 to Cl_2 is about 1 : 1, as shown in Fig. 5.

3.3. TaN/HfSiON gate stack etching process

Although a vertical etching profile of the TaN/HfSiON stack could be obtained using $BCl_3/Cl_2/O_2$/Ar plasma, it is very difficult to obtain a high etch selectivity of high-*k* dielectric to Si substrate since Cl_2 has almost no selectivity to Si substrate. Therefore, a separate etching of metal gate followed by high-*k* dielectric removal may be a practical solution. We propose a separate etching method for the TaN/HfSiON gate stack, namely the TaN metal gate is vertically etched by $BCl_3/Cl_2/O_2$/Ar plasma and the remaining HfSiON high-*k* dielectric is completely removed using BCl_3/Ar plasma with high selectivity to Si substrate. Figure 6 presents a SEM image

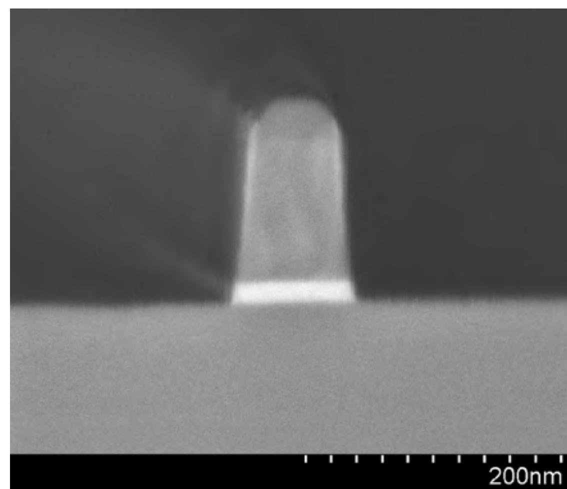


Fig. 6. SEM image of a poly-Si/TaN/HfSiON stack etched by a separate etching method.

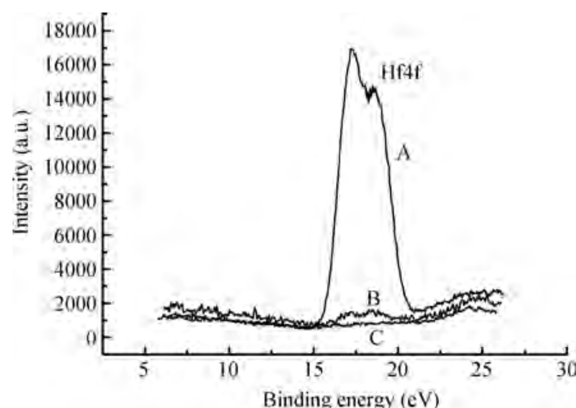


Fig. 7. Hf4f XPS spectra obtained from the exposure surface after the TaN/HfSiON stack was etched by endpoint with $BCl_3/Cl_2/O_2$/Ar plasma and followed by BCl_3/Ar plasma etching for (a) 0 s, (b) 4 s, (c) 6 s.

of a poly-Si/TaN (110 Å)/HfSiON (30 Å) stack etched by endpoint with $BCl_3/Cl_2/O_2$/Ar plasma and followed by BCl_3/Ar plasma etching for 6 s. It can be seen that the profile of the poly-Si/TaN/HfSiON stack was vertical with an angle greater than 85 degrees and the Si substrate loss was very little.

In order to confirm whether TaN and HfSiON were completely removed, XPS measurement results were obtained in Fig. 7 for a TaN/HfSiON stack etched by endpoint with $BCl_3/Cl_2/O_2$/Ar plasma and followed by different BCl_3/Ar plasma etching times. The results indicate that TaN was completely removed and HfSiON film was still existing after the TaN/HfSiON stack was etched by endpoint with $BCl_3/Cl_2/O_2$/Ar plasma because there was no Ta element left (not shown here) and Hf element still had obvious peaks, which ensures that the Si substrate will not be etched by Cl_2. There was a little Hf4f peak with 4 s of BCl_3/Ar plasma etching, which indicates that the HfSiON film was not completely removed, and the Hf4f peak completely disappeared with 6 s of BCl_3/Ar plasma etching. Therefore, the optimized separate etching method for the TaN/HfSiON gate stack is successfully applied to completely remove TaN and HfSiON with a vertical

profile and little Si substrate loss.

4. Conclusions

In summary, a novel dry etching process suitable for a poly-Si/TaN/HfSiON gate stack has been developed. The vertical profile of poly-Si and TaN are both attained by optimizing the plasma etching process. Moreover, considering that Cl_2 has almost no selectivity to Si substrate, a separate etching method is applied to etch a TaN/HfSiON gate stack. Finally, dry etching of a poly-Si/TaN/HfSiON stack with a vertical profile and almost no Si loss is successfully obtained using these new etching technologies.

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