A novel high reliability CMOS SRAM cell

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Abstract: A novel 8T single-event-upset (SEU) hardened and high static noise margin (SNM) SRAM cell is proposed. By adding one transistor paralleled with each access transistor, the drive capability of pull-up PMOS is greater than that of the conventional cell and the read access transistors are weaker than that of the conventional cell. So the hold, read SNM and critical charge increase greatly. The simulation results show that the critical charge is almost three times larger than that of the conventional 6T cell by appropriately sizing the pull-up transistors. The hold and read SNM of the new cell increase by 72% and 141.7%, respectively, compared to the 6T design, but it has a 54% area overhead and read performance penalty. According to these features, this novel cell suits high reliability applications, such as aerospace and military.

Key words: single-event-upset; static noise margin; critical charge; SRAM
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1. Introduction

As integrated circuit geometries continue to scale down, it is possible to achieve extremely high density in one circuit. However, the aggressive scaling of CMOS technology also suffers reliability of operation with respect to external circumstances. For SRAM, with the feature size shrinking and the supply voltage decreasing, there are three reliability problems to be faced: single-event upset (SEU)[1], hold SNM and read SNM.

When ions strike the storage cell's sensitive node, the data stored in the cell may be corrupted and lead to system failure. Corrupted data due to a single particle is termed as SEU[2, 3]. Due to the lower supply voltage and the smaller node capacitance, the amount of charge stored on a circuit node is smaller, increasing the susceptibility of SEUs to particles. Nowadays, the SRAM cell can upset even in normal terrestrial circumstance for those advanced technology. To solve this problem, quite a number of SEU hardening design techniques, such as hardening process and design, have been developed to mitigate the threat of SEUs.

To reduce the dynamic and leakage power, the supply voltage is decreased. However, this trend makes the conventional six transistors SRAM cell encounter stability problems; for example, the hold and read SNM are getting smaller and smaller. Furthermore, low supply voltage and limited beta ratio (the ratio between the pull-down MOSFET and the access MOSFET) cause operation failure and loss of yield[4].

In this paper, a novel 8T SRAM cell is proposed to alleviate those reliability problems mentioned above. Though this new 8T cell suffers layout area and read performance penalties, it can strengthen SEU immunity, and enhance the stability of the cell and so the yield of the chips. It is suitable for aerospace, military and high-reliability applications.

2. SEU mechanisms and SRAM cell's SNM

2.1. SEU mechanisms

A basic 6T SRAM cell and the layout cross-section of one inverter are shown in Fig. 1. Basically, the circuit comprises two cross-coupled CMOS inverters forming a bi-stable latch and two NFET access transistors that provide controlled access to the two data nodes of the latch. In its static mode, the latch has an ON transistor at each of its data nodes, which actively couple the node to a supply voltage.

There are two situations in this storage cell. One is that Q couples to V_{cc} and QB couples to V_{ss}. PD-1 and PU-2 are cut off and its reverse-biased drain depletion regions are the SEU sensitive volumes. The other is that QB couples to V_{cc} and Q couples to V_{ss}, and the sensitive volumes are similar to those above. The reverse-biased drain depletion region of cutoff NMOS is more sensitive to SEU than PMOS and is about three times larger than PMOS[5]. So the reverse-biased drain depletion region of the cutoff NMOS is the shortest piece of wooden barrels. The track of the ion loses its energy and generates ionization charge (electron–hole pairs: EHP), as illustrated in Fig. 1. The excess charges that escape recombination are collected by Q as a result of a single-event ion hit. The min-

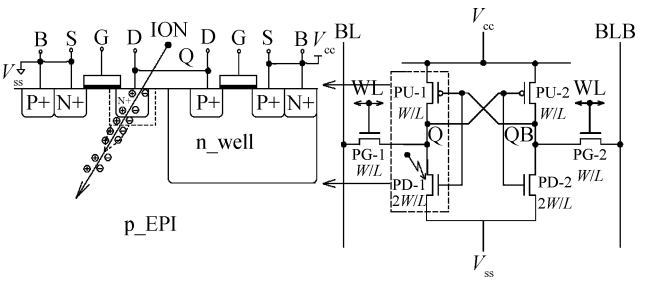

Fig. 1. Conventional 6T cell and ion strike schematic.

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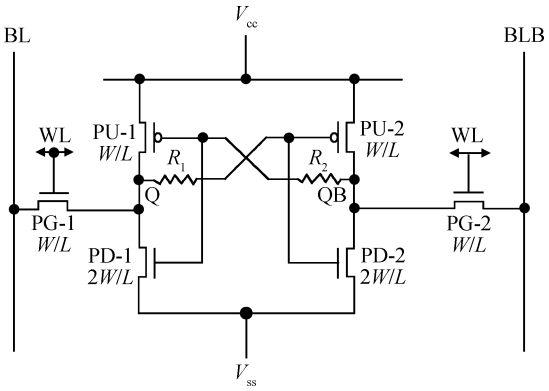

Fig. 2. Resistive hardening cell.

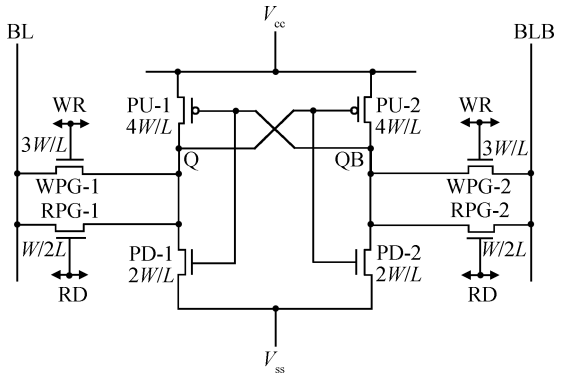

Fig. 3. Proposed 8T cell.

imum amount of charge that needs to be collected by a sensitive data node to cause an upset is referred to as the critical charge, Q_{crit}. Whether an observable SEU occurs depends on which happens faster: the feedback of the voltage transient through the opposite inverter, or recovery of the struck node voltage as the single-event current dies out[6]. In a 6T cell, because of the read-write constraint condition, the drive ability of pull-up PMOS is 1/4–1/6 compared to pull-down NMOS. When the ion strikes at the pull-down NMOS, the pull-up current $I_{\text{p, on}}$ is small because the drive ability is weak. This difference aggravates the SEU sensitivity of NMOS and decreases Q_{crit}.

Design hardening techniques can usually be classified into two brand categories[7]. In the first, the storage cells are designed to be insensitive to transient current independent of the circuit electrical parameters, such as sizing of the transistors and the capacitance of the nodes of a cell. An example of the hardening cell in the first category is a DICE cell[8]. This approach has the advantage of technology independence, but it may cause a significant design overhead due to the additional circuitry. In the second category, hardening is achieved by increasing the capacitance of critical nodes as well as the resistors between cross-coupled inverters. A typical example of the second category is the current pulse feedback time resistive hardening cell, as shown in Fig. 2.

If the resistor's values of R_1 and R_2 are too large, it will affect the write performance of the cell. However, as the technology scales, this resistor's value must increase to achieve the SEU immunity. These two considerations are conflicting.

2.2. Hold and read SNM

There are strict constraints on the sizing of transistors to be able to maintain the data stability and functionality of standard 6T SRAM cells. In order to maintain the read stability, the current produced by PD-1 and PD-2 must be higher compared to the access transistors PG-1 and PG-2. Alternatively, for write ability, the current conducting capability of PG-1 and PG-2 must be stronger compared to PU-1 and PU-2. For read stability, write ability, and sufficient feedback pull-up strength, the ratio of the width of PD, PG and PU is 4 : 2 : 1.

The static noise margin (SNM) is the metric used in this paper to characterize the stability of the SRAM cells. The SNM is defined as the minimum noise voltage necessary to flip the state of a SRAM cell[9]. So the hold and read SNM is the side length of the maximum nested square between voltage transfer characteristics of the two data storage nodes during hold and read access, respectively.

Because the constraints of the stability of read and write, latched inverters are high skewed gates and the hold SNM is small. In the meantime, the read stability cannot increase by the strength of the drive ability of pull down NMOS. This method will worsen the hold SNM.

3. Proposed highly reliable cell

The proposed highly reliable cell is shown in Fig. 3. It adds two extra access transistors in parallel with the originals. It needs two access signals, RD and WR. When reading, BL and BLB are pre-charged to a high level, and then the RD signal goes to a high level and turns on RPG-1 and RPG-2. One of the bit-lines is discharged through the storage node, which couples to V_{ss}. When writing, BL and BLB are pre-charged to a high level, then the column multiplexer connects selected bit-lines to a write driver and one bit-line is driven to V_{ss} and the other to V_{cc}. WR and RD signals turn on simultaneously and the data are written in selected cells.

In this configuration, extra transistors, WPG-1 and WPG-2 are added to the memory cell to separate the read and write operations. Its read and write operations are similar to those of the traditional 6T cell. Compared to a 6T SRAM cell, there are three advantages, as follows.

3.1. Larger Q_{crit}

In a 6T cell, the reversed drain of NMOS is very sensitive to SEU for its relatively weak pull-up PMOS. The traditional method is to add capacitance or resistance to increase the feedback time, as described above. This method conflicts with the fast write operation. This new cell focuses on weak pull-up PMOS, i.e. recovery time. The weak PMOS is caused by read-write constraints and reduces Q_{crit}. In this new cell, the read and write operation uses different access transistors, so the drive ability can be enhanced by the transistor size design. Much PMOS drive capability decreases the recovery time and so Q_{crit} increases.

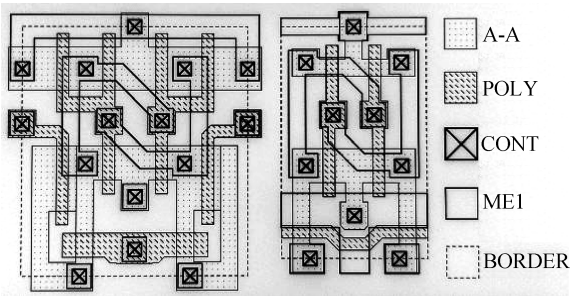

Fig. 4. Layout comparison.

3.2. Larger hold SNM

When the cell is in storage mode, a SRAM cell is presented as two equivalent inverters. The voltage transfer characteristics (VTC) of both inverters are depicted in one coordinate system with an exchanged $x-y$ axis, as illustrated in Fig. 6. A hold SNM is defined as the maximum square drawn between the inverter's VTC characteristics. Because of a weak PMOS and strong NMOS in the inverter, the hold SNM of a traditional 6T cell is small. In this new cell, the inverters are not highly skewed, so the hold SNM increases.

3.3. Larger read SNM

In a 6T cell, its read SNM is relatively small. This is caused by the contradiction of the hold SNM and the read SNM. The most effective way to increase the read SNM is to decrease the drive ability of the access transistor. This will cause a weaker PMOS and decrease the hold SNM and read performance. In the proposed cell, the read access NMOS drive capability can shrink but does not affect the hold SNM. In this way, a new cell can attain a larger read SNM and the poor read performance can be enhanced by an appropriate block partition.

In the next section, area, SNM, $Q_{\rm crit}$ and read-write performance will be compared between the novel cell and the conventional cell through HSPICE simulation.

4. Simulation result comparison

Figure 4 shows the layout of two cells, based on 0.13 μm technology. The left of Fig. 4 is the layout of the proposed cell and the right is the conventional cell. Its transistor size ratio is shown in Figs. 1 and 3. The area of the proposed cell is 2.05 $\times$ 1.83 μm^2, and that of the conventional cell is 1.33 $\times$ 1.83 μm^2.

The proposed cell has a 54% area penalty compared to the conventional cell. According to these two cell layouts, RC net-lists are extracted by process files. $Q_{\rm crit}$, hold SNM, read SNM and read/write operation simulation are performed based on these two RC net-lists.

4.1. $Q_{\rm crit}$ simulation

A high-energy heavy ion strike is modeled by a trapezoidal pulsed current source to simulate the dynamics of the prompt charge collection at sensitive data nodes, since for the static cells the drift component generally poses the greater SEU threat compared to the diffused component of charge collection at a sensitive node[8]. The current pulse had a fixed 0.05 ns pulse-width and variable amplitudes were adjusted to determine the minimum amount of excess charge needed to cause an upset. The product of the pulse-width and the amplitude represents the total charge collected by the node due to a single ion strike. When this current pulse source is placed between a sensitive data node and $V_{\rm ss}$, this means ion strike at a drain of NMOS.

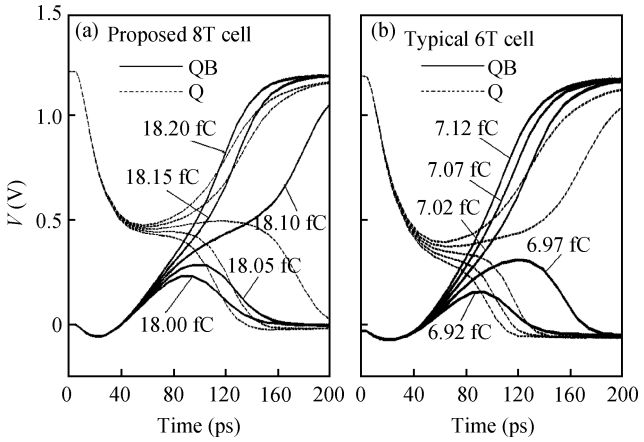

Fig. 5. SEU response simulation results of (a) the proposed 8T cell and (b) the typical 6T cell.

Figure 5 shows the SEU response of simulation results for the novel and conventional cell at ambient temperature and TT (typical NMOS and typical PMOS) process corner. In Fig. 5(b), the charge of the current noise sweep from 6.92 to 7.12 fC for the conventional cell and the interval is 0.05 fC, because this interval will not introduce large errors compared to the order of magnitude. Due to 6.97 fC, charge cannot flip the cell, but 7.02 fC charge flips the cell, so the $Q_{\rm crit}$ of the traditional cell is 7.02 fC. Similar simulations of the novel cell were performed and are shown in Fig. 5(a). From this figure, the novel cell's $Q_{\rm crit}$ is 18.10 fC.

4.2. Hold SNM simulation

The stability of a SRAM cell is usually defined by the SNM as the maximum value of DC noise voltage that can be accepted by the SRAM cell without changing the stored bit. The SNM can be graphically measured on the butterfly curve[9]. In this paper, the VTC of inverters were simulated by HSPICE and the maximum square between the inverter characteristics was derived by mathematical manipulation of the measured data after the butterfly curves of the cell were obtained.

Figure 6(a) shows the holding butterfly curve of two cells through simulation at ambient temperature and TT process corner. The hold SNM calculation results are 0.25 V and 0.43 V for the traditional and the proposed cell, respectively.

4.3. Read SNM simulation

The read SNM simulation is similar to the hold SNM simulation and it is also obtained from the VTC of the inverter through DC sweep simulation. The difference is that the RD is at a high level and the BL and BLB are at high level too.

Figure 6(b) shows the read butterfly curve of two cells through simulation. The read SNM was calculated and the re-

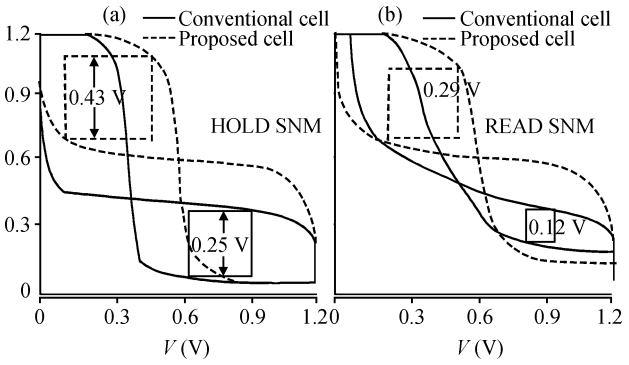

Fig. 6. (a) Hold and (b) read butterfly curves of the proposed 8T cell and the conventional 6T cell.

Table 1. Read/write time.

Cell	6t cell	8t cell
Write time (ns)	0.11	0.05
Read time (ns)	0.15	0.20

sults are 0.12 V and 0.29 V for the traditional and the proposed cell, respectively.

With scaling of MOSFET dimensions, technology variation, for example the microscopic variations of doping atoms in the channel region of the device, increasingly limiting electrical deviations in the device characteristics. These variations are most pronounced to SRAM for its minimum-geometry transistors and will introduce threshold mismatch in one cell[10]. This mismatch will result in reduction in SNM, and when SNM degrades to a certain extent, read operations that minimize the cell's SNM will lead to storage data corruption. The proposed cell's read SNM is enhanced greatly and is very suitable for advanced technology with aggressive dimension and low V_{cc} to enhance the chip's yield.

4.4. Read and write operation

In this proposed cell, the drive ability of access transistors is reduced to provide high read SNM. The read performance will be worsening. Because two parallel access transistors are turned on when writing, the write performance will be improved.

The performance of the proposed and the conventional cell is compared by HSPICE simulation. Assuming that there is a 1 Mbit memory and its array configuration is 256-row × 256-column × 16-bank, the read and write simulation schematic is one column of a bank, as shown in Fig. 7. The read time is specified as the time between WL changes to 0.6 V and BL or BLB changes to 0.9 V. The write time is defined as the time between WL changes to 0.6 V and Q or QB changes to 0.6 V.

Table 1 gives the simulated read/write time. From the table, the write time decreased from 0.11 to 0.05 ns. As we expected, the write performance increased by 54.5%, but the read time increased from 0.15 to 0.20 ns, by 33.3%.

Worsening of the read performance can be compensated by shrinking the number of the cell in one memory bit-line. In Fig. 7, the memory array configuration is that one bit-line connects 256 memory cells. By changing the memory array configuration to 128-row × 256-column × 32-bank, one column of a bit-line connects 128 memory cells. In this way, the capacitance of one bit-line decreases, so the read performance fault compensates and the simulated read time reduces to 13 ns.

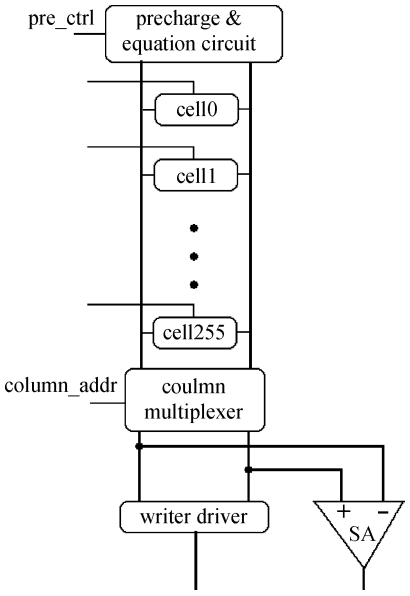

Fig. 7. Read/write simulate circuit: one column of a bank.

5. Summary

A new 8T SRAM cell is presented in this paper to enhance the read and hold SNM while increasing the critical charge of SEU as compared to the conventional 6T SRAM circuits. The proposed static memory circuit adds two access transistors parallel to the originals, so it needs two different access signals, RD and WR, for the read and write operations, respectively. During a read operation, the RD signal is valid and two access transistors are weaker than that in the conventional cell are turned on, thereby enhancing the read SNM by 147% compared to the conventional 6T SRAM cells. During a write operation, RD and WR signals are valid and four access transistors stronger than that in the conventional cell are turned on, and thereby the drive ability of pull-up PMOS increases. In this way, the hold SNM increases by 72% compared to the conventional cell. A greater benefit brought by PMOS drive strength is to increase the critical charge of the cells for SEU. With HSPICE simulation, the critical charge of this new cell is about three times greater than that of traditional cells. The proposed cell can form registers, cache and a single SRAM chip and is suitable for advanced deep sub-micron process technology for its higher read SNM. It can be used in fields such as the military and aviation that require high reliability. It can also be used in harsh radiation environments for its SEU hardened performance.

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