A radiation-hardened SOI-based FPGA

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Abstract: A radiation-hardened SRAM-based field programmable gate array VS1000 is designed and fabricated with a 0.5 μm partial-depletion silicon-on-insulator logic process at the CETC 58th Institute. The new logic cell (LC), with a multi-mode based on 3-input look-up-table (LUT), increases logic density about 12% compared to a traditional 4-input LUT. The logic block (LB), consisting of 2 LCs, can be used in two functional modes: LUT mode and distributed read access memory mode. The hierarchical routing channel block and switch block can significantly improve the flexibility and routability of the routing resource. The VS1000 uses a CQFP208 package and contains 392 reconfigurable LCs, 112 reconfigurable user I/Os and IEEE 1149.1 compatible with boundary-scan logic for testing and programming. The function test results indicate that the hardware and software cooperate successfully and the VS1000 works correctly. Moreover, the radiation test results indicate that the VS1000 chip has total dose tolerance of 100 krad(Si), a dose rate survivability of 1.5×10^{11} rad(Si)/s and a neutron fluence immunity of 1×10^{14} n/cm^2.

Key words: radiation-hardened; FPGA; partial-depletion SOI; reconfigurable LC; routing channel block; switch block

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1. Introduction

Field programmable gate arrays (FPGAs) have become the key design and manufacturing vehicle for implementing a vast majority of digital circuits due to its advantages over application-specific integrated circuits (ASICs) such as lower depreciated mask costs and a fast time to market. However, some features of FPGAs implemented with bulk-CMOS technology, especially radiation hardened performance, can still not meet the increased demands for aerospace and military applications. To endure the harsh environment of space, including total dose radiation, transient phenomena and single event upset, aerospace systems require radiation-hardened components. In contrast to the traditional bulk CMOS, silicon-on-insulator (SOI) materials have a higher silicon density, smaller parasitic capacitance, better latch-up immunity and, in particular, better radiation hardened performance. Therefore devices and circuits with a high radiation-hardened level using SOI technology are very important for high performance space systems.

Combining the above advantages of FPGAs with those of SOIs, a VS1000 FPGA fabricated with a 0.5 μm SOI-CMOS logic process is presented in this paper. Atmel ATFS450[1] and Honeywell HXRFP6010[2] are both SOI-based FPGA products with high reliability features. JAXA[3] in Japan also has finished its SOI-FPGA design for space systems based on Atmel architecture in 2009. However, similar FPGA samples or products are still very scarce. The work reported in this paper represents our effort not only to explore the architecture design for FPGAs, but also to fabricate it with an SOI-CMOS logic process at the CETC 58th Institute.

2. VS1000 FPGA architecture

Figure 1 depicts the architecture of the tile-based VS1000 FPGA, which contains 14×14 programmable logic tile (LT) arrays, 56 programmable I/O blocks (IOB), 2 programmable global signal blocks (GB) and programming logic (PGM).

As the basic building block of the VS1000, the LT is made up of a logic resource (LB) and a hierarchical programmable routing resource (CHB). Each LT contains an LB, a CHB in horizontal direction (CBX), a CHB in vertical direction (CBY) and a switch block (SB).

An IOB provides the interface between the chip pins and internal signals. Each IOB contains 2 I/O cells (IOC) and a dedicated I/O interconnection resource. Each IOC contains input, output and tristate control logic.

The GB, independent of the CHB, serves as the dedicated source and routing channel for global signals, such as clock and global set/reset signals.

In addition to the above fundamental components, it also contains IEEE 1149.1 standard compatible boundary-scan logic for testing and programming. The PGM supports three different modes for bitstream downloading: JTAG, serial master (SM) and serial slave (SS).

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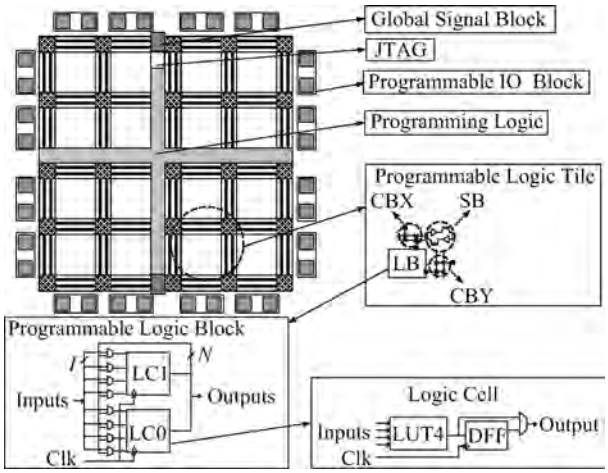

Fig. 1. VS1000 architecture.

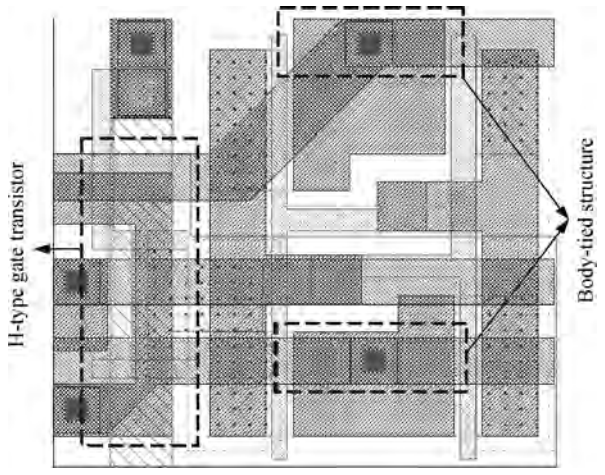

Fig. 2. Body-tied five-transistor memory cell.

2.1. Radiation hardened design

The SRAM-based VS1000 uses a five-transistor (5T) memory cell[4] to store configuration bits. So the functional correctness of the FPGA depends on all of the SRAM cells' contents. The SOI devices' floating-body effect will worsen under a radiation environment and result in an upset, from '0' to '1' or '1' to '0', of the SRAM cell content. Then the FPGA chip will fail to work. So the 5T SRAM cell was specially designed using body-tied techniques and an H-type gate transistor structure[5] to suppress the floating-body effect based on the natural radiation-hardened performance of SOI material, as Figure 2 shows.

Body-tied techniques can stabilize the voltage of the body and avoid triggering a BJT effect by tying the bodies of the NMOS and PMOS transistors to their own sources. This helps to restrain the floating-body effect and reduce the transient current of the BJT under a radiation environment. The stable body voltage can also greatly decrease the parasitic capacitance mismatch of the corresponding bit lines, which is good for the read operation of an SRAM cell.

The typical T-type gate body-tied structure is not suitable for transistors with a large width because of its large body-tied resistor, which is not good for quickly transferring the electric charge caused by radiation in the floating body. Therefore an H-type gate body-tied structure is proposed to decrease the body-tied resistor. It consists of two connected T-type body-tied structures, one opposite to the other.

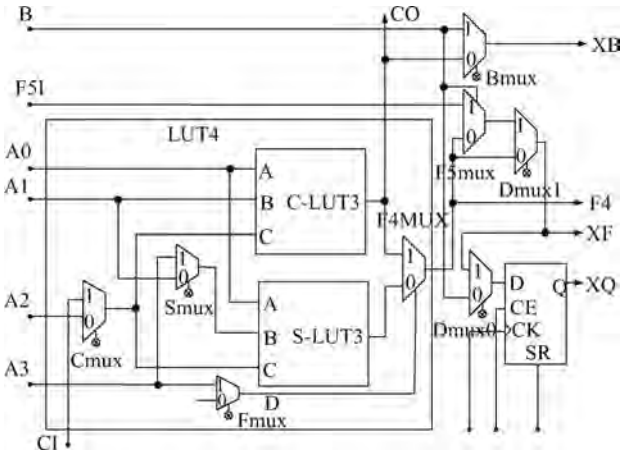

Fig. 3. Logic cell.

Table 1. Four common modes of LC.

LC mode	Smux	Cmux	Fmux	Function
1	0	0	1	LUT4
2	0	1	0	Carry-chain
3	0	0	0	Carry head
4	1	0	0	Multiplier

In addition to radiation hardening by technology (RHBT) techniques, radiation hardening by design (RHBD) was also used during the development of VS1000. SPICE models under post-radiation conditions are used to simulate the chip functionality and the whole layout of VS1000 was designed using a full-custom method.

2.2. Logic block architecture

2.2.1. The novel logic cell architecture

Figure 3 shows the novel logic cell architecture. An LC is composed of a 4-input LUT and a D-type flip-flop. Unlike a general 4-input LUT structure, the 4-input LUT consists of two 3-input LUTs and four multiplexers. Obviously, the LC can be configured into 8 (2^3) modes based on the control bit patterns of the three multiplexers, Smux, Cmux, and Fmux. As such, the LC can not only realize two 3-input logic functions or one of any 4-input logic functions by combining the two 3-input LUTs, but also many other functions. After an extensive analysis of the benchmark circuits, the four most frequently used LC modes are listed in Table 1.

For example, LC mode 1 functions as a normal 4-input LUT. LC mode 2 implements the fast carry-chain logic in the one-bit full-adder, which can be expressed as

$$S = A \oplus B \oplus C_{\mathrm{i}}, \tag{1}$$

$$C_{\mathrm{o}} = AB + (A \oplus B)C_{\mathrm{i}}, \tag{2}$$

where $C_{\mathrm{i}}/C_{\mathrm{o}}$ is carry-in/carry-out. The sum and carry-out can be implemented by S-LUT and C-LUT, respectively. This will

Table 2. Comparison between 4-LUT and VS1000-LUT.

MCNC Benchmarks	4-input LUT	VS1000-LUT	Gain (%)
c1908	125	105	16
misex3c	263	231	12.2
dalu	413	363	12.1
spla	559	493	11.8
t481	691	641	7.2
table3	785	702	10.6
ex1010	1069	930	13
des	1438	1244	13.5
Average	680	601	12.1

cut down area consumption roughly by half in comparison with a normal 4-input LUT. Mode 3 can be used as carry-chain head logic, i.e., full-adder logic without input C_i. The LUT-based multiplier logic can be realized using mode 4 combined with mode 2. Two LCs are used: one LC in mode 4 produces two partial products and the other LC in mode 2 adds them to get the final result. A traditional scheme would use four LCs to implement a LUT-based multiplier slice. Therefore the distinct advantage of the new LC is that it can realize two independent 3-input logic functions while the 4-input LUT can only waste half of the LUT area to realize a 3-input logic. The experimental results based on the MCNC benchmark circuits in Table 2 show that the 3-input LUT based LC improves logic density by about 12% compared with implementation based on a traditional 4-input LUT using the technology mapping of our FPGA application toolset. The LC of Altera FLEX family FPGAs[6], Atmel AT40k Family FPGAs[7] and FDP chips[8] are all 3-input LUT based, but each are defined in a different architecture.

Furthermore, Bmux can be configured to fit a logic from the input BI to bypass the entire LC or to be registered before output. BI can also be used to cascade the registers of the LC chain. The D-type flip-flop of the LC can be configured as a DFF or a latch.

2.2.2. Logic block architecture

As Figure 4 shows, the cluster-based LB[9] is composed of 2 LCs, an input and output local routing pool (LRP) and a distributed RAM logic. The LB inputs include global signal inputs and data inputs. The input LRP provides the interconnections between LB data inputs and LC data inputs, between LB global signal inputs and LC clock or set/reset signals, between logic '0' or '1' and LC inputs, and between LC feedback outputs and LC inputs. Similarly, the output LRP is used to connect LC outputs to LB outputs.

The values of flexibility of connection (Fc) between LB I/Os and LC I/Os are based on the tradeoff between area and speed. Each LC pin has a different logic characteristic that determines its need for routing resources and is reflected in the Fc value. Our design strategy is to minimize the Fc values based on the minimal routing needs of LC pins. As such, the area consumption is cut down without obvious performance degradation. The local interconnection among LCs through LPR is faster than LB channel routing due to a shorter wire and switching delay.

All LB I/Os are evenly distributed around the LB perimeter and each LC I/O can be evenly connected to LB I/Os of the same type. Both of which can significantly improve the routability of the routing channel.

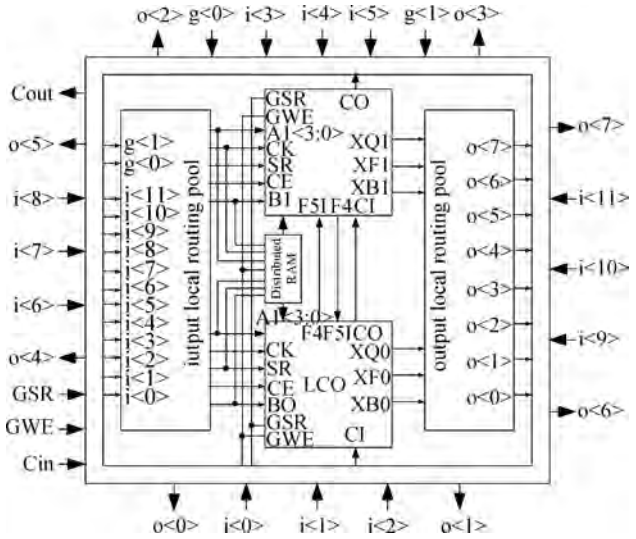

Fig. 4. Logic block.

Table 3. Logic bock modes.

Mode		Control bit			
		S1	S2	S3	D
LUT		0	0	0	0
Distributed RAM	Single-port 16 × 1	1	0	0	0
	Single-port (16 × 1) × 2	1	1	0	0
	Single-port 32 × 1	1	0	1	0
	Dual-port 16 × 1	1	0	0	1

An LB can implement any 5-input Boolean function using F5mux. Compared with the 3-input H-LUT of the Xilinx Spartan family CLB[10], F5mux can improve speed when the LB are configured as 5-input LUT or single-port 32 × 1 RAM. Furthermore, the two F5mux outputs in LB can benefit a high fan-out signal.

As shown in Table 3, an LB can be configured as a LUT or a distributed RAM by using different control bit patterns. Details for distributed RAMs are omitted in this paper.

2.3. Hierarchical routing resource architecture

The VS1000 programmable routing resource adopts the most typical hierarchical routing architecture, which thus provides excellent performance for FPGA implementation. It consists of two levels: a local routing pool inside the LB and a routing channel block outside the LB.

Figure 5 shows the top view of the hierarchical routing architecture. The local routing pool includes the ILRP and OLRP, which choose LC inputs from LB inputs and LB outputs from LC outputs, respectively. The ILRP receives 14 inputs from LB and provides 13 inputs to the 2 LCs. The OLRP receives 6 outputs from them and provides 8 outputs to LB. The routing channel block consists of a CBX, a CBY and SB. CBX and CBY have identical architectures. There are three types of segment wires in the CHB: single-length, double-length and longlines. The SB provides the interconnections between the

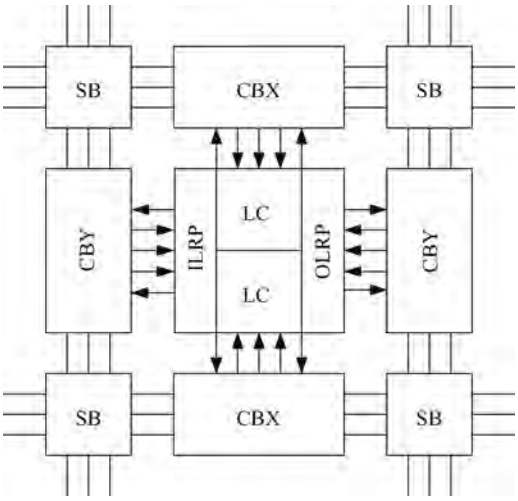

Fig. 5. VS1000 hierarchical routing architecture.

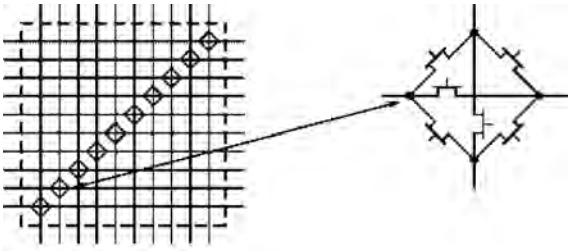

Fig. 6. VS1000 programmable switch block.

Table 4. Connections among wire segments.

Segment	Single-length	Double-length	Longlines
Single-length	8	0	6
Double-length	0	4	0
Longlines	6	0	0

horizontal and vertical wire segments, and the CHB connects the inputs and outputs of LB to wire segments.

Single-length lines and Double-length lines are connected by a disjointed type SB, as Figure 6 shows. Double-length lines are grouped in pairs with staggered SBs, so that each line goes through an SB at every other row or column of LBs. Longlines which run the entire length or widths of the LT array are intended for high fan-out or a time-critical signal net. In SB the single-length line and longlines can be connected for improving the routing flexibility and performance of the VS1000 chip. The connections are summarized in Table 4, where the number indicates the connections between wires.

2.4. VS1000 architecture evaluation

The detailed architecture of an FPGA specifies the number of LCs in an LB (N), the number of inputs to the LB (I), the Fc value of the local routing inside the LB for the LC inputs and outputs, the Fc value for LB inputs and outputs, the routing channel width (W), the length of every wire, the type of switch used to make every connection, the SB topology, the metal layer, width and spacing of each routing wire, and several other related parameters[9].

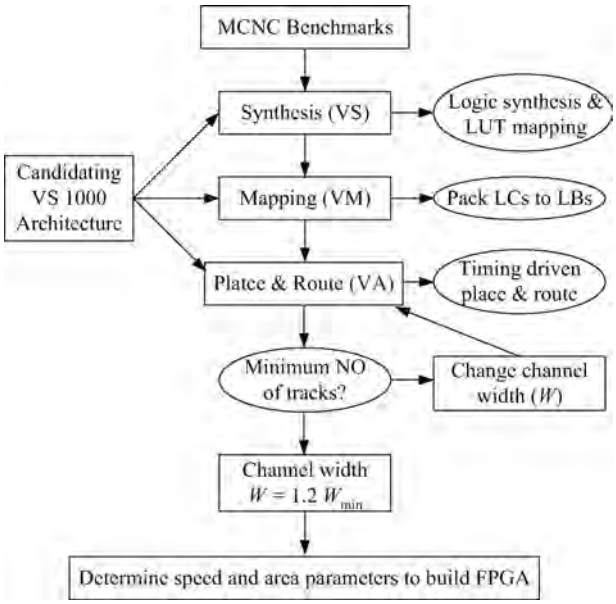

Fig. 7. VS1000 architecture evaluation flow.

Table 5. VS1000 architecture parameter.

Architecture		Parameter
VS1000	Array size	14 × 14
LB	LB inputs, I	12
	LB outputs, O	8
Local connection	ILRP input Fc (A0, A1, A2, A3)	6/12
	ILRP input Fc (B)	3/12
	ILRP input Fc (CK, SR, CE)	2/12
	OLRP output Fc (XB)	2/8
	OLRP output Fc (XF, XQ)	4/8
Channel connection	CHB input Fc (I<11:0>)	16/18
	CHB output Fc (O<7:0>)	8/18
Segments routing	Channel width, W	18
	Single-length	8
	Double-length	4
	Longlines	6

These parameters are interdependent. Therefore, we must determine every parameter using special evaluation programs and statistical analysis based on the other parameters by making tradeoff between chip speed and area. Figure 7 shows the VS1000 architecture evaluation flow.

First, the MCNC benchmarks were optimized logically and mapped to LUTs and DFFs by a VS based on Icarus[11]. Then the LUTs and DFFs were packed into an LB by a VM based on T-VPack[12]. Finally, placement and routing were implemented by a VA based on VPR[9]. This flow was iterated until the minimal channel width was achieved. Table 5 lists the architecture parameters of VS1000.

3. Implementation of VS1000 FPGA

The VS1000 chip was designed and fabricated with a 0.5 μm partial-depletion SOI-CMOS logic process at the CETC 58th Institute. The entire chip layout was designed with the full custom design method. The VS1000 die size is about

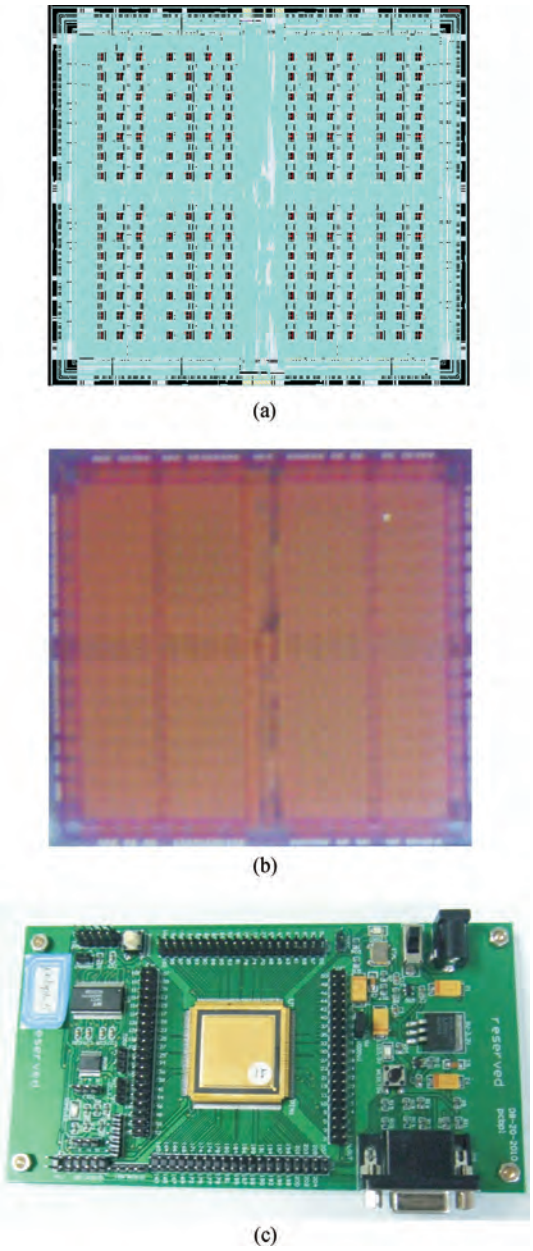

Fig. 8. (a) VS1000 layout. (b) Photo. (c) Test board.

10.2×9.5 mm^2 with a CQFP208 package. Figure 8 shows the VS1000's layout, die photo and test board.

We also developed the corresponding VS1000 design kit (VDK), which includes logic synthesis and technology mapping (VS), packing LUTs and DFFs into LB (VM), place & routing (VA), bit stream generation (VB), downloading tool (VT). The VDK is ignored in this paper.

3.1. Fault and functional test

Based on the FPGA testing research in Refs. [13–18], we propose a rich set of test vectors for the VS1000 fault and function tests. These vectors are generated using a semi-automated approach. First, we write a verilog file and its user constraint file (UCF). Then a bitstream file is generated by our VDK using those two files. Finally, the test vector tool generates the vector file after a simulation using the bitstream file. As shown in Table 6, a total of 128 test vectors[19] are classified according to the different configuration modes of several blocks, such as LB, CHB, GB, IOB. All of them can be used in chip tests and packaged tests. The total average test coverage is estimated to be 85%. The functionality test coverage is a subjective measure of the functionalities of each tested block type array. All test experiments are performed using a Teradyne J750 test system at the CETC 58th Institute, which can provide 1024 I/O channels and 100 MHz vector rates.

Table 6. Total testing cases for FPGA chip.

Block type	Configuration mode		Function test coverage
LB array	LUT mode	Mode1|Mode2|Mode3|Mode4	95%
	RAMD mode	RAMD16x1S|S_1 RAMD16x1D|D_1 RAMD16x1Sx2|2_1 RAMD32x1S|S_1	
	Flip-flop mode	FD|FD_1|FDC|FDC_1|FDP(total 24 types)	
CHB array	SB type & track type	Diagonal-1 | diagonal-2 | orthogonal Single | double | long	80%
GB array	Global tracks & gcs	8 global tracks & 8 gcs	85%
IOB array	buffer mode & ioc flip-flop mode	CMOSIN|CMOSOUT| pullup|pulldown| open-drain enable | idelay enable | FF (24 types)	82%
Total test cases		128	85%

Xilinx Spartan XCS10 and VS1000 both contain 14×14 CLB arrays and are based on 0.5 μm CMOS logic process, so we make some comparisons between them. The first difference is Spartan CLB[10] uses H-LUT to implement the last level multiplexer, but VS100 uses F5MUX. H-LUT is identical to the three level cascaded F5MUX, so the later has improvements in timing. Second, Spartan is based on 0.5 μm bulk-CMOS process but VS uses 0.5 μm SOI-CMOS process, so the latter also has an improvement in timing. Due to the two above improvements, the test results indicate that both the maximum LUT logic propagation delay and the distributed RAM average access time are improved by about 20%. Table 7 shows the performance summary of VS1000 and XCS10 and some comparisons between them.

3.2. Radiation test

The radiation tests included a total ionizing dose (TID) test, a dose rate test and a neutron fluence test. The TID test was done in a Co-60 gamma source with a dose rate of 50 rad(Si)/s. We monitored the real-time work current change and the function correctness of VS1000 under the radiation environment. The work currents of VS1000 before, under and after irradiation are very close and the function under and after irradiation are both correct. Finally, the test results show that the total dose tolerance is superior than 100 krad(Si). Table 8 lists the all radiation test results.

Table 7. Performance summary of XCS10 and VS1000 and comparisons between them.

	XCS10	VS1000	Improvement
Supply voltage (V)	5	5	—
CLB architecture	H-LUT3	F5MUX	Timing
Logic process	0.5 μm bulk-CMOS	0.5 μm SOI-CMOS	Timing
Max LUT logic propagation delay (ns)	2	1.6	20%
Average distributed RAM access time (ns)	4.5	3.55	21.1%
Max clock frequency (MHz)	80	100	20%
Quiescent current (mA)	3	< 10	—
Max system gates (K)	10	10	—

Table 8. Radiation test results.

Radiation test	Result
TID	100 krad(Si)
Dose rate	1.5×10^{11} rad(Si)/s
Neutron fluence	1×10^{14} n/cm^2

4. Conclusion

In this paper a radiation-hardened FPGA VS1000 is designed and fabricated with 0.5 μm partial-depletion SOI logic process. Both RHBT and RHBD are used to improve its radiation-hardened performance. The proposed 3-input LUT based LC with multi-mode increases logic density by about 12% compared with a traditional 4-input LUT. The LB can be used in two functional modes: LUT mode and distributed RAM mode. Comparing with the published data about the CLB in a Xilinx Spartan FPGA, both the maximum LUT logic propagation delay and the distributed RAM average access time show about 20% improvement. The hierarchical routing channel block (CHB) and switch block (SB) can significantly improve routability of routing resource. The function test results indicate that the hardware and software cooperate successfully and the VS1000 chip works correctly. The radiation test results show that the VS1000 chip a has total dose tolerance of 100 krad(Si), a dose rate survivability of 1.5×10^{11} rad(Si)/s and a neutron fluence immunity of 1×10^{14} n/cm^2.

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