A 5 Gb/s transceiver in 0.13 μm CMOS for PCIE2.0*

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Abstract: This paper presents a CML transceiver for a PCI-express generation 2 physical layer protocol that has been fabricated by SMIC's 0.13 μm CMOS technology. The active area of the transceiver is 0.016 mm^2 and it consumes a total of 150 mW power at a 1.2 V supply voltage. The transmitter uses two stage pre-emphasis circuits with active inductors, reducing inter-symbol interference and extended bandwidth; the receiver uses a time-domain adaptive equalizer, the circuit uses an inductive peaking technique and extends the bandwidth, and the use of active inductors reduces the circuit area and power consumption effectively. The measurement results show that this circuit could stably transmit the signal at the data rate of 5 Gbps, the output signal swing of the transmitter is 350 mV with jitter of 14 ps, the eye opening of the receiver is 135 mV and the eye width is 0.56 UI. The circuit performance sufficiently meets the requirements of the PCI-Express 2.0 protocol.

Key words: serial link; CML; pre-emphasis; adaptive equalizer; inductive peaking; active inductor
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1. Introduction

With the development of microprocessor architecture and semiconductor process technology, the clock frequency of modern high-performance microprocessors has exceeded 5 GHz. The interconnection between computers, computer peripherals and communications, etc., is pushing the data transmission rate into the gigabits-per-second (Gbps) range. Serial communication is faster, more reliable and requires fewer pins, etc., gradually substituting parallel communication in board level communication. Currently, the serial links are almost everywhere, and most of the communication between chips is serial.

The CML (current mode logic) is a low voltage difference signal transmission technology for high-speed serial interfaces that developed on the basis of ECL, LVDS. Low voltage swing, differential signal transmission and current driven models made it have high speed, low noise and low power consumption and low cost, etc. It is widely used in the network physical layer and high-speed SerDes. CML possesses these advantages, especially in high-speed data transmission capability, giving it great prospects for application.

In this paper, a CML high-speed serial transceiver suitable for the PCI express 2.0 physical layer protocol was designed. The transmitter adopted the two-stage pre-emphasis circuit with active inductors, having reduced the inter-symbol interference (ISI) and extended the bandwidth. The receiver adopted the time domain adaptive equalizer and its circuit used the inductive peaking technology to expand the bandwidth, and it adopted the active inductor to effectively reduce the chip area and power consumption.

2. System architecture

The overall structure of the CML high-speed serial interface circuit designed in this paper is shown in Fig. 1.

The transmitter is designed to drive the high-speed signal from on the chip to the devices on off-chip transmission lines. The driver circuit was divided into analog and digital modules. The digital module consisted of a level shift circuit and a single-ended to differential circuit; the analog circuit module consisted of a driving stage circuit and a pre-emphasis circuit, and the driving stage consisted of a pre-driving stage and a primary driving stage circuit. The use of a pre-emphasis circuit avoided the ISI resulting from serious loss of a decay high-frequency component on the transmission lines.

The receiver received the signal sent by the driver to the transmission line and accurately transmitted the signal to the on-chip circuit. It consisted of an adaptive equalizer, a limiting-like amplifier circuit, a comparator circuit, a level shift circuit, a shaping output circuit and the high stability reference voltage source circuit providing the equalizer with a reference level.

The receiver circuit should have a certain capability to identify the low-swing signal and ensure that the received differential signal could be transmitted to the on-chip circuit in the form of a single-ended signal reaching a specific duty ratio.

3. Circuit design

3.1. Transmitter

The transmitter mainly consisted of the modules of the level shift circuit, the single-ended to differential circuit, the

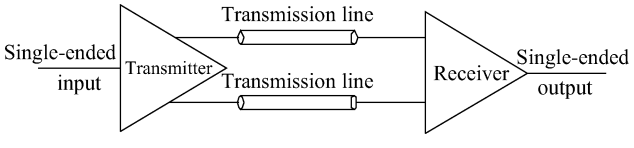

Fig. 1. A typical transceiver interface.

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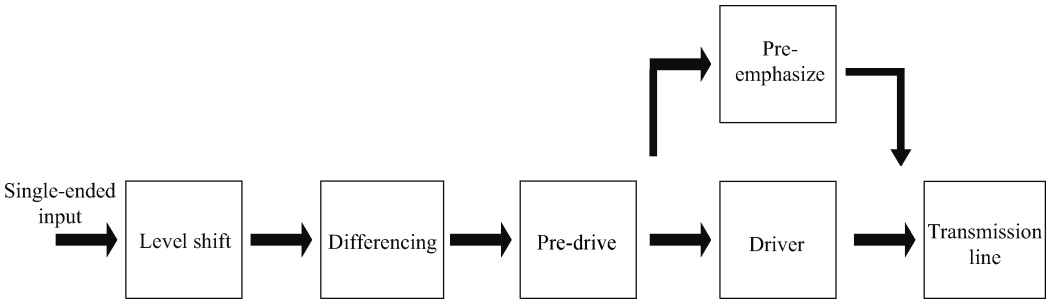

Fig. 2. Block diagram of the transmitter.

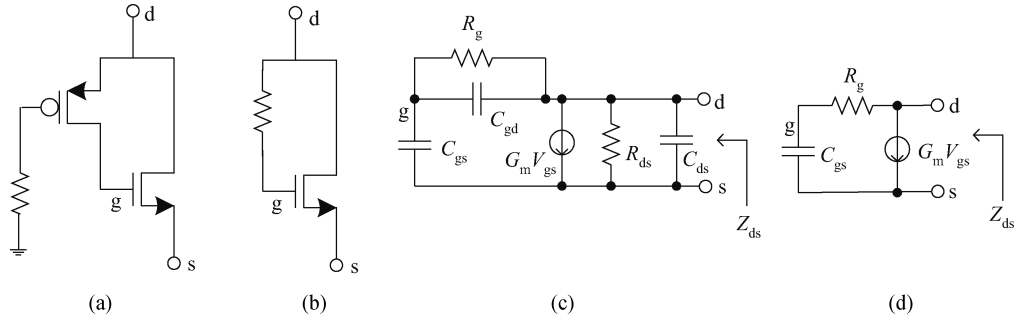

Fig. 3. Active inductance schemes.

driving stage circuit and the pre-emphasis circuit. A block diagram of the transmitter is shown in Fig. 2.

The level shift circuit transformed the low-level input signal of a 1.2 V supply voltage to the high-level signal of a 2.5 supply voltage to solve the problem of incompatible stages between the system internal and the I/O[2]. The single-ended to differential circuit mainly functioned to achieve the conversion from the single-ended signal to the differential signal.

The driving stage circuit consisted of a pre-driving stage module and a primary driving stage module. In order to effectively expand the system bandwidth, we applied the inductive peaking technique and the active negative feedback technique to the pre-driver.

The single-stage CML driving circuit was constructed with differential amplifiers as the basic unit, and its –3 dB bandwidth generally was of only about 1 GHz. The –3 dB bandwidth of the amplifier can be calculated from the following formula,

$$\omega_{\mathrm{H}} = \frac{1}{\sqrt{\left(\frac{1}{\omega_{\mathrm{P1}}^2} + \frac{1}{\omega_{\mathrm{P2}}^2} + \cdots\right) - 2\left(\frac{1}{\omega_{\mathrm{Z1}}^2} + \frac{1}{\omega_{\mathrm{Z2}}^2} + \cdots\right)}}, \tag{1}$$

where ω_{P1}, ω_{P2} $\cdots$ are the frequency values corresponding to the amplifier poles and ω_{Z1}, ω_{Z2} $\cdots$ are the frequency values corresponding to the amplifier zeros.

From the above formula, it can be seen that one approach to improve the amplifier bandwidth is to improve the frequency values corresponding to the poles of the amplifier. In a normal cascaded amplifier, the poles are mainly limited by the RC network consisting of the load resistances and parasitic capacitances, and the RC network has a significant low-pass property. By introducing a parallel inductive load to each gain stage to partially offset the capacitive load of the RC network, the pole of each stage can be moved to the high frequency end and the bandwidth can then be effectively expanded, which is called the inductive peaking technique.

In order to avoid the huge area consumption and the parasitic effect brought by the passive inductor, the active inductor with a simple structure and small area was adopted in our design to expand the bandwidth.

Figure 3(a) is the structural drawing of the active inductor used in this paper and the tube grid linked to the PMOS tube grid is a ESD protection resistor; Figure 3(b) is another form of circuit equivalent to the active inductor in this paper; Figure 3(c) is the small-signal model of the active inductor in this paper; Figure 3(d) is the simplified small-signal model of the active inductor.

Through the simplified small-signal model of the active inductor, its equivalent impedance can be obtained as

$$\begin{aligned} Z_{\mathrm{ds}} &= \frac{1 + sR_{\mathrm{g}}C_{\mathrm{gs}}}{G_{\mathrm{m}} + SC_{\mathrm{gs}}} = s\frac{\frac{R_{\mathrm{g}}}{\omega_{\mathrm{T}}} - \frac{1}{G_{\mathrm{m}}\omega_{\mathrm{T}}}}{1 + \left(\frac{\omega}{\omega_{\mathrm{T}}}\right)^2} + \frac{\frac{1}{G_{\mathrm{m}}} + R_{\mathrm{g}}\left(\frac{\omega}{\omega_{\mathrm{T}}}\right)^2}{1 + \left(\frac{\omega}{\omega_{\mathrm{T}}}\right)^2} \\ &= sL_{\mathrm{eff}} + R_{\mathrm{eff}}, \end{aligned} \tag{2}$$

where $L_{\mathrm{eff}} = \frac{\frac{R_{\mathrm{g}}}{\omega_{\mathrm{T}}} - \frac{1}{G_{\mathrm{m}}\omega_{\mathrm{T}}}}{1+(\frac{\omega}{\omega_{\mathrm{T}}})^2}$ is the equivalent inductance; $R_{\mathrm{eff}} = \frac{\frac{1}{G_{\mathrm{m}}} + R_{\mathrm{g}}(\frac{\omega}{\omega_{\mathrm{T}}})^2}{1+(\frac{\omega}{\omega_{\mathrm{T}}})^2}$ is the equivalent resistance in series with L_{eff}; and $\omega_{\mathrm{T}} = G_{\mathrm{m}}/C_{\mathrm{gs}}$ is the gain angular frequency per unit of current.

From the above derivation, it can be found that L_{eff} will increase along with the increase in resistance R_{g}. In order to avoid peaks in the frequency response of the circuit, L_{eff} has an optimal L_{opt}.

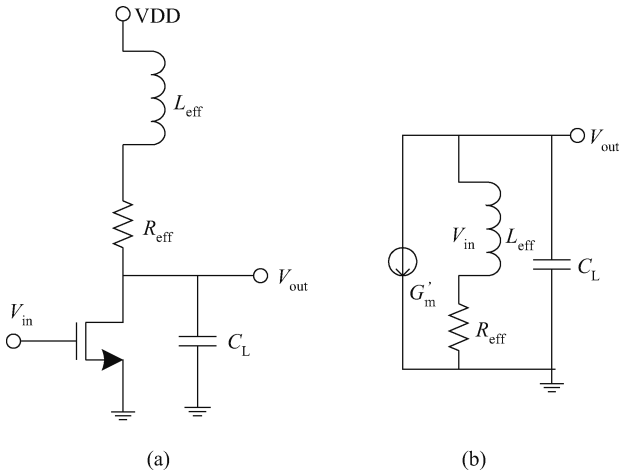

Fig. 4. (a) Differential gain stage schemes. (b) Small signal model.

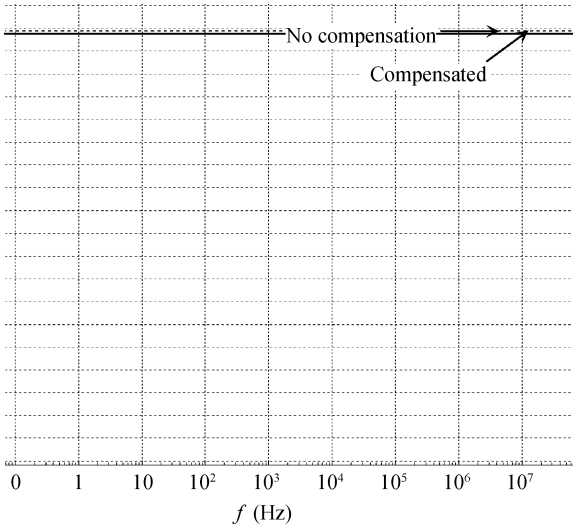

Fig. 5. Frequency response comparison.

Take the one-side equivalent circuit of the single-stage driver into consideration, and let the series of the inductors and resistors equal the active inductors, and let CL equal the secondary load effect. In this way, the equivalent circuit of the differential gain stage, as shown in Fig. 4(a), can then be obtained. Figure 4(b) shows its corresponding small-signal model.

From Fig. 4(b), the response frequency of the gain stage can be obtained as

$$\frac{V_{\text{out}}}{V_{\text{in}}}(\omega)=\frac{G_{\text{m}}'(R_{\text{eff}}+\text{j}\omega L_{\text{eff}})}{1+\text{j}\omega R_{\text{eff}}C_{\text{L}}-\omega^2 L_{\text{eff}}C_{\text{L}}},\quad m=\frac{R_{\text{eff}}C_{\text{L}}}{L_{\text{eff}}/R_{\text{eff}}}. \tag{3}$$

From Eq. (2), it can be found that the ratio m of the time constants determines the characteristic of response frequency of the gain stage with the inductive peaking technique. The bandwidth of the gain stage will decrease along with the increase in m, and the best flat-band response can be obtained at $m_{\text{opt}}=1+\sqrt{2}$, where the bandwidth is about 1.72 folds of that without the inductive peaking technique[3].

After using the active inductor for offsetting, a comparison of the frequency response curves of the single-stage CML buffer is shown in Fig. 5. It can be seen from this figure that the –3 dB bandwidth is extended to 6 GHz from 1 GHz after offsetting, and the CML buffer bandwidth obtains very significant expansion.

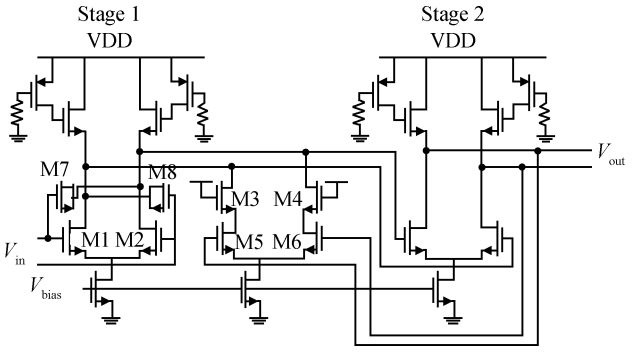

Fig. 6. Pre-driver schemes.

The gain unit using an active inductor as the load also has the feature to withstand PVT (process, voltage and temperature) changes. The ±30% R_{g} floating can only cause the gain change less than 0.35 dB[4]. Moreover, the current gain mainly depends on the ratio of the geometric factors of the MOS tubes and is insensitive to the changes in process, temperature and bias. Therefore, its anti-PVT-change performance is significantly better than the PMOS active resistor load and the polycrystalline resistor load.

In order to further improve the circuit gain bandwidth, in addition to using the active inductors, the active negative feedback was also introduced into the design. In the pre-driving circuit, as shown in Fig. 6, the M3 and M4 tubes mainly are used as the current source loads to increase the transconductance values G_{m1} and G_{m2} of the two-stage driver. The M7 and M8 tubes were introduced in the negative Miller capacitors functioning to offset the gate leakage and gate–source capacitance of the MI and M2 tubes.

The primary CML driver circuit consists of three CML single-stage drivers within the cascade structure. In order to increase the driving capability, the size of these CML drivers is increased stage by stage, forming a driver chain within the conical structure.

With the increased bandwidth of the drive, when the bit width of each bit of data (the time occupied by each bit of data) is less than the bit processing time of the driver, the value of the foregoing signal will influence the waveform of the current bit. Such interference is also called the inter-symbol interference. Inter-symbol interference is most likely to appear in the cases containing continuous “0” or “1” in the serial data. Inter-symbol interference will reduce the maximum system operation frequency[5]. However, in the pre-emphasis circuit, the circuit will intensively over-drive the signal at the signal jumping, and within any continuous same value of the signal, the speed of the jumping will be greatly increased to avoid the occurrence of continuous “0” or “1”, and thus the inter-symbol interference can be reduced[6].

In order to further expand the bandwidth and address the problems of high-speed serial transmission, such as signal high-frequency component attenuation and inter-symbol interference, we used the two-stage pre-emphasis circuit in the main

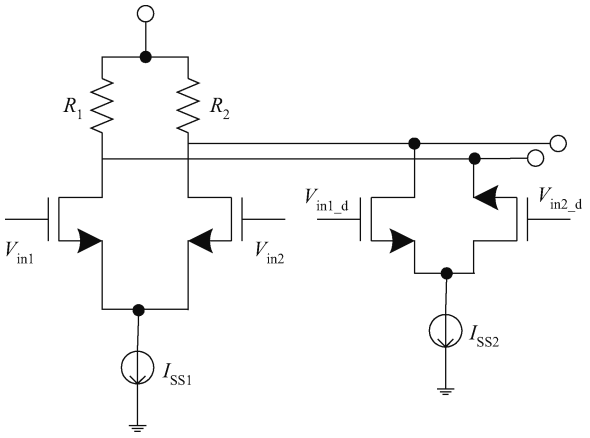

Fig. 7. A simple pre-emphasis scheme.

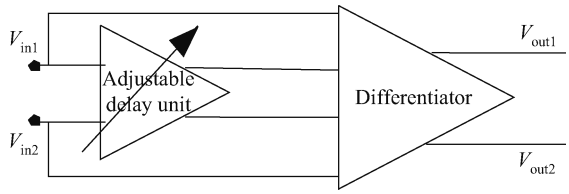

Fig. 8. Block diagram of voltage-peaking circuit.

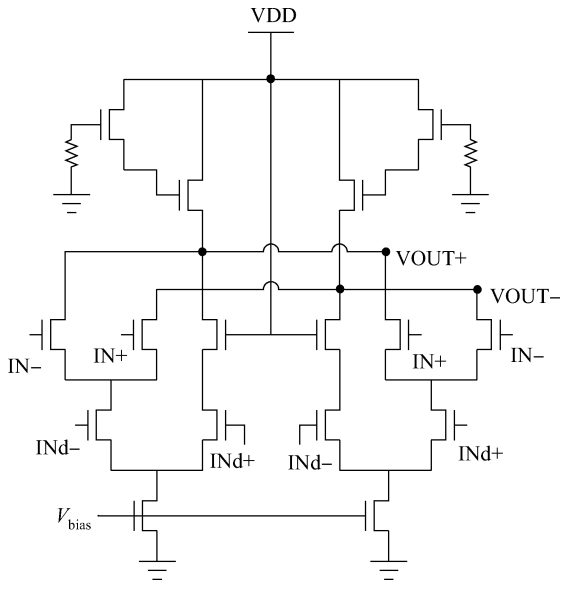

Fig. 9. Differentiator schematic.

driver. The first stage is the parallel CML BUFFER with a simple structure, as shown in Fig. 7.

The second stage is the differential pre-emphasis circuit, which superimposes a certain percentage of first-order differential waveform on the original signal waveform to obtain one high step signal at each jumping edge[7]. Subsequently, the pre-emphasis waveform can be achieved with its structure shown in Fig. 8[8].

The structure of the differential circuit is shown in Fig. 9. In this circuit, the current size of the current source controls the height of the voltage value peaks. In the design process, the active inductors were used to replace the load resistors in the traditional design and further expand the bandwidth.

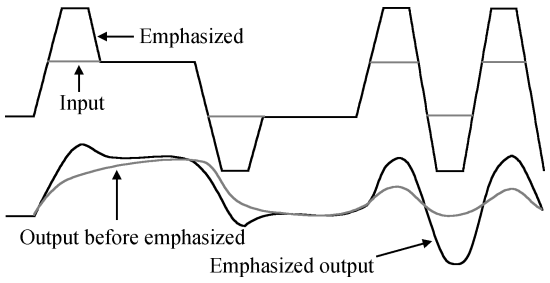

Fig. 10. Output wave contrast

The driver output waveforms, before and after using the pre-emphasis circuit, are shown in Fig. 10. From this figure, it can be seen that, after using the pre-emphasis circuit, the driver output signal generates a small peak at each jumping, effectively offsetting the signal high-frequency component.

3.2. Receiver

The receiver consists of the adaptive equalizer circuit and its auxiliary circuit module, limiting-like amplifier circuit, comparator circuit, level shift circuit and shaping output circuit. A block diagram of the receiver is shown in Fig. 11.

The equalizer circuit at the receiving terminal mainly functions to offset the loss of the high-frequency component at the receiver terminal during the transmission process. The structure of the equalizer used in the design is shown in Fig. 12[9]. This equalizer is an active time domain adaptive equalizer, mainly consisting of the feedforward path and the feedback path, where the feedforward path mainly consists of the adjustable equalization filter, slicer and the output driver; and the feedback path consists of two edge detectors and one synthesizer.

In Fig. 12, the tuned amplifier branch is a high-pass network and the flat response amplifier is a low-pass network. In the waveform superimposer, the control voltage V_{ctr} controls the weights of the two inputs. After adding them together, the Slicer restores the signal to full logic level. Then the output driver amplifies the level and transmits it to the limiting amplifier. In the feedback path, the edge detectors are responsible for detecting the transition times output by the waveform superimposer and Slicer, and sending them to the synthesizer. The control voltage, V_{ctr}, is proportional to the difference between the output of the synthesizer and the transition times, and it can adjust the adjustable equalization filter so as to control the proportion of the two branch signals from the tuned amplifier and the flat response amplifier in the transmission signal and then control the ratio of high- and low-frequency components in the signal to achieve the offsetting of the high-frequency component in the transmission signal, thereby reducing the error rate.

Figure 13 shows the circuit structures of the tuned amplifier and the flat response amplifier. From the figure, it can be seen that the circuit structure adopts the active inductor structure again to expand the bandwidth and form one branch of the high-pass filter network of the tuned amplifier.

The slicer mainly functions to restore the output of the waveform superimposer to full logic level. In order to achieve adaptive equalization and to facilitate feedback circuit sam-

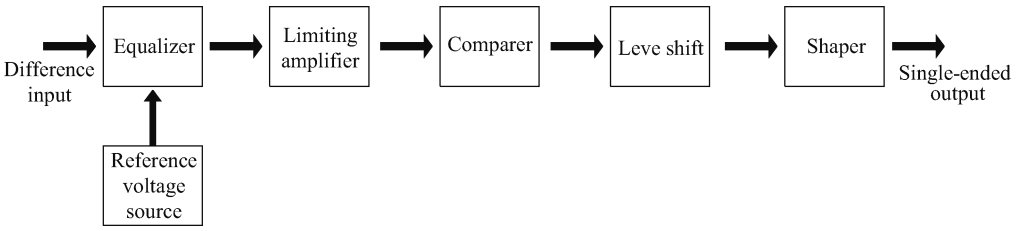

Fig. 11. Block diagram of the receiver.

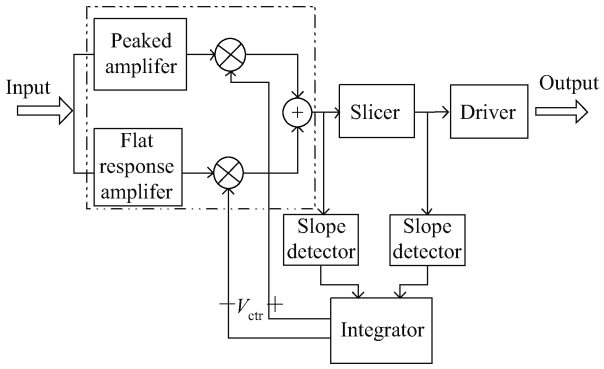

Fig. 12. Adaptive equalizer block.

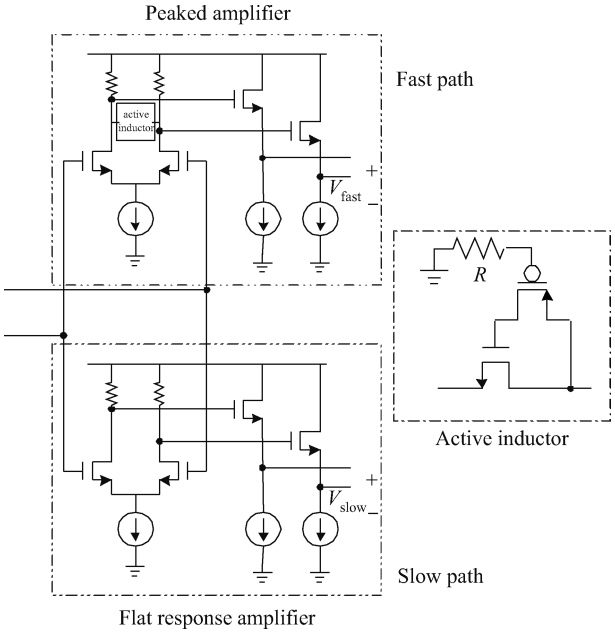

Fig. 13. Peaked amplifiers and flat response amplifier schematic.

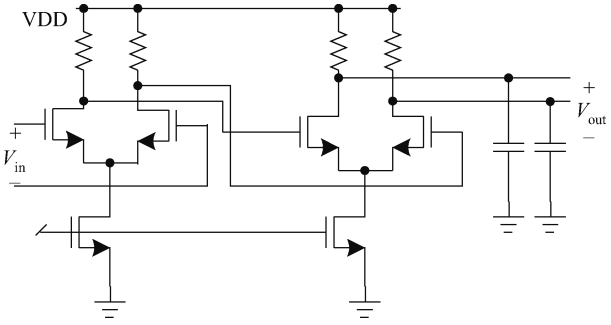

Fig. 14. Slicer schematic.

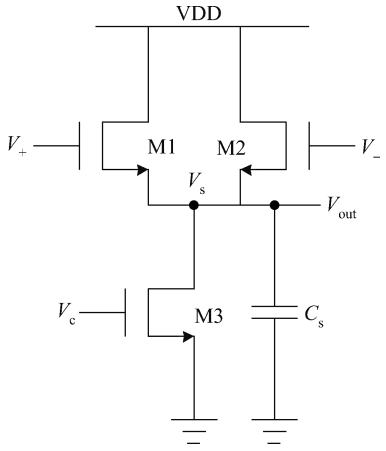

Fig. 15. Slope detector schematic.

pling, the design adopted the two-stage cascaded CML buffer with the structure shown in Fig. 14.

The equalizer feedback circuit consists of the edge detectors and the synthesizer. The edge detector functions to detect the transition times output by the adjustable equalization filter and the slicer, and its circuit performance is closely linked with the performance of the entire equalization circuit. Here we adopted a new type of edge detection circuit that has a simple structure and excellent performance, and avoids the problem of the difficulty in high frequency performance promotion for the traditional structure of high-pass filter plus rectifier. The specific structure of the circuit is shown in Fig. 15.

The principle of the circuit is as follows. When M1 and M2 work in the saturation region, due to the symmetry of the circuit differential pairs, the $W_1/L_1 = W_2/L_2 = W/L$ and it can be determined that

$$V_+ - V_- = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\dfrac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\dfrac{W}{L}}}. \tag{4}$$

Equation (3) can be developed as

$$(V_+ - V_-)^2 = \frac{2}{\mu_n C_{ox}\dfrac{W}{L}}(I_{ss} - 2\sqrt{I_{D1}I_{D2}}). \tag{5}$$

Since V_+ and V_- are symmetrical inverting input signals,V_+, V_- and $V_+ - V_-$ have the same transition situation. Thus, the principle of the edge detection circuit in Fig. 15 can be divided into the following two cases for discussion:

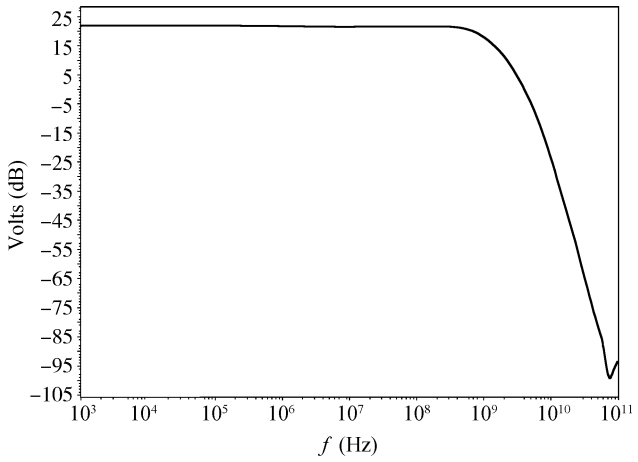

Fig. 16. Frequency responses of the equalizer.

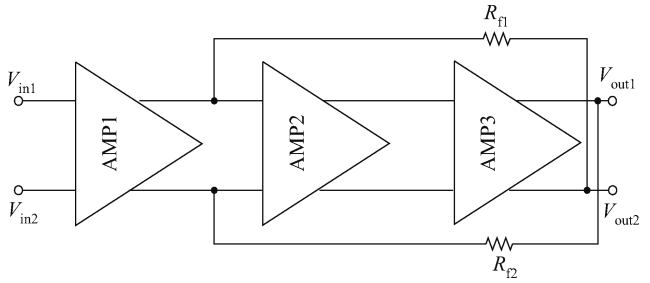

Fig. 17. The improved Cherry–Hooper schematic.

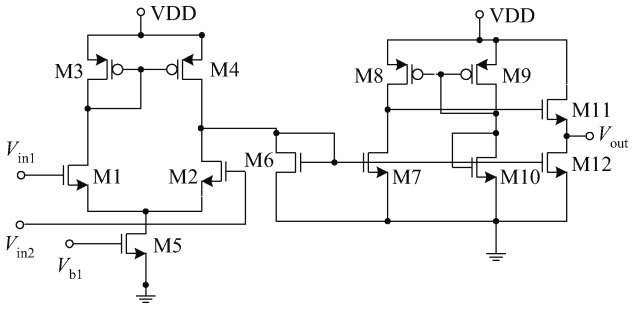

Fig. 18. The improved comparator schematic.

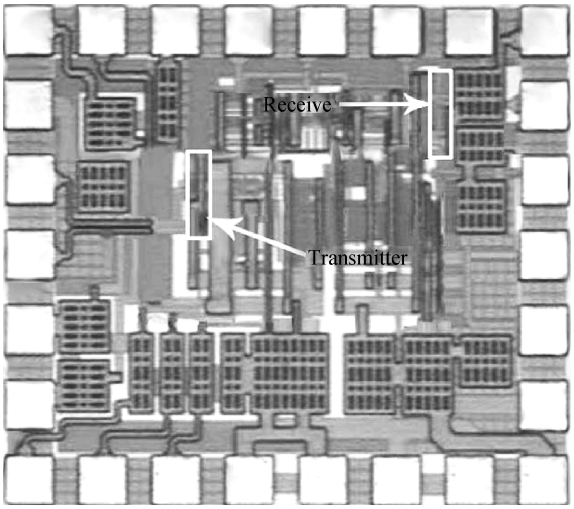

Fig. 19. Micrograph of the transceiver.

(1) Slow transition occurs in the input: because, when the differential input is 0, the source electrode coupled node voltage V_s shows a minimum value, the output response is a negative pulse for any input transition. From Eq. (4), it can be seen that the magnitude value depends on the size of the differential pair.

(2) Rapid transition occurs in the input: the reason for the generation of a negative pulse here is the same as when slow transition occurs. However, the accelerated transition results in a shorter charging time, while the charge and discharge time constants are fixed values that are in turn determined by the tube size and the capacitor capacity. Therefore, in this case, this negative pulse amplitude is smaller than when the slow transition occurs.

As can be seen from the above discussion, although this circuit is much simpler than the traditional structure, the high sampling accuracy can still be obtained as long as the transistor size and the capacitor capacity are well adjusted.

Figure 16 shows the frequency response curve of the adaptive equalizer in this design. It can be seen from the figure that the circuit's –3 dB bandwidth is 5 GHz, and thus this circuit can fully meet the working requirement at 5 Gbps.

The auxiliary circuit mainly functions to provide a reference voltage source output for the feedback module of the equalizer circuit. In order to ensure the stable voltage output of the reference voltage source circuit in cases of the variations of the process, voltage and temperature, the design of the reference voltage source adopted the bandgap reference source.

Limiting the amplifier structure further amplifies the low swing signal output by the adaptive equalizer circuit to a certain amplitude for the comparator to identify. The design adopted the improved Cherry–Hooper structure, as shown in Fig. 17[10], to form the limiting amplifier's broadband amplification unit.

The comparator functions to compare the two output signals from the limiting-like amplifier to convert the differential signal into the single-ended signal. In order to meet the requirements of the comparator response time, the design adopted the improved comparator structure, as shown in Fig. 18.

The output shaping circuit mainly functions to further adjust the signal waveform about to enter the core chip to help the duty ratio and the rise and fall times reach the requirements of the core chip on the input signal.

In this design, it was achieved by using the Schmitt trigger and several series-connected inverters.

4. Measurement results

We implement the entire PCI-E2.0 physical layer prototype chip in SMIC's 0.13 μm process. As part of the chip, the transmitter and receiver are identified in Fig. 19. They are both $40 \times 200\ \mu m^2$. The circuit power consumption of the transmitter and the receiver were 81 mW and 69 mW, respectively.

The input data-rate is 5 Gbps and as passing through the 20 cm differential transmission line with RF4 as the base material, the entire circuit worked properly under a 2 pF load capacitance. The eye pattern of the transceiver is shown in Fig. 20. It can be seen from the figure that the driver has a 350 mV output

Table 1. Design summary.

Technology	Supply (V)	Data-rate (Gb/s)	Area (mm^2)	Tx swing (mV)	Rx eye opening (mV)	Rx eye width	Power (mW)
0.13 μm CMOS	1.2	5 (single-channel)	0.016	350	135	0.56 UI (1UI = 200 ps)	150

Table 2. Performance comparison.

Parameter	Ref. [11]	Ref. [12]	Ref. [13]	This work
Technology	0.13 μm CMOS	90 nm CMOS	65 nm CMOS	0.13 μm CMOS
Supply (V)	1.2	1	1	1.2
Data-rate (Gb/s)	10	12 (PAM2)	10 (PAM2)	5
Area (mm^2)	1.584	0.23	0.13	0.016
Tx swing (mV)	300	Variable	420	350

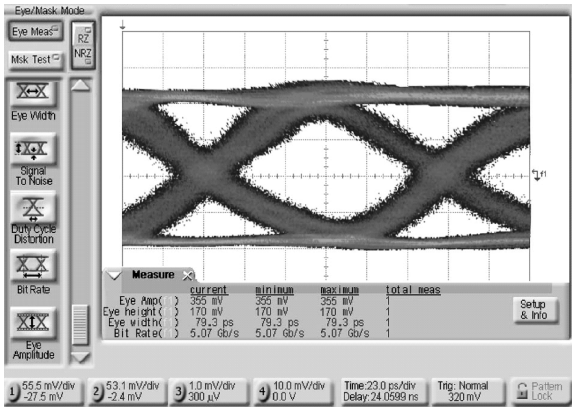

Fig. 20. TX eye pattern at 5 Gbps.

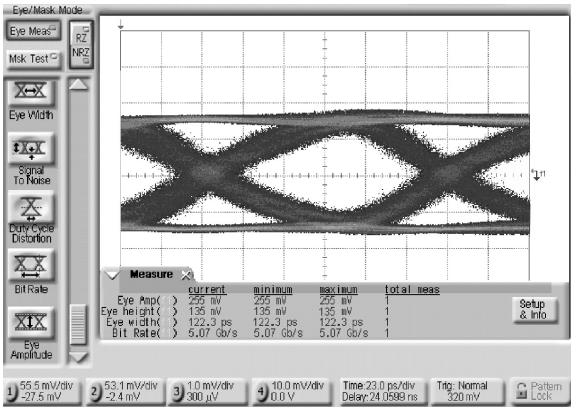

Fig. 22. Output eye pattern of the receiver.

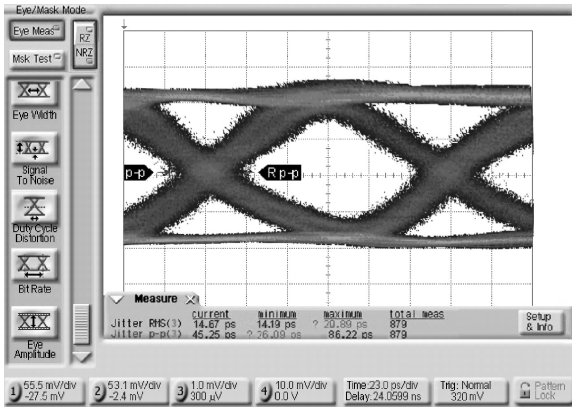

Fig. 21. Jitter performance of the transmitter at 5 Gbps.

signal swing.

The measured eye RMS jitter is 14 ps, as shown in Fig. 21.

Figure 22 shows the output eye pattern of the receiver, which input 5 Gbps PRBS data transmitted through a 20 cm PCB trace. Obviously, the eye opening amplitude is 135 mV and the eye width is 0.56 UI (1UI = 200 ps). Follow-up results show that the bit error rate of the receiver is less than 10^{-12} and fits with the PCI Express 2.0 specifications well.

Table 1 shows the performance summary of the proposed transceiver and Table 2 shows the performance comparison with other recent work. From Table 2, it can be seen that in this work, the area of the circuit is much smaller than in other work, even in a wider process width.

5. Conclusion

This paper designed and implemented a CML transmitter and receiver. The design used the 0.13 μm CMOS process and had an area of 0.016 mm^2 and a power supply voltage of 1.2 V. The result of layout post simulation showed a total power consumption of 150 mW. Under a 5 Gb/s transmission rate, it identified the differential input voltage as low as 80 mV and increased the output swing to 340 mV. The test results showed that this circuit could stably transmit the signal at a data transfer rate of 5 Gbps and sufficiently meet the PCI-Express 2.0 protocol requirements of the physical layer performance.

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