A fast transient response low dropout regulator with current control methodology*

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Abstract: A transient performance optimized CCL-LDO regulator is proposed. In the CCL-LDO, the control method of the charge pump phase-locked loop is adopted. A current control loop has the feedback signal and reference current to be compared, and then a loop filter generates the gate voltage of the power MOSFET by integrating the error current. The CCL-LDO has the optimized damping coefficient and natural resonant frequency, while its output voltage can be sub-1-V and is not restricted by the reference voltage. With a 1 μF decoupling capacitor, the experimental results based on a 0.13 μm CMOS process show that the output voltage is 1.0 V; when the workload changes from 100 μA to 100 mA transiently, the stable dropout is 4.25 mV, the settling time is 8.2 μs and the undershoot is 5.11 mV; when the workload changes from 100 mA to 100 μA transiently, the stable dropout is 4.25 mV, the settling time is 23.3 μs and the overshoot is 6.21 mV. The PSRR value is more than -95 dB. Most of the attributes of the CCL-LDO are improved rapidly with a FOM value of 0.0097.

Key words: current control loop; transient response; LDO; damping coefficient; natural resonant frequency
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1. Introduction

The power integrated circuit (IC) is an indispensable element in modern electronic systems in which the low-dropout regulator (LDO) is widely used. A typical structure of the LDO is shown in Fig. 1(a)[1−4], which is a definitely classical second-order loop. Figure 1(b) shows the transform model. The output waveform is presented in Fig. 1(c) when the workload changes transiently.

The transient response is a major property of LDO to its applications, although other performances of it are also basilic. But in fact, the loop's time-constant is very large because of the huge gate capacitor of a massive power MOSFET. It is said that the gate capacitor of a 10000 μm-wide MOS can reach more than 50 pF in a 0.35 μm CMOS process[1]. In a typical LDO, the control loop changes the gate voltage of the power MOSFET to maintain the output voltage only if the workload increases. But when the workload decreases, the settling process depends on the workload itself. By this issue, the transient response of the typical LDO presented in Fig. 1 is inefficient. On the other hand, the reference voltage in a normal LDO is delivered from a bandgap voltage reference. The normal reference voltage is 1.23 V, which means that the sub-1-V output is produced discommodiously[5].

Lots of ways are employed to improve the transient performance of LDOs, including reducing the time constant of the loop, optimizing the damping coefficient and natural resonant frequency, and establishing additional charging/discharging paths to accelerate the settling period. Heng[1] implemented a discharging path on the gate of the power MOSFET, by which the single-side time constant is reduced. Meanwhile, a charging path was implemented additionally, so that the gate voltage of the power MOSFET changed rapidly on both sides[2]. Lim[6] set up a special current path that was shunt-wound to the workload, by which the discharging was speeded up at the output end.

All of those accelerations are the appendices of a typical LDO. As a novel structure, like the control methodology of a charge pump phase-locked loop (PLL)[7], an LDO with a current control loop (CCL-LDO) is proposed in this article. In the CCL-LDO, the driving ability of the error amplifier (EA) is enhanced. The output voltage is not restricted by a classical reference and can be sub-1-V. Both manual analysis and verification by Hspice^{TM} show that the transient performance of the CCL-LDO is extraordinarily excellent.

2. Structure and circuit of CCL-LDO

Generally, the transient performance of current signals is faster than that of voltage signals, and it also has stronger interference immunity. Therefore, the transient performance is better in the current second-order loop.

The conceptual structure of the proposed CCL-LDO is illustrated in Fig. 2, which adopts the control method of a charge pump PLL. Compared with the classical structure in Fig. 1(a), there is no resistor network but a voltage buffer (BUF) adopted, by which the output voltage is sampled, and an OTA generates the control current instead of the operational amplifier (OP). Then, this current is integrated to voltage by the capacitor C_s, which is connected to the gate of the power MOSFET. Several advantages can be concluded, as follows:

(1) The feedback signal is the true voltage of the output and is not restricted by the 1.23 V bandgap reference, so that the sub-1-V output can be generated easily.

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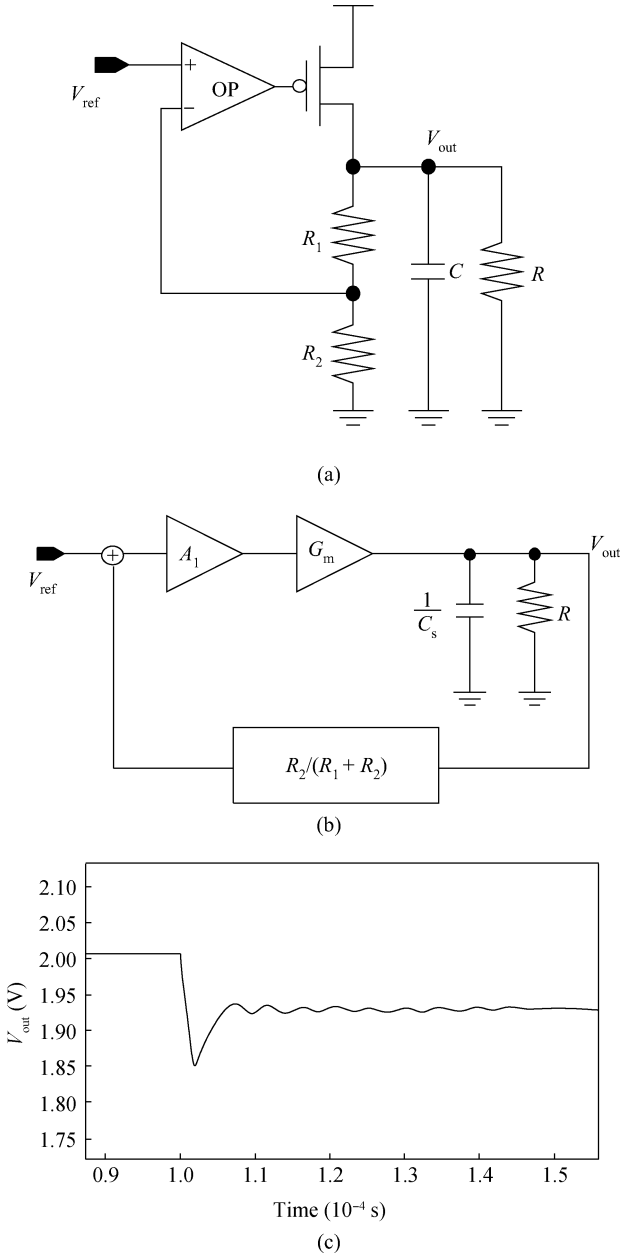

Fig. 1. (a) Structure, (b) transform model, and (c) transient response of a classical LDO.

(2) Because the reference signal of the OTA is current I_{ref}, the precision of control is extremely high.

(3) The gate capacitor of the power MOSFET is driven by the output current of the OTA, so that the transient response of the loop is faster than in classical LDOs.

The detailed circuit of the proposed CCL-LDO in this article is illustrated in Fig. 3. The left portion is the voltage buffer mentioned above, which consists of an OP, and resistors R_0 and R_1. With this BUF, the output voltage signal has been delivered to the OTA, which is another important portion in that circuit and consists of source followers M0 and M9/M10, and current mirrors M1–M4 and M5–M8. The OTA converts the sampling signal V_S into current and generates the error current against the reference signal, I_{ref}. The gate voltage of the power MOSFET M11, V_A, is generated by the capacitor C_{int2}, which integrates the error current. A convenient issue is that there is

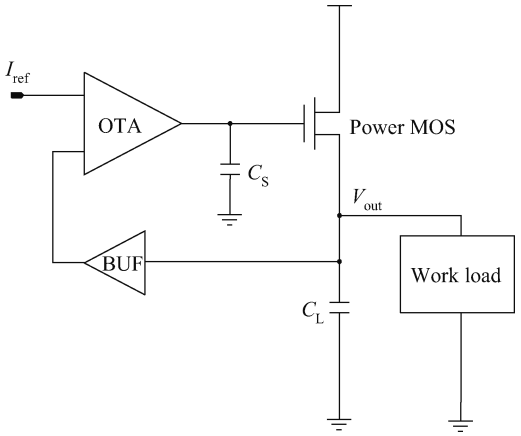

Fig. 2. Structure of the proposed CCL-LDO.

no need to establish an individual capacitor C_{int2} but one can use the gate capacitor of M11 instead, because the dimension of the power MOSFET M11 is wide enough. The same is true with C_{int1}, which is implemented with the gate capacitor of M9. And, by the utilization of those two capacitors, the first polar frequency of the OTA is also increased.

Provided that the current gain of the cascode current mirror is K, the current mirror consists of transistors M1–M4. Equation (1) can be matched when the loop is stable, in which V_C tightly associates with the transconductance of M0.

$$\frac{1}{2}\mu_n C_{ox}\frac{W_0}{L_0}\left(\frac{R_1+R_0}{R_1}V_{out}-V_C\right)K=I_{ref}. \tag{1}$$

3. Transform model of the loop

A CCL-LDO can be extracted and is shown in Fig. 4 as a second-order closed loop model. With this model, the closed loop transform function of the CCL-LDO formed as follows, where A_1 is the gain of the BUF, G_m is the transconductance of the OTA, C_{int2} is the integrating capacitor, g_m is the transconductance of the power MOSFET, g_{mb} is the equivalent transconductance with a block effect of the power MOSFET, C_L is the decoupling capacitor, and R_L is the workload.

The open loop transform function of the CCL-LDO is expressed in Eq. (2), with high-order effects of MOS being considered.

$$G(s)=A_1G_m\frac{1}{C_{int2}s}\frac{g_mR^*}{1+(g_m+g_{mb})R^*}, \tag{2}$$

in which $R^*=R_L//\frac{1}{C_Ls}=\frac{R_L}{1+R_LC_Ls}$.

Therefore, the closed loop transform function of the CCL-LDO is expressed in Eq. (3).

$$\begin{aligned}H(s)&=\frac{G(s)}{1+G(s)}\\&=\frac{A_1G_mg_mR^*}{C_{int2}s[1+(g_m+g_{mb})R^*]+A_1G_mg_mR^*}.\end{aligned} \tag{3}$$

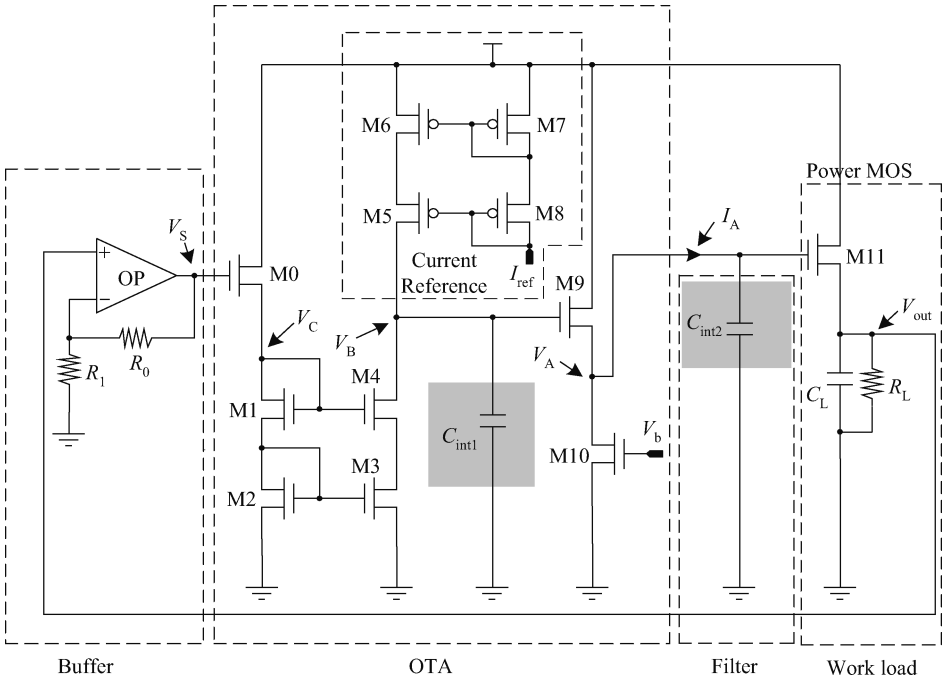

Fig. 3. Circuit of the proposed CCL-LDO.

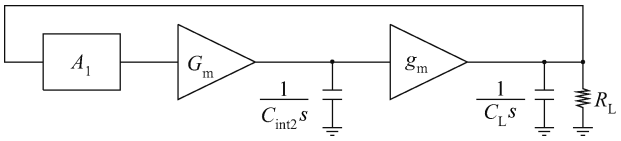

Fig. 4. Transform function of the proposed CCL-LDO.

With R^* deployed, an expression of $H(s)$ is shown in Eq. (4),

$$H(s)=\frac{A_1G_mg_m\dfrac{R_L}{1+R_LC_Ls}}{C_{int2}s\left[1+\dfrac{(g_m+g_{mb})R_L}{1+R_LC_Ls}\right]+A_1G_mg_m\dfrac{R_L}{1+R_LC_Ls}}$$
$$=\frac{A_1G_mg_mR_L}{R_LC_LC_{int2}s^2+[1+(g_m+g_{mb})R_L]C_{int2}s+A_1G_mg_mR_L}. \quad (4)$$

Obviously, $H(s)$ presents the standard format of a second-order closed loop control system. With the empirical formula in Eq. (5), the natural resonant frequency ω_n and damping coefficient ζ can be calculated, and the expressions are shown in Eqs. (6) and (7), respectively, in which η is the block effect coefficient.

$$g_m+g_{mb}\cong(1+\eta)g_m, \quad (5)$$

$$\omega_n=\sqrt{\frac{A_1G_mg_m}{C_LC_{int2}}}, \quad (6)$$

$$\zeta=\frac{1+(1+\eta)g_mR_L}{2R_L}\sqrt{\frac{C_{int2}}{A_1G_mg_mC_L}}. \quad (7)$$

The transient response of a second-order closed loop is determined by ω_n and ζ. Generally, the loop is overdamping

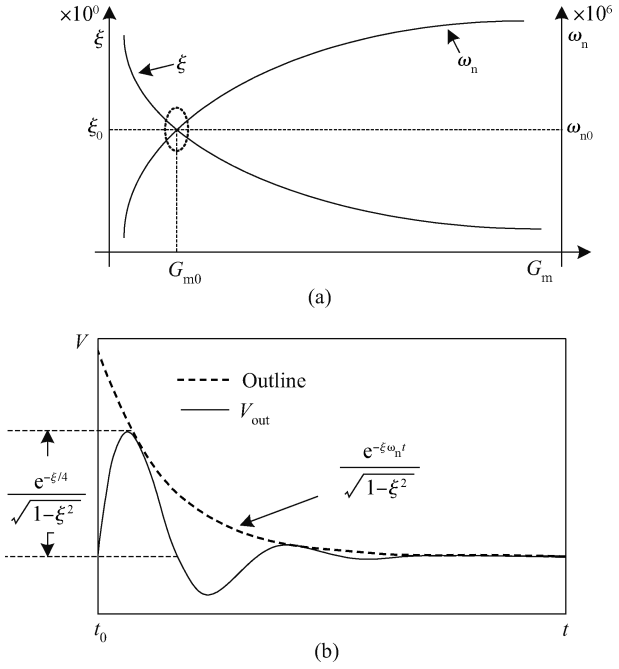

Fig. 5. Correlations between [ζ, ω_n, G_m] and transient response in underdamping state.

when ζ is bigger than 1, and there is no overshoot or undershoot. However, the settling time is too long to be accepted[6]. Therefore, an optimized loop should be set up in an appropriate underdamping state and when the parameter ζ is less than 1, thus the transient response can be rapid enough and no oscillating will occur. According to the above analysis, ω_n and ζ are determined by both the transconductance of the OTA and the gain of the BUF, once the decoupling capacitor, workload and dimension of power MOSFET are determined. But the

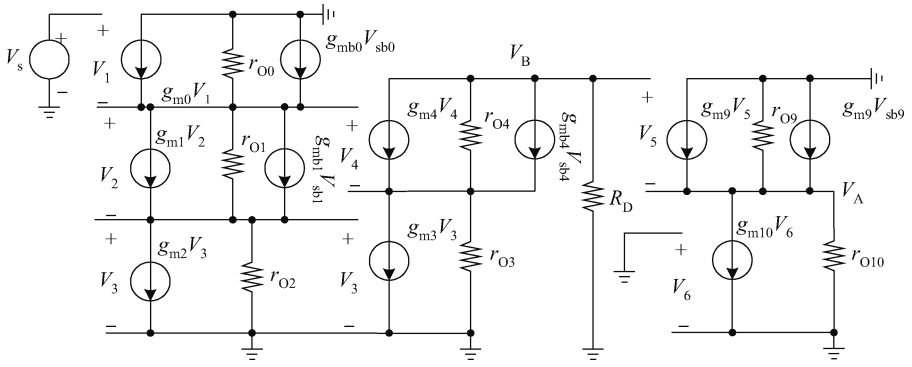

Fig. 6. Small signal model of OTA.

gain of the BUF is tightly correlative with the current reference $I_{\rm ref}$, so there is not enough adjustable range for A_1 because of the constraint of low power. Accordingly, it is a valid method to change the loop performance by adjusting the transconductance $G_{\rm m}$.

The quick transient response generally means that a short settling time can be reached with the minimum of overshoot/undershoot. The correlations among ζ, $\omega_{\rm n}$ and $G_{\rm m}$ are shown in Fig. 5(a) based on Eqs. (6) and (7). A curve of second-order output is illustrated in Fig. 5(b) when it is underdamping, and the envelope curve is illustrated in the same figure too. The function of the envelope curve is expressed in Eq. (9), while the peak overshoot $\Delta V_{\rm max}$ at the time of $1/(4\omega_{\rm n})$ is expressed in Eq. (8).

$$\Delta V_{\rm max} = {\rm e}^{-\zeta/4}/\sqrt{1-\zeta^2}, \tag{8}$$

$$V_{\rm outline} = {\rm e}^{-\zeta\omega_{\rm n}t}/\sqrt{1-\zeta^2}. \tag{9}$$

Obviously, the overshoot/undershoot is determined only by ζ. According to Eqs. (6) and (7), the value of $\zeta\omega_{\rm n}$ is a constant when the peripheral elements are decided. In order to improve the transient performance of the loop, large $\omega_{\rm n}$ and ζ are both required to achieve a status of underdamping. But as shown in Fig. 5(a), $\omega_{\rm n}$ and ζ have different trends as $G_{\rm m}$ increases, and the cross point of the two curves is the ultimate point of the loop's performance. A noticeable option is that ζ of an underdamping loop is smaller than 1 and $\omega_{\rm n}$ is measured in megahertz in general, which means that the order of magnitude of $\omega_{\rm n}$ is far greater than that of ζ, and the curves in Fig. 5(a) are the results of normalization. The point $[G_{\rm m0}, \zeta_0, \omega_{\rm n0}]$ is the ultimate point, and the optimal solution of $G_{\rm m}$ is expressed in Eq. (11).

$$\begin{aligned}\zeta_0 \cdot 10^6 = \omega_{\rm n0} &= 10^6 \frac{1+(1+\eta)g_{\rm m}R_{\rm L}}{2R_{\rm L}}\sqrt{\frac{A_1 C_{\rm int2}}{G_{\rm m0}g_{\rm m}C_{\rm L}}} \\ &= \sqrt{\frac{A_1 G_{\rm m0} g_{\rm m}}{C_{\rm L}C_{\rm int2}}},\end{aligned} \tag{10}$$

$$G_{\rm m0} = \frac{1+(1+\eta)g_{\rm m}R_{\rm L}}{2A_1R_{\rm L}g_{\rm m}}C_{\rm int2}\times 10^6. \tag{11}$$

4. Optimal solution of OTA

According to the analysis above, the cross point $[G_{\rm m0}, \zeta_0, \omega_{\rm n0}]$ is the ultimate point of transient performance of the loop, and $G_{\rm m}$ is a key parameter. In order to get the detailed physical attributes of every transistor, the analysis of a small signal model of the OTA is required. Provided that $g_{\rm mx}$ is the transconductance of every transistor, and $g_{\rm mbx}$ is the corresponding equivalent transconductance of the block effect, $r_{\rm Ox}$ is the output resistor of each transistor, and a small signal model of the OTA is shown in Fig. 6, in which $R_{\rm D}$ is equal to the sum of $r_{\rm O6}$ and $r_{\rm O5}$.

According to the small signal model, the transconductance $G_{\rm m}$ of the OTA is expressed as

$$G_{\rm m} = -\frac{\kappa_3 R_{\rm D}(g_{\rm m3}r_{\rm O3}+1+\kappa_1-\kappa_4)}{(1+\kappa_3)(1+\kappa_1+\kappa_2)r_{\rm O3}r_{\rm O10}}, \tag{12}$$

in which,

$$\kappa_1 = \frac{g_{\rm m2}+r_{\rm O2}^{-1}+g_{\rm mb1}}{g_{\rm m1}+r_{\rm O1}^{-1}}, \quad \kappa_3 = \frac{g_{\rm m9}}{g_{\rm mb9}+r_{\rm O9}^{-1}+r_{\rm O10}^{-1}},$$

$$\begin{aligned}\kappa_2 = {} & \{(g_{\rm mb0}+r_{\rm O0}^{-1})[g_{\rm m2}+r_{\rm O2}^{-1}+(1+\eta)g_{\rm m1}+r_{\rm O1}^{-1}] \\ & +(g_{\rm m1}+r_{\rm O1}^{-1})(g_{\rm m2}+r_{\rm O2}^{-1})\} / \left[g_{\rm m0}(g_{\rm m1}+r_{\rm O1}^{-1})\right],\end{aligned}$$

$$\begin{aligned}\kappa_4 = {} & \{(R_{\rm D}r_{\rm O4}^{-1}r_{\rm O3}^{-1}+r_{\rm O4}^{-1}+r_{\rm O3}^{-1}+g_{\rm mb4})\left[g_{\rm m2}+r_{\rm O2}^{-1}\right. \\ & \left.+(1+\eta)g_{\rm m1}+r_{\rm O1}^{-1}\right]+(R_{\rm D}r_{\rm O4}^{-1}+1)(g_{\rm m1}+r_{\rm O1}^{-1})\} \\ & \times\{\left[(1+\eta)g_{\rm m4}+R_{\rm D}r_{\rm O4}^{-1}r_{\rm O3}^{-1}+r_{\rm O4}^{-1}+r_{\rm O3}^{-1}\right] \\ & \times(g_{\rm m1}+r_{\rm O1}^{-1})\}^{-1}.\end{aligned}$$

Observing each item in Eq. (12), κ_1 and κ_2 are related to the input transistor M0 and the cascode current mirror, which determines the reference current $I_{\rm ref}$. There is not enough adjustable range of κ_1 and κ_2 because of the constraint of low power. And κ_4 cannot be adjusted much for the same reason as κ_1 and κ_2. The remainder is κ_3, which is only determined by M9 and M10, and means that the transconductance of the OTA has a wide adjustable range after the still parameters are identified.

5. Implementation and experiment

A test chip of the CCL-LDO is established based on a 0.13 μm CMOS process, of which the input voltage ranges from 3 to 5 V, the output voltage is 1.0 V, the maximum workload is over or equal to 100 mA, and the static power consumption is less or equal to 100 μW. A snapshot of the layout is shown in Fig. 7, in which the area of that chip is 140 ×

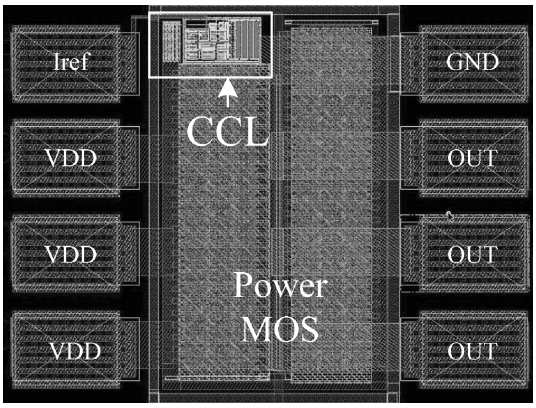

Fig. 7. Layout of the proposed CCL-LDO.

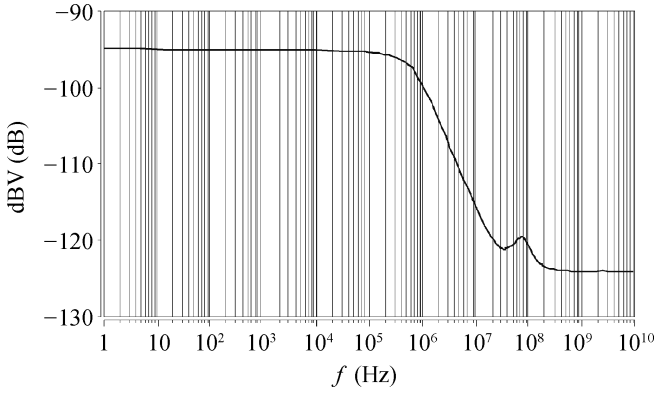

Fig. 9. PSRR of the proposed CCL-LDO.

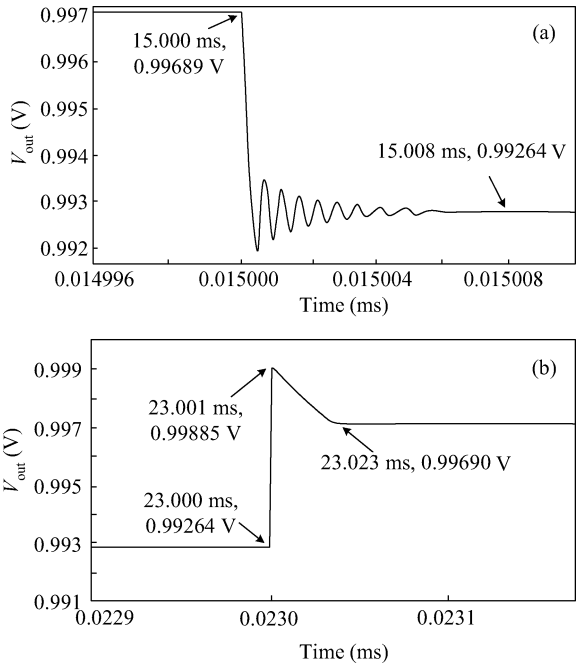

Fig. 8. Transient response of the CCL-LDO with a workload step change.

220 μm^2, with the PAD area excluded. The portion in the white rectangular box is the current control loop in Fig. 7.

According to the manual analysis, the requisite reference current I_{ref} is 6 μA, double voltage sampling is required, the dimension of the power MOSFET is 7000 μm/0.35 μm, and the decoupling capacitor is 1 μF. The post-layout simulation results are illustrated in Fig. 8, and these are based on the golden simulation tool Hspice^{TM}. In Fig. 8(a), the workload changes at the ratio of +60 dB from 100 μA to 100 mA transiently. The dropout is only 4.25 mV, the peak undershoot is 5.11 mV, and the settling time is 8.2 μs. On the other side, in Fig. 8(b), the workload changes at a ratio of −60 dB from 100 mA to 100 μA transiently. The dropout is also 4.25 mV, the peak overshoot is 6.21 mV, and the settling time is 23.2 μs. The static power consumption is only 80 μW when I_{ref} is 6 μA. All of the data show that the transient performance of the CCL-LDO is excellent.

Another significant performance of the LDO is power supply rejection (PSR)[8, 9]. In the circuit presented in Fig. 3, multiple cascode current mirrors enhance the PSR performance of the CCL-LDO. The curve of the power supply rejection ratio (PSRR) to frequency is shown in Fig. 9. In the band lower than 1 MHz, the PSRR value of the CCL-LDO is approximately −95 dB, and in the high band, the PSRR value of the CCL-LDO is beyond −120 dB. According to these data, the PSR performance of the CCL-LDO is excellent, and most of the noise on the power supply is filtered by the CCL-LDO in the wide band.

In the circuit presented in Fig. 3, it seems that the bias voltage V_b is important to the OTA. In fact, in Eq. (12), only the output resistor r_{O10} of M10 exists in that equation. This means that the performance of CCL-LDO is not so sensitive to the bias voltage V_b. Correlations between loop performance and bias voltage are shown in Fig. 10, while the range of V_b is 0.9 ± 0.05 V and the dynamic indices are the workload steps +60 dB (100 μA → 100 mA) and −60 dB (100 mA → 100 μA) separately.

The relationship between the dropout voltage and the bias voltage is shown in Fig. 10(a): the change in dropout is less than 0.5 mV in the full range of V_b when the workload increases, and less than 0.1 mV when the workload decreases. The curve of the overshoot/undershoot to V_b is shown in Fig. 10(b): the change in the overshoot is less than 2.8 mV in the full range, and less than 0.7 mV for the undershoot. The correlation between the settling time and bias voltage is shown in Fig. 10(c): the change in settling time is less than 7 μs in the full range of V_b when the workload increases, and less than 25 μs when the workload decreases. The curve of the output voltage to the bias voltage is illustrated in Fig. 10(d): there is almost no change in the output voltage in the full range of V_b.

Generally, Figure 10 shows that the bias voltage does not affect the output voltage, and it has very little impact on the overshoot, undershoot or dropout; even the change in the settling time is in an acceptable range. Because there is no strict constraint on bias voltage in the CCL-LDO, the precise reference voltage generator is not critical. Thus, the area and power consumption of the loop are also reduced.

The classical evaluating index, figure of merit (FOM), is expressed in Eq. (13), in which C_L is the decoupling capacitor, ΔV_{out} is the overshoot, I_{SS} is the static current, and $I_{out(max)}$ is the maximum output current. The FOM of the CCL-LDO

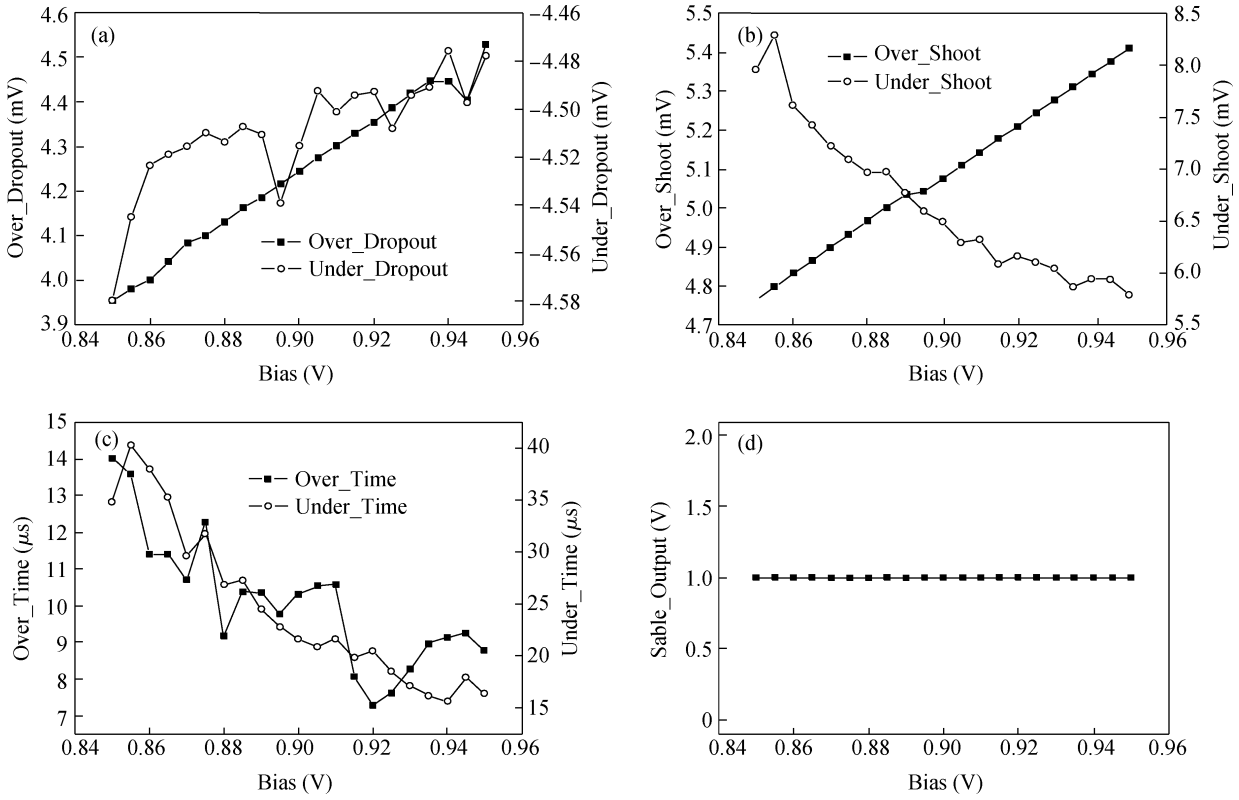

Fig. 10. CCL-LDO performance versus V_b.

Table 1. Comparison between CCL-LDO and former work.

Parameter	Ref. [2]	Ref. [10]	Ref. [9]	This work
Process (μm)	0.18	0.35	0.13	0.13
De-capacitor (μF)	4.7	1	1	1
ESR (mΩ)	No	No	No	No
V_{out} (V)	1.2	0.9	1.0	1.0
$Power_{int}$ (μW)	22	N/A	$\geqslant$ 57.5	80
PSRR (dB)	–61.8	> -50	> -56	$\geqslant -95$
Overshoot (mV)	116	6.6	15	5.11
Undershoot (mV)	104	6.6	10	6.21
Settling time O (μs)	65	0.5	0.01	8.2
Settling time U (μs)	45	0.5	0.01	23.2
FOM (ns)	0.073	0.0106	0.096	0.0097

proposed in this article is 0.0097 ns.

$$\text{FOM} = \frac{C_L \Delta V_{out} I_{SS}}{I^2_{out(max)}}. \quad (13)$$

A comparison between this work and former work is made in Table 1.

According to Table 1, the CCL-LDO proposed in this article is much better than former work in most aspects, which has the best FOM index. Notice that the dynamic range of I_{out} in Ref. [10] is within 50 mA, and that in Ref. [9] is within 25 mA.

6. Conclusion

There are extremely comprehensive applications of LDOs in electronic systems, but the transient performance of the classical LDO is really limited. In this article, a current control loop is established, which is very similar to the control method in the charge pump PLL. While the CCL-LDO has very good transient performance, its output voltage is not restricted by a voltage reference. Experimental results based on a 0.13 μm CMOS process show that the output voltage is 1.0 V, the maximum output current is over or equal to 100 mA, and the static power consumption is less or equal to 66 μW. For dynamic performance, when the workload current steps from 100 μA to 100 mA transiently, the dropout becomes 4.25 mV, the peak undershoot is 5.11 mV, and the settling time is 8.2 μs. In contrast, when the workload current steps from 100 mA to 100 μA, the dropout is also 4.25 mV, the peak overshoot is 6.21 mV and the settling time is 23.2 μs.

Compared with former work, the transient response of the CCL-LDO proposed in this article is extremely fast, and it has good performance in most aspects with a FOM index of 0.0097.

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