A 5 GHz CMOS frequency synthesizer with novel phase-switching prescaler and high-Q LC-VCO*

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Abstract: A phase-locked loop (PLL) frequency synthesizer with a novel phase-switching prescaler and a high-Q LC voltage controlled oscillator (VCO) is presented. The phase-switching prescaler with a novel modulus control mechanism is much more robust on process variations. The Q factor of the inductor, I-MOS capacitors and varactors in the VCO are optimized. The proposed frequency synthesizer was fabricated by SMIC 0.13 μm 1P8M MMRF CMOS technology with a chip area of 1150 × 2500 μm^2. When locking at 5 GHz, the current consumption is 15 mA from a supply voltage of 1.2 V and the measured phase noise at a 1 MHz offset is –122.45 dBc/Hz.

Key words: PLL frequency synthesizer; differential voltage controlled oscillator; phase-switching prescaler; CMOS

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1. Introduction

CMOS frequency synthesizers are widely used in modern RF transceivers. The purity of a local oscillating (LO) signal generated by a frequency synthesizer affects the transceiver's performance. The phase noise of the frequency synthesizer degrades the spurious transmission and sensitivity performance in up- and down-conversion. It is very important and challenging to design low noise frequency synthesizers in modern CMOS processes because the lower supply voltage limits the swing of the LO signal. Furthermore, the active components are noisier, especially in high-frequency applications. When applied in battery supplied systems, there are always power consumption limitations. It is much more difficult to generate LO signals with the desired signal-to-noise-ratio (SNR).

In this paper, a frequency synthesizer with a novel phase-switching prescaler and high-Q LC voltage controlled oscillator (LC-VCO) is presented. The system architecture of the proposed frequency synthesizer is introduced. The system parameters are determined by taking noise into consideration. Also, the important building blocks, including the novel phase-switching prescaler and high-Q LC-VCO, are introduced. Design consideration and optimization are presented.

2. System consideration

The system parameters are determined due to the application's requirements and its modules' performance. Figure 1 shows the architecture of the presented type-II 4th-order ΣΔ fractional-N PLL frequency synthesizer. There are two perfect integrators and four poles in the phase domain loop transfer function, and there is also a zero. The impedance of loop filter (LF) determines the dynamic response of the PLL. The phase margin is affected by the locations of open-loop crossover frequency (f_c), poles and the zero. The f_c is determined by the loop noise performance and the VCO noise performance to optimize the residual phase deviation performance[1]. The capacitance and resistance of passive components (C_1, C_2 and R_1) in LF can be calculated to get the maximum phase margin[1] by taking the settling time and LF chip area into consideration. The extra pole (R_3 and C_3) is added to filter away the high-pass shaped quantization noise of a MASH 1-1-1 ΣΔ modulator. With a properly placed extra pole, the output phase noise introduced by the ΣΔ modulator can be ignored with little phase margin sacrifice. Then the output phase noise at a relative frequency higher than the loop bandwidth is mainly caused by VCO. The out-of-band phase noise performance is critical in some applications with a large blocker, such as GSM.

First, the loop is broken by the switch between the charge pump (CP) and the LF, and the control signal of the VCO is

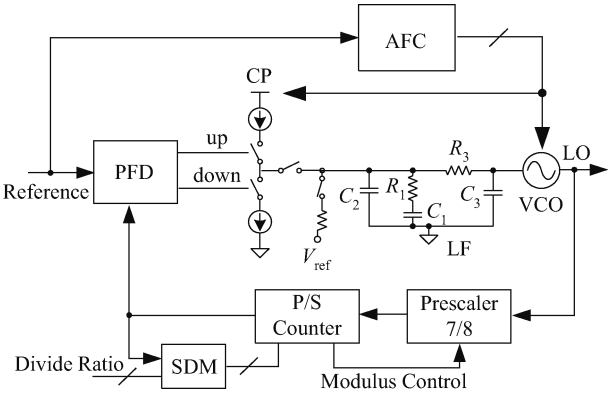

Fig. 1. Architecture of the presented PLL frequency synthesizer.

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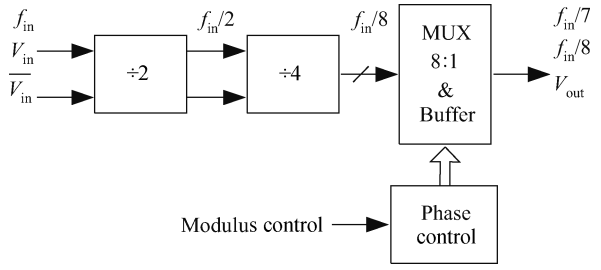

Fig. 2. Block diagram of the proposed phase-switching prescaler.

connected to the DC reference voltage (V_{ref}) when the frequency needs to be switched. And the switches of the VCO capacitor array and the CP bias current are determined as open or closed by the automatic frequency control (AFC) module according to the integer part of the division ratio. Then the loop is closed and the VCO control signal is connected to the output of the LF. The loop is locked when the frequency of the output signal is division ratio times higher than the reference's frequency and there is no average phase error between the multi-modulus divider output signal and reference.

3. Module design

3.1. Phase switching prescaler

Typically, the programmable frequency division in a frequency synthesizer is provided by a high-speed dual-modulus prescaler along with a low-speed pulse-swallow (P/S) counter. The prescaler is a high-speed frequency divider and it is the speed bottleneck of a high-frequency PLL. The speed of a traditional digital prescaler is limited by the synchronous input counter. Moreover, the traditional prescaler is usually power and area consuming[1]. The moduli of the prescaler determine the operation speed of the P/S counter and affect the range of the division ratio.

Figure 2 shows the block diagram of the novel phase-switching prescaler, which is composed of a divide-by-8 circuit, an 8 : 1 multiplexer (MUX) and a phase control module. The digital phase control module generates the select signal of the MUX. Then the proposed prescaler may work as a divide-by-7 or a divide-by-8 dual-modulus prescaler controlled by the modulus control signal. The reverse-switching technique provides glitch-free output for dual-modulus frequency division, which may be achieved by additional circuits in a conventional prescaler as Ref. [2]. The asynchronous divide-by-8 divider is composed of a divide-by-2 circuit and a divivide-by-4 circuit in serial. This frequency division topology consumes less current than the synchronous ones, and there are no misunderstandings of its output phase patterns as in Ref. [2].

The divide-by-2 circuit and divide-by-4 circuit are based on current-mode-logic (CML) flip-flops with different circuit parameters to achieve the required frequency range while saving power. The block schematic of 4 : 1 divider is the same as in Ref. [3]. The 45°-spaced output phases are generated by the divide-by-8 asynchronous divider. The 7 : 1 frequency division is achieved by changing the current output to the output with a leading phase of 45°. The operating speed is no longer limited by the CML dividers. Instead, the propagation delays in the digital logics used to switch the output phase become the critical limitations.

The phase control module chooses one out of the 8 : 1 divider's buffered outputs (P0–P7) by controlling the MUX. The modulus control signal is generated by the P/S counter. Then, the total frequency division ration in the loop is 7P+S with the prescaler working as a 7 : 1 divider in (P–S) periods and an 8 : 1 divider in the other S periods. The logic schematic of the phase control module is shown in Fig. 3. The select signals of the MUX are the outputs of eight RS flip-flops (S0–S7). There is one and only one of the select signals set to be valid when the frequency synthesizer is working. When the prescaler becomes a 7 : 1 divider, the output must be switched within 7 input periods. As shown in Fig. 4, the prescaler works as a 7 : 1 divider with its output switched from inverter-buffered P1 to P0. If MC and S1 are high voltage when P1 and P4 are high, the select signal S0 will be set. Then S1 will be reset by S0. The phase control module works a sampling system, and it samples the select signal (S0–S7) and the modulus control signal (MC) during one input signal (V_{in}) period. Timing of the phase control module is clear and accurate. The MC must be generated and valid within three periods of V_{in}, then select signals must be valid and phase switching must be done within another four periods. The former timing requirements balance the operation speed of the P/S counter and phase control module. While acting as a sampling system, the timing is solid with process variation. There is no need to add programmable delays in select signals' propagation paths as in Ref. [3].

3.2. VCO

A schematic of the differential LC-VCO is given in Fig. 5, which is a complementary VCO with cross-coupled PMOS and NMOS transistors. A tail LC-tank resonated at second harmonic is used to block the second harmonic. In the absence of tail current source, the voltage headroom is released and the noise source is reduced. The LC-tank resonator is formed by inversion mode (I-MOS) capacitors and a single turn differential inductor. The switched capacitors for sub-frequency bands are inversion mode PMOS capacitors and varactors are inversion mode NMOS capacitors. In order to program the VCO gain, the I-MOS varactors are controlled by switches. When the varactor is switched on, its equivalent capacitance is controlled through the transmission gates (M3 and M4).

When the transistor is working in inversion mode, the channel resistor of I-MOS capacitor can be calculated[4]. So the inversion channel sheet resistance $R_{ch,\square}$ can be deduced by

$$R_{ch,\square} = \frac{1}{\mu C_{ox}(|V_{GS}| - |V_T|)}, \tag{1}$$

where μ is the carrier mobility, and C_{ox} is the unit area capacitor of the gate oxide. The Q factor of the I-MOS capacitor can be expressed as[5]

$$Q = \frac{1}{\omega C R_s} = \frac{1}{\frac{\omega C_{ox}}{12}(R_{ch,\square}L^2 + R_{poly,\square}W^2)} = \frac{12}{\omega C_{ox}R_{ch,\square}L^2 + \omega C_{ox}R_{poly,\square}W^2}. \tag{2}$$

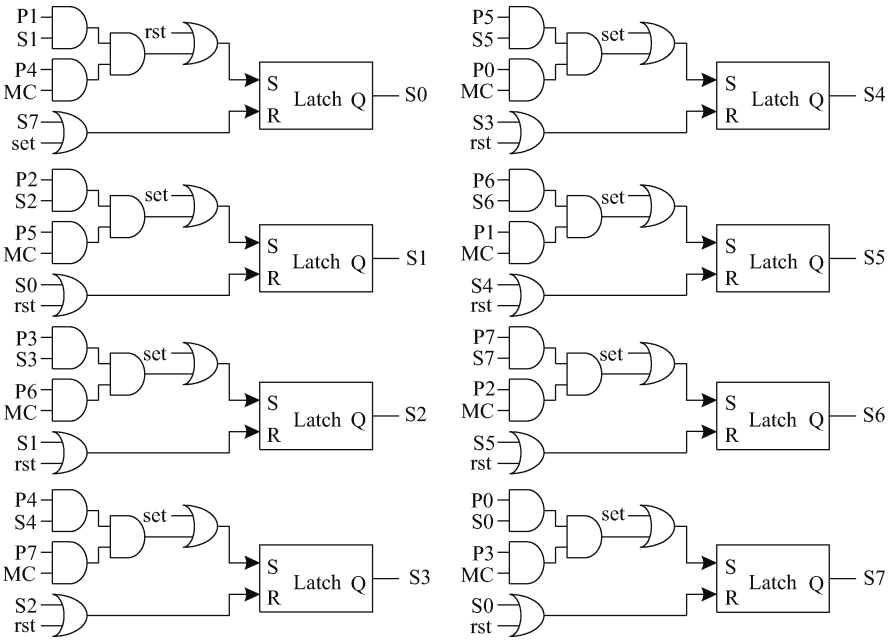

Fig. 3. Logic schematic of the phase control module.

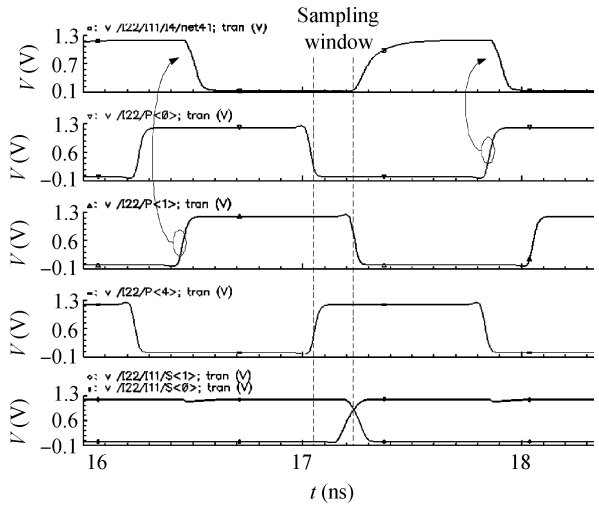

Fig. 4. Transition simulation of the prescaler's divide-by-7 operation.

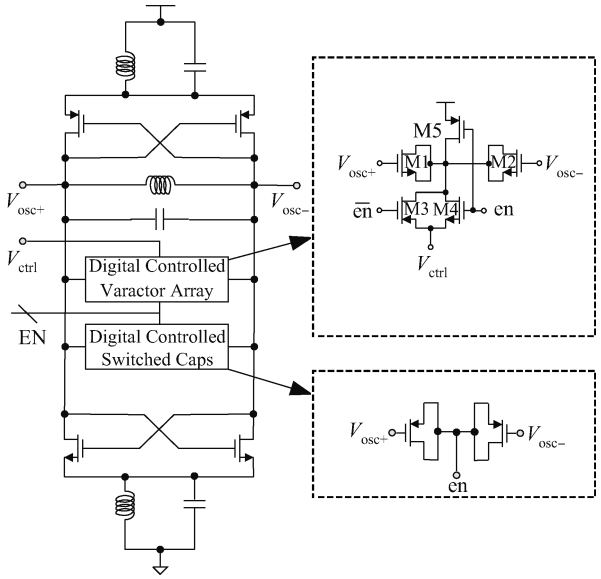

Fig. 5. Circuit diagram of high-Q LC-VCO.

In Eq. (3), $R_{poly,\square}$ is the sheet resistance of the gate, and ω is the resonation frequency. W and L are the width and length of the transistor. The channel resistor dominates the total series resistance. From Eqs. (1) and (2), the Q factor is approximate to

$$Q = \frac{12}{\omega C_{ox} R_{ch,\square} L^2} = \frac{12\mu(|V_{GS}| - |V_T|)}{\omega L^2}. \quad (3)$$

Equation (3) shows that the Q factor of the proper channel length I-MOS capacitors with sufficient overdrive voltage will be high enough at the frequency below 10 GHz, e.g., minimum length PMOS capacitors can have a Q factor higher than 100. The inversion PMOS switched capacitors sources/drains are biased at the power supply higher than the VCO supply when switched on to have sufficient overdriven voltage over the entire oscillating cycle. Additionally, the proper biased switched I-MOS capacitors suppress AM to FM noise conversion through their nonlinearity.

The varactors are implemented by native NMOS transistors. The NMOS pair (M1, M2) is the differential varactor. The varactor keeps minimum capacitance when the signal en is low. And the varactor is controlled by V_{ctrl} when the switch signal en is high. The varactor is switched ON/OFF and continuously controlled by biasing the AC ground node. When the varactor is switched ON, the resistor of the transmission gate (M3, M4) will only affect the Q factor part of the oscillating cycle because of the MOS capacitors' (M1, M2) nonlinearity.

Figure 6 shows the simulated Q factor of varactors in the proposed VCO and conventional varactors in Ref. [6]. The varators are switched on and controlled by V_{ctrl}. The width and length of the PMOS switches (M5) and transmission gates

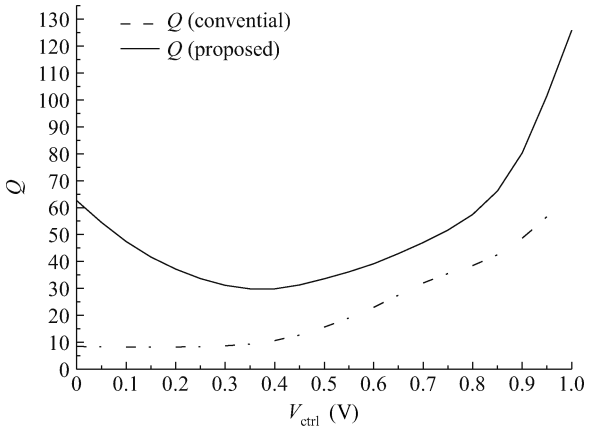

Fig. 6. Simulated Q factor of varactors.

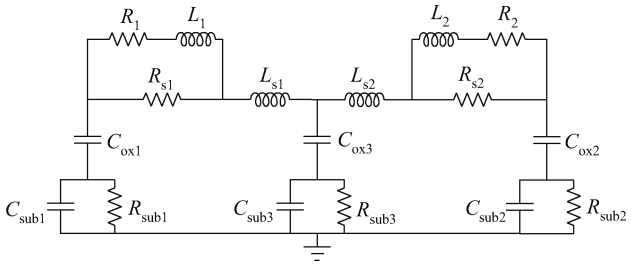

Fig. 7. Simplified double-π equivalent circuit of single turn spiral inductor.

(M3, M4) are the same in both varactors. The upper curve is the simulation Q factor of the proposed varactor versus $V_{\rm ctrl}$, and the lower is the conventional varactor's. The Q factor of the proposed varactor is several times larger than the conventional varactor's. The proposed varactor's Q factor is the minimum at about 0.35 V and increasing when $V_{\rm ctrl}$ goes up or down. When the $V_{\rm ctrl}$ is at 0 V, the I-MOS capacitors M1 and M2 are both in their maximum capacitance region and their capacitance changes little during the whole oscillating cycle. So there is almost no AC signal flow through the transmission gate (M3, M4), and its serial resistor doesn't affect the varactor's Q factor. This is the same reason that the proposed varactor's Q factor is large when the $V_{\rm ctrl}$ is higher than 1.0 V and the I-MOS capacitors M1 and M2 are both in their minimum capacitance region. The phenomenon explained before proves that the proposed circuit worked as a differential varactor and the conventional worked as a single-ended varactor.

The inductor in the parallel LC-tank resonator is a single turn spiral differential inductor. In physical analysis, the simplified double-π inductor model[7] is used as shown in Fig. 7. The series R_{si} and L_{si} ($i = 1, 2$) characterize the uniformly distributed DC current inside the conductor. The additional R_i and L_i ladder is used to capture the different current density caused by the skin effect when the frequency goes up. The substrate network can be modeled by $C_{{\rm ox}i}$, $C_{{\rm sub}i}$ and $R_{{\rm sub}i}$, with $C_{{\rm ox}i}$ representing the metal–oxide capacitance, and $C_{{\rm sub}i}$ and $R_{{\rm sub}i}$ representing the substrate capacitance and resistance, respectively. The components representing coupling capacitance between adjacent tracks and overlap capacitance between the spiral and underpass metal are negligible, because it is a single

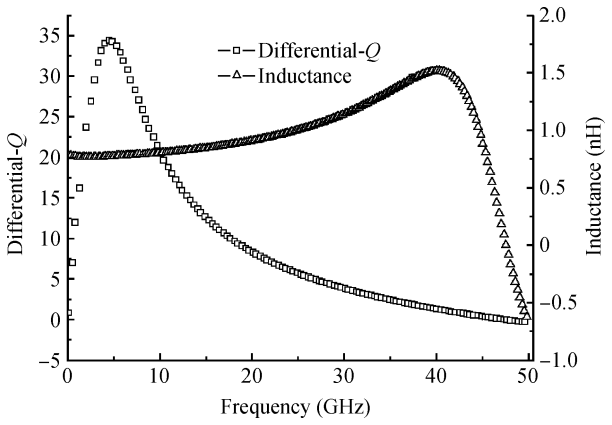

Fig. 8. Simulated Q factor and inductance of the on-chip inductor.

turn inductor without any crossover interconnections. The inductor is fully symmetrical, and then relationships of the components in the equivalent circuit are shown in Eqs. (4) and (5). The series branch partition is

$$\frac{R_1}{R_2} = \frac{R_{\rm s1}}{R_{\rm s2}} = \frac{L_1}{L_2} = \frac{L_{\rm s1}}{R_{\rm s2}} = 1. \tag{4}$$

The oxide capacitance and substrate branch partition is

$$\frac{C_{\rm ox1}}{C_{\rm ox2}} = \frac{R_{\rm sub1}}{R_{\rm sub2}} = \frac{C_{\rm sub1}}{C_{\rm sub2}} = 1. \tag{5}$$

The summation rules for the middle branch $C_{\rm ox3} = C_{\rm ox1} + C_{\rm ox2}$, $C_{\rm sub3} = C_{\rm sub1} + C_{\rm sub2}$, $1/R_{\rm sub3} = 1/R_{\rm sub1} + 1/R_{\rm sub2}$[7] will be accurate.

Single turn inductors can have superior quality factors because the ohmic loss in the top metal trace is less and the proximity effect leading Q factor degradation at high frequency is ruled out. The eddy current in the relatively high resistivity substrate (10 Ω·cm) is not the dominating substrate loss compared to the substrate ohmic losses from displacement currents conducted through turn-to-substrate capacitors, $C_{\rm oxi}$ [8]. The inductor suffers significant power dissipation mechanisms including ohmic losses in the substrate and interconnections, and the skin effect at high frequency. The skin effect loss will be reduced when the trace width increases[9], but the substrate ohmic losses will be increased under the same conditions. It will be seen directly after parameter extraction and mapping that R_i, R_{si}, $R_{{\rm sub}i}$ and L_i will decrease while $C_{{\rm ox}i}$ and $C_{{\rm sub}i}$ will increase. The inductor Q factor can be optimized by taking the tradeoff between the skin effect loss, DC ohmic loss and substrate ohmic losses into consideration. The optimized single turn differential spiral inductor has a simulated Q factor of about 35 at 6 GHz and its self resonation frequency is 48 GHz in the Agilent Momentum environment. The results are shown in Fig. 8.

4. Measurement

The proposed PLL frequency synthesizer was designed and fabricated by SMIC 0.13 μm 1P8M MMRF CMOS technology. Two single-ended RF open source on-chip output buffers are used to drive the test instrument. Figure 9 shows the micrograph of the proposed frequency synthesizer, which

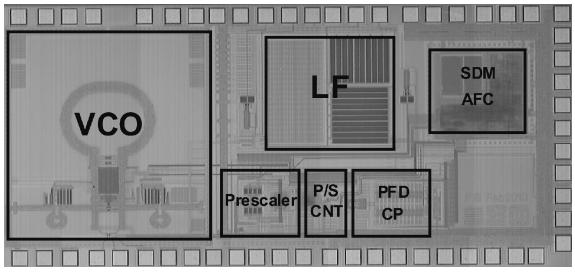

Fig. 9. Micrograph of the proposed frequency synthesizer.

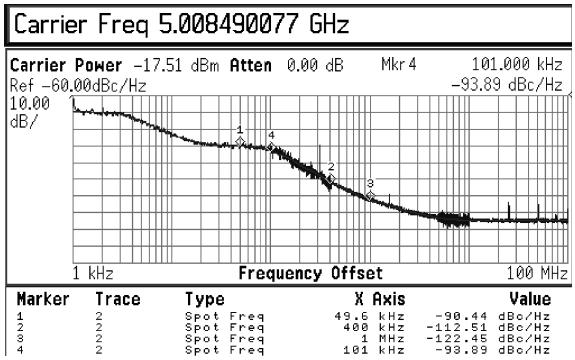

Fig. 10. Measured phase noise performance.

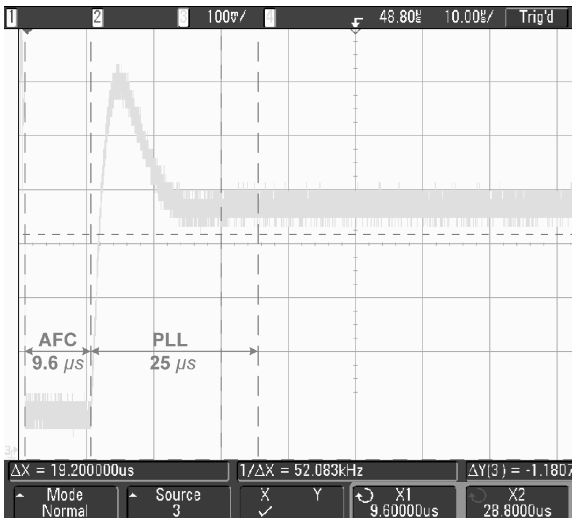

Fig. 11. Measured system settling behavior.

has a chip area of 1150×2500 μm^2, including pads. The chip is supplied by an Agilent E3631A at a voltage of 1.2 V. The phase noise of the proposed frequency synthesizer is measured by an Agilent E4440A spectrum analyzer. Figure 10 illustrates the measured phase noise at 5 GHz with current consumption of 15 mA without RF output buffers. The phase noise is –122.45 dBc/Hz at 1 MHz offset from the carrier. The measured settling behavior of the proposed frequency synthesizer is presented in Fig. 11. The AFC module takes 9.6 μs to select the capacitor array and another 25 μs is needed for phase locking. Table 1 gives the performance summary and comparison results. The proposed frequency synthesizer has better phase noise performance with comparable power dissipation. There are some reasons why the area is larger than others. The high-Q inductor is a signal turn spiral, which has a larger area than multi-turn ones with the same inductance. And the wider trace of the inductor needs a larger keep-away area, which is a far greater sacrifice of area. In order to suppress quantization noise of the $\Sigma\Delta$ modulator and not contribute to in-band phase noise, the loop filter needs more capacitance in zero and poles. So the out-band phase noise is determined by the VCO phase noise and the quantization noise isn't visible, as shown in Fig. 10. Also, a larger area is needed to isolate the noisy modules, such as the digital module and the sensitive modules. In conclusion, the area can be reduced a lot with sophisticated isolation technology and a digital module floor plan.

Table 1. Performance summary and comparison.

Parameter	Ref. [10]	Ref. [11]	Ref. [12]	This work
Freq. (GHz)	4.35–5.9	5.14–5.32	5.15–5.35	4.65–5.01
$f_{\rm ref}$ (MHz)	40	10	4	25
Tech. (μm)	0.13	0.18	0.18	0.13
Settling time (μs)	< 200	80	N/A	35
PN @ 1 MHz (dBc/Hz)	–108	–110	–104	–122
In-band PN (dBc/Hz)	–90	> -80	N/A	–90
Power (mW)	51	19.8	18	18
Area (mm^2)	0.41 (core)	1.68	1.05	2.88

5. Conclusion

The proposed frequency synthesizer with a novel phase-switching prescaler and high-Q LC-VCO has been implemented and measured. The phase-switching prescaler is a dual-modulus asynchronous divider that consumes less power, and it has a novel modulus control mechanism that is much more robust with process variation. The VCO has a parallel LC resonator constituted of I-MOS capacitors and a single turn differential inductor. The Q factor of the inductor, I-MOS capacitors and varactors are optimized. The proposed frequency synthesizer has better phase noise performance with comparable power dissipation with some area sacrifice. The chip area can be optimized significantly with sophisticated isolation technology and a digital module floor plan.

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