Gate-enclosed NMOS transistors

Fan Xue(范雪)†, Li Ping(李平), Li Wei(李威), Zhang Bin(张斌), Xie Xiaodong(谢小东), Wang Gang(王刚), Hu Bin(胡滨), and Zhai Yahong(翟亚红)

School of Microelectronics and Solid-State Electronics, State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

Abstract: In order to quantitatively compare the design cost and performance of various gate styles, NMOS transistors with two-edged, annular and ring gate layouts were designed and fabricated by a commercial 0.35 μm CMOS process. By comparing the minimum W/L ratios and transistor areas, it was found that either the annular layout or its ring counterpart incurs a higher area penalty that depends on the W/L ratio of the transistor to be designed. Furthermore, by comparing the output and transfer characteristics of the transistors and analyzing the popular existing methods for extracting the effective W/L ratio, it was shown that the mid-line approximation for annular NMOS could incur an error of more than 10%. It was also demonstrated that the foundry-provided extraction tool needs significant adaptation when being applied to the enclosed-gate transistors, since it is targeted only toward the two-edged transistor. A simple approach for rough extraction of the W/L ratio for the ring-gate NMOS was presented and its effectiveness was confirmed by the experimental results with an error up to 8%.

Key words: radiation; total ionizing dose; gate-enclosed transistor; annular NMOS; ring NMOS

DOI: 10.1088/1674-4926/32/8/084002 **EEACC:** 2220; 2550R; 2570A

1. Introduction

Complementary metal–oxide–semiconductor (CMOS) integrated circuits (ICs) are widely used in radiation-harsh environments, such as space, high-energy physics and nuclear applications. In such environments, ionizing radiation may generate holes trapped in the oxide, and the trapped holes may induce a leakage-current path from the drain to the source. In advanced CMOS technologies with thin gate oxides, the leakage paths beneath the bird's beak or the shallow trench corner become the major contributor to the total ionizing dose (TID) effect of NMOS[1−4]. A common approach to eliminate the leakage path is to adopt a gate-enclosed layout[5−8]. Nevertheless, by transforming a two-edged-gate layout into an enclosed-gate one, the performance of the circuit, such as power and speed, may be adversely affected due to parametric changes in effective and minimum W/L ratios, layout area, input capacitance, etc. Furthermore, the aforementioned changes in circuit performance also vary with process technologies and enclosed-gate styles[9−11]. Thus, in order to ensure the performance equivalency when replacing the two-edged gate by enclosed gate for radiation hardening, it is crucial to quantitatively characterize the performance of the NMOS with various gate styles and manufacturers.

In this work, gate-enclosed layout NMOS in annular and ring gate styles of various gate oxide thicknesses were designed and fabricated by a commercial 0.35 μm CMOS process. For the first time to our knowledge, we systematically characterized the transistors' minimum W/L ratios, transistor areas, and output and transfer characteristics. And our experimental results could provide guidelines for TID-hardening layout design. The commonly used approaches for extracting the effective W/L ratios of different layout styles were also quantitatively compared and selection suggestions were made in different design scenarios. A simple approach for rough extraction of the W/L ratio for the ring-gate NMOS was presented and its effectiveness was confirmed by the experimental results.

2. Experiment

2.1. Test structures

Two-edged (standard single-stripe poly), annular and ring NMOS transistors (Fig. 1) were designed and fabricated by a commercial 0.35 μm CMOS process. The gate oxide thickness (T_{ox}) of each transistor was either 11 nm or 26 nm. For ease of description, the transistors with $T_{ox} = 11$ nm are referred to as "NMOS-11" in this paper, while the others are "NMOS-26".

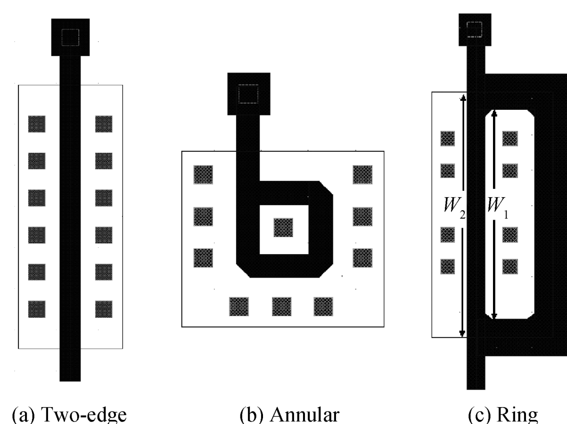


Fig. 1. Layout of NMOS transistors with (a) the regular gate and (b), (c) the radiation-hardened enclosed gates.

† Corresponding author. Email: x_fan@foxmail.com
Received 14 February 2011, revised manuscript received 17 April 2011
© 2011 Chinese Institute of Electronics

Table 1. Comparison of key geometric parameters of N-channel transistors in different gate styles.

Parameter	NMOS-11 ($L = 0.5$ μm)			NMOS-26 ($L = 2.1$ μm)		
	Two-edged	Ring	Annular	Two-edged	Ring	Annular
Minimum W/L (μm/μm)	1.0/0.5	1.25/0.5	6.0/0.5	4.2/2.1	4.2/2.1	12.4/2.1
Minimum area (μm^2)	4.8	8.7	18.2	20.7	52.1	60.9
Area for $W/L = 6$ μm/0.5 μm (μm^2)	16.3	20.3	18.2	—	—	—
Area for $W/L = 12.4$ μm/2.1 μm (μm^2)	—	—	—	52.7	102.9	60.9

The W/L ratios of the NMOS-11 and NMOS-26 transistors were approximately 6.4 μm/0.5 μm and 40 μm/2.1 μm, respectively. All of the enclosed-gate transistors were designed with the drain enclosed by the gate.

2.2. Approach for estimating minimum W/L ratio and area penalty

The minimum W/L ratio and area penalty of the enclosed-gate transistors were estimated using Virtuoso Layout Editing from Cadence, with the minimum feature size determined by the design rules of the given technology. In an enclosed-gate transistor, the gate makes turns at the corners, where the gate length (L) changes slightly due to the existence of the "corner device"[12]. Thus, L is not a constant for the transistor. In order to simplify the computation of the W/L ratio, we approximated L as the minimum distance from source to drain. To compute W, the mid-line approximation was adopted for the annular transistor, while for the ring transistor, W was approximated as $(W_1 + W_2)/2$, with W_1 and W_2 being shown in Fig. 1(c).

2.3. Experimental setup for measuring the output and transfer characteristics and effective W/L extraction

In order to extract the effective W/L ratios of the gate-enclosed NMOS transistors, the I_D of the two-edged and gate-enclosed transistors was compared. The I_D of the two-edged transistor with given W and L in layout design was used as a reference I_D. The difference between the I_D of the gate-enclosed NMOS and the reference I_D was the error of the extraction method. Five sample unbonded chips were tested through a probe tester, and each chip consisted of all of the test structures in Fig. 1. For each transistor on a chip, the I_D was measured as a function of V_G and V_D with an Agilent 4155B semiconductor parameter analyzer. In these tests, V_G and V_D ranged from 0 to 5 V, and the substrate and source of each transistor were connected to ground.

3. Results and discussion

3.1. Minimum W/L ratio and area penalty

Table 1 lists the minimum W/L ratios as L is minimum, minimum transistor areas and effective transistor areas for given W/L ratios of the tested NMOS transistors in various gate styles. The minimum W/L ratios of the gate-enclosed NMOS transistors are constrained by certain layout design rules, such as the uniform contact size and the minimum space between the active area and the poly gate. As shown in Table 1, the difference between the minimum W/L ratios of the annular NMOS and the two-edged NMOS increases from 3x to 6x as L decreases from 2.1 to 0.5 μm. This result is consistent with that reported in Ref. [11], where for $L = 0.13$ μm the difference is about 8x. The minimum W/L ratio for the annular NMOS can be smaller if L is drawn with a larger size, but larger L will lead to a larger transistor area. Thus, a higher area penalty has to be paid when applying the annular gate layout to improve TID-tolerance for more advanced technologies. It can be also seen from Table 1 that the minimum W/L ratios of the ring-gate transistors are nearly the same as those of the two-edged ones.

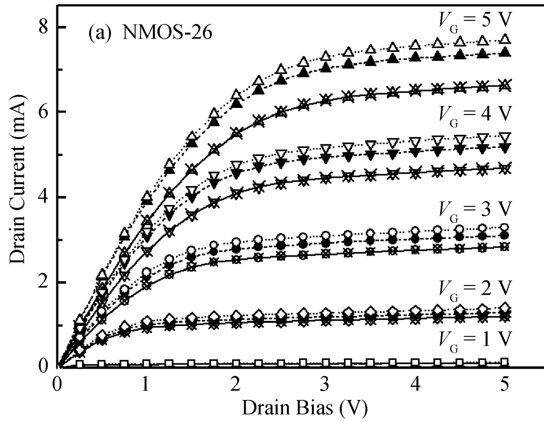
When estimating the area penalty for the enclosed-gate layout in a CMOS gate, we need to consider the sizes of both the NMOS and the PMOS. Whether the ring gate or the annular gate is a better solution for TID-tolerant design in terms of area penalty depends on the size of the transistor to be designed. When the width of the NMOS to be designed is close to its minimum size, the area penalty of the annular gate layout is larger than that of the ring gate layout due to its larger minimum W/L ratio, which also leads to larger PMOS size in order to keep the relative W/L ratios between the PMOS and the NMOS unchanged. The area penalty of the ring-gate NMOS transistors (about 2x that of the two-edged) naturally exists because the poly gate must overlap the field oxide (FOX), but the PMOS size does not have to be increased. When the width of the NMOS to be designed is as large as the minimum width of the annular layout, the size of an annular transistor is closer to its two-edged counterpart while the area penalty of the ring-gate transistor becomes non-negligible and depends on the overlapping distance between the gate and the field oxide. As a consequence, the ring transistor is superior when W/L of the transistor to be designed is close to the minimum W/L of the two-edged transistor, while the annular transistor is a better solution when the W/L of the transistor to be designed is larger than the minimum W/L of the annular transistor.

3.2. Output characteristic, transfer characteristic and effective W/L extraction

3.2.1. Characteristics and effective W/L extraction of annular transistors

The output characteristics and transfer characteristics of the annular and two-edged transistors are shown in Figs. 2 and 3. The W/L of the annular transistors were calculated by mid-line approximation, which is a commonly used W/L extraction method for annular transistors. It can be seen that the effective W/L ratio of an annular transistor is smaller than approximated by the mid-line approximation for both NMOS-26 and NMOS-11. This is consistent with the test results based on 2.5 μm, 0.5 μm and 0.25 μm CMOS processes[9, 13]. This implies that if the transistor is drawn with the mid-line approximation, the drain current I_D will be smaller than what is expected, and the difference is not negligible. For example, the I_D difference is

Closed Symbols: two-edged transistor data (W/L = 40/2.1)
Open Symbols: annular transistor N26A1 data (mid-line W/L = 45.6/2.1)
Open Symbols with crosses: annular transistor N26A2 data (mid-line W/L = 40/2.1)



Closed Symbols: two-edged transistor data (W/L = 6.4/0.5)
Open Symbols: annular transistor N11A data (mid-line W/L = 6.26/0.5)

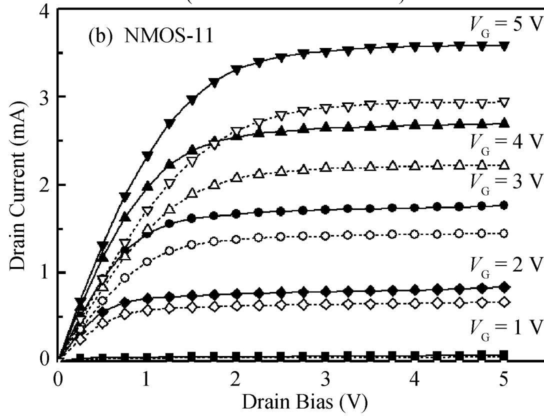
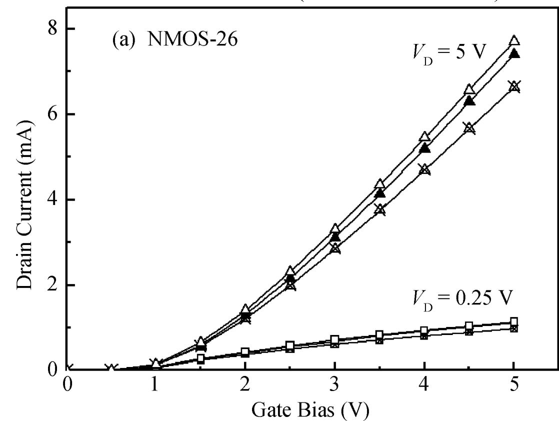


Fig. 2. Measured I_D versus V_D for annular transistors.

Closed Symbols: two-edged transistor data (W/L = 40/2.1)
Open Symbols: annular transistor N26A1 data (mid-line W/L = 45.6/2.1)
Open Symbols with crosses: annular transistor N26A2 data (mid-line W/L = 40/2.1)



Closed Symbols: two-edged transistor data (W/L = 6.4/0.5)
Open Symbols: annular transistor N11A data (mid-line W/L = 6.26/0.5)

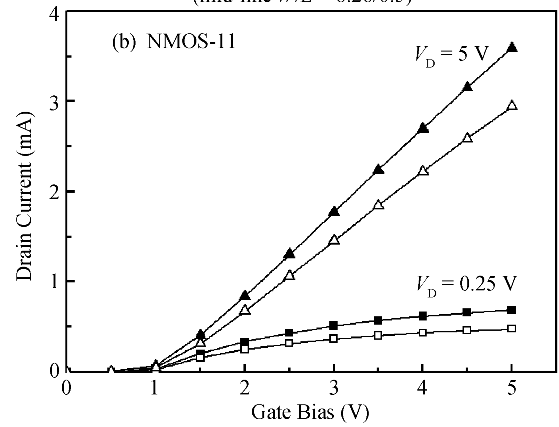


Fig. 3. The measured I_D versus V_G for annular transistors.

as large as 10.3% at the point of $V_G = 5$ V and $V_D = 5$ V for an NMOS-26 N26A2. As a matter of fact, the higher the voltage bias, the more evident the difference is. This can be explained by

$$I_{\rm Dsat} = \frac{\mu_{\rm n} C_{\rm ox}}{2} \frac{W}{L} (V_{\rm GS} - V_{\rm T0})^2. \qquad (1)$$

Hence,

$$\Delta I_{\rm Dsat} = \frac{\mu_{\rm n} C_{\rm ox}}{2} \Delta \left(\frac{W}{L}\right) (V_{\rm GS} - V_{\rm T0})^2. \qquad (2)$$

Commonly, the commercial foundries do not employ a special extraction method for gate-enclosed transistors and their extraction methods may vary from one foundry to another. One popular extraction approach is

$$W = \frac{l_{\rm GD} + l_{\rm GS}}{2}, \qquad (3)$$

$$L = \frac{S_{\rm g}}{W}, \qquad (4)$$

where $l_{\rm GD}$ is the length of the borderline between the gate and the drain, $l_{\rm GS}$ is the length of the borderline between the gate and the source, and $S_{\rm g}$ is the poly gate area, which is above the active area (gate oxide region). By adopting the notations in Fig. 4, $l_{\rm GD}$, $l_{\rm GS}$, $S_{\rm g}$ can be calculated as

$$l_{\rm GD} = 2a_1 + 2a_2, \qquad (5)$$

$$l_{\rm GS} = 2a_1 + 2a_2 + 7b + 2x, \qquad (6)$$

$$S_{\rm g} = \sum_{i=1}^{8} S_i. \qquad (7)$$

It can be seen from Eqs. (3)–(7) that W/L is related to the distance x, but x has little effect in determining the effective W/L, since the foundry-provided tool for extracting effective W/L is targeted toward the two-edged transistor rather than the gate-enclosed transistor.

Another W/L extraction approach[14] states that the poly gate should be divided into certain special rectangles and other sections. What is special about the rectangles is that one side of a rectangle is adjacent to the source and its opposite side is adjacent to the drain (S1, S2, S3 and S4 in Fig. 4). We denote these two sides as W-sides, the other two sides as L-sides, and the special rectangles as regular rectangles (RRs). For the RRs, the effective W/L ratio is calculated as the ratio of the length of the W-side to the length of the L-side. For example, it is

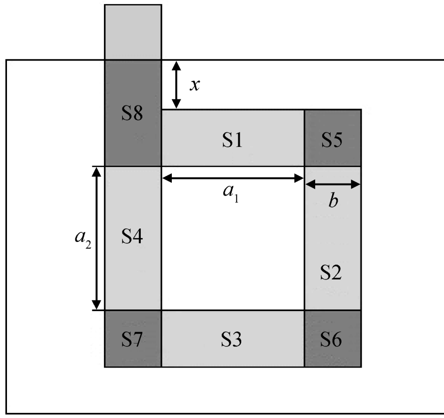


Fig. 4. Schematic layout of an annular transistor.

Table 2. Effective W/L ratios of annular style test devices estimated from various extraction methods.

Test structures	Mid-line approximation	Foundry-provided tool	Calculation method in Ref. [14]
N26A1	22.8	21.2 ($x = b/2$)	19.7 ($C_{ab} = 2$)
N26A2	19.0	18.5 ($x = b/2$)	17.9 ($C_{ab} = 2$)
N11A	12.5	11.5 ($x = b/2$)	10.5 ($C_{ab} = 2$)

a_2/b for S4 in Fig. 4. The effective W/L ratio of the annular device is the sum of the W/L ratios of the RRs and a constant C_{ab}, which is an empirical value between 1 and 2. Thus, the effective W/L ratio can be expressed as

$$\left(\frac{W}{L}\right)_{\text{eff}} = \sum\left(\frac{W}{L}\right)_{\text{RR}} + C_{\text{ab}}. \quad (8)$$

In Fig. 4, it is

$$\left(\frac{W}{L}\right)_{\text{eff}} = \frac{2a_1 + 2a_2}{b} + C_{\text{ab}}. \quad (9)$$

The W/L ratios of our annular test devices derived from the aforementioned three methods are listed in Table 2. The result of the calculation method in Ref. [14] is closer to the effective W/L.

By comparing the mid-line approximation and the calculation method in Ref. [14], it shows that the only difference between the two methods occurs when evaluating the W/L of the corner devices at the four corners of the annular transistor. Indeed, the mid-line approximation can also be expressed by Eq. (9) with $C_{ab} = 4$, while for the calculation method in Ref. [14], C_{ab} is approximately 2. This implies that if C_{ab} is 4, the W/L of the four corner devices will be overestimated; while if C_{ab} is 2, the model can better fit the test results. With the down-scaling of the semiconductor devices, it can be projected that this trend is also applicable to smaller annular transistors.

3.2.2. Characteristics and effective W/L extraction of ring transistors

The output and transfer characteristics of inner-drain ring transistors are shown in Figs. 5 and 6, where it can be seen

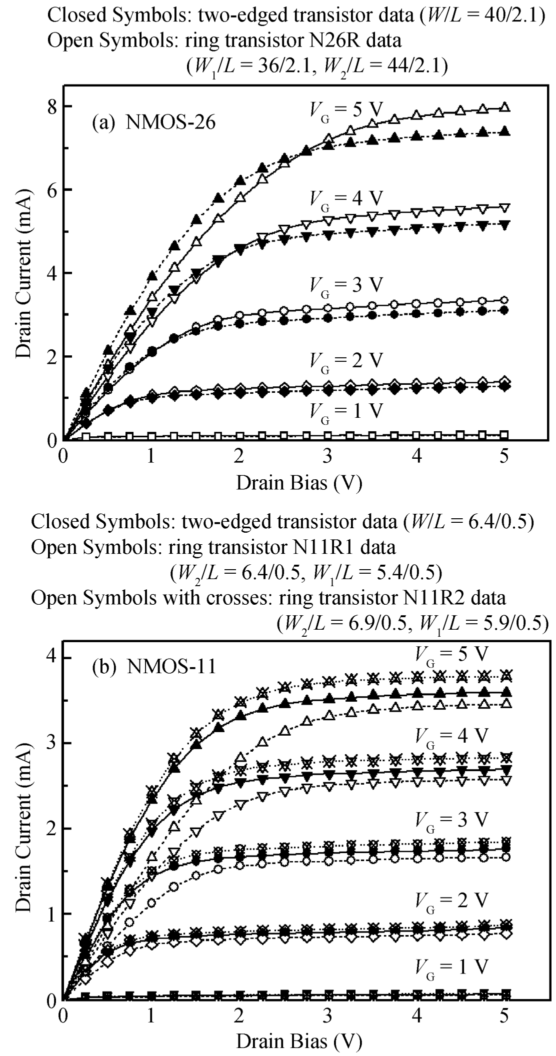


Fig. 5. Measured I_D versus V_D for ring transistors.

that there are significant differences between the ring transistors and the other two types of transistors: annular and two-edged. In the saturation region, the ring transistor's drain current is larger than those of its annular and two-edged counterparts, while it is smaller in the linear region. This implies that there is not an effective W/L ratio for this device that can consistently match the two-edged device in both the linear and saturation regions. The ring style gate layout leads to higher saturation current, a unique feature of the ring transistor with the drain in the ring gate[11], due to its long borderline between the gate and drain, which results in significant channel length modulation.

For the aforementioned reason, the extraction of the effective W/L ratio for the ring transistor is more complicated than that for the annular transistor. The effective W/L of the ring transistor is larger than the W_1/L, due to the existence of the two corner devices. By applying the $(W_1+W_2)/2$ approximation, it can be seen that I_D is larger than its approximated value in the saturation region, and the difference is 5.6% at the point of $V_G = 5$ V and $V_D = 5$ V for the NMOS-11 N11R1 and 7.7% for the NMOS-26 N26R.

In Ref. [12], another simple evaluation method was proposed. When applied to the device in Fig. 7, the method esti-

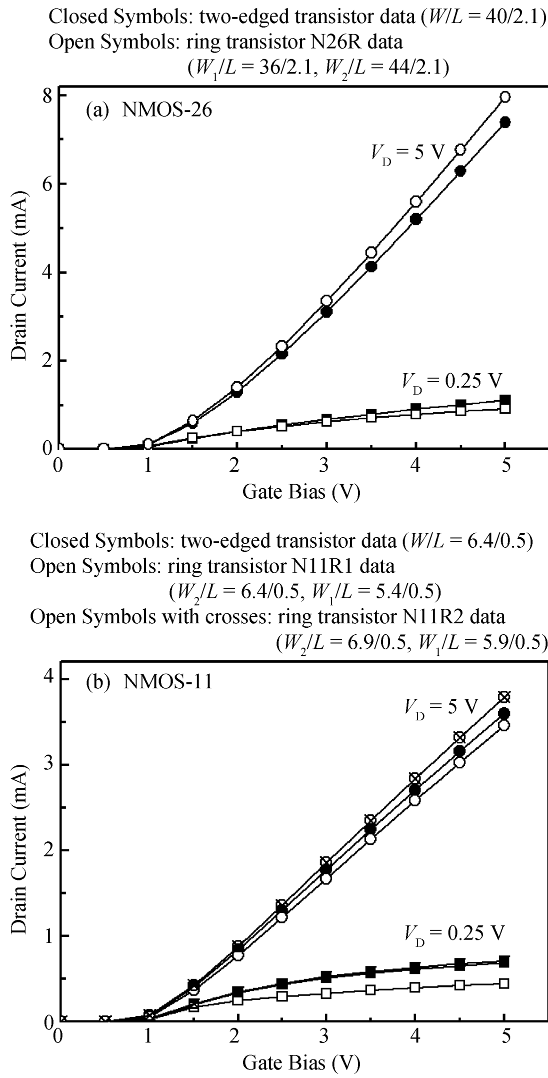


Fig. 6. Measured $I_{\rm D}$ versus $V_{\rm G}$ for ring transistors.

mates the effective W/L as follows,

$$\left(\frac{W}{L}\right)_{\rm eff} = \frac{W_1}{L_1} + 2\frac{W_3}{L_3}, \tag{10}$$

where W_3/L_3 is a rough approximation of the W/L of the corner device. There are two corner devices in each ring style transistor, leading to $2x$ in Eq. (10).

The foundry-provided extraction approach can also be expressed as Eqs. (3) and (4). The W/L ratios of the ring style test devices calculated from the aforementioned methods are listed in Table 3. Among these three methods, none can obtain an effective W/L ratio for a test device that is consistent in both the linear and saturation regions. In the saturation region, the $(W_1+W_2)/2$ approximation underestimates the actual effective W/L ratio. The accuracy of a particular method can be different from NMOS-11 to NMOS-26. Thus, accurately estimating the W/L ratios of ring style transistors needs more tests with more sizes, drawn gates, excess distances overlapping the FOX and more manufacturers. From the test results of this experiment, it appears that the $(W_1 + W_2)/2$ approximation possesses acceptable accuracy for rough estimation of the effective W/L for the ring transistor.

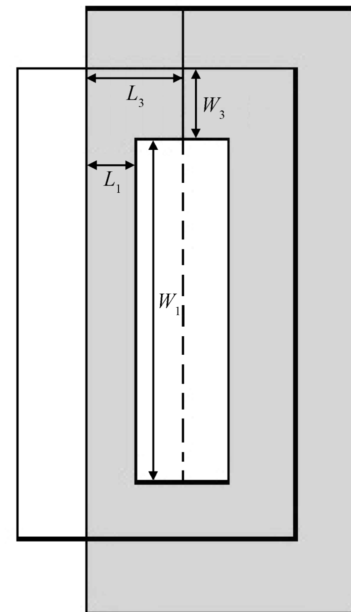


Fig. 7. Schematic layout of a ring style transistor.

Table 3. Effective W/L ratios of ring style test devices estimated from various extraction methods.

Test structure	$(W_1 + W_2)/2$ approximation	Foundry-provided tool	Calculation method in Ref. [12]
N26R	19.0	19.0	19.9
N11R1	11.8	12.1	11.5
N11R2	12.8	13.2	12.5

4. Conclusions

Enclosed-gate NMOS transistors with gates in annular and ring styles were designed and manufactured by a commercial 0.35 μm CMOS process. The key geometric parameters of these transistors, including the minimum W/L ratios and the transistor areas, were quantitatively compared with each other to provide guidelines for TID-tolerant design. It was shown that in terms of area penalty, the ring transistor is superior when the W/L ratio of the transistor to be designed is close to the minimum W/L of the two-edged transistor, while the annular transistor is a better solution when the W/L ratio of the transistor to be designed is larger than the minimum W/L of the annular transistor.

The output and transfer characteristics of the enclosed-gate transistors were measured and compared with their two-edged counterparts to extract the effective W/L ratios. Three popular methods were applied in the extraction and it was shown that while for the annular transistors there existed one method providing results with acceptable accuracy, none of the three methods was accurate enough for the ring transistors. The $(W_1 + W_2)/2$ approximation for the ring transistors was presented as a simple approach for rough estimation of the effective W/L. Moreover, the foundry-provided tool for extracting the effective W/L is targeted toward the two-edged transistor and needs significant adaptation when applying to the enclosed-gate transistors.

References

[1] Lopez P, Cabello D, Hauer H. Improved analytical $I-V$ model for polygonal-shape enclosed layout transistors. 18th European Conference on Circuit Theory and Design, 2007: 755

[2] Chen L, Gingrich D. Study of N-channel MOSFETs with an enclosed-gate layout in a 0.18 μm CMOS technology. IEEE Trans Nucl Sci, 2005, 52(4): 861

[3] Faccio F, Cervelli G. Radiation-induced edge effects in deep submicron CMOS transistor. IEEE Trans Nucl Sci, 2005, 52(6): 2413

[4] Li Dongmei, Huangfu Liying, Gou Qiujing, et al. Total ionizing dose radiation effects on MOS transistors with different layouts. Chinese Journal of Semiconductors, 2007, 28(2): 171

[5] Lacoe R, Osborn J, Koga R, et al. Application of hardness-by-design methodology to radiation-tolerant ASIC technologies. IEEE Trans Nucl Sci, 2000, 47(6): 2334

[6] Lacoe R. Improving integrated circuit performance through the application of hardness-by-design methodology. IEEE Trans Nucl Sci, 2008, 55(4): 1903

[7] Dodd P, Shaneyfelt M, Schwank J R, et al. Current and future challenges in radiation effects on CMOS electronics. IEEE Trans Nucl Sci, 2010, 57(4): 1747

[8] Snoeys W, Faccio F, Burns M, et al. Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2000, 439(2/3): 349

[9] Martin M, Strohbehn K. Analog rad-hard by design issues. The 11th Annual NASA Symposium on VLSI Design Conference, May 2003

[10] Giraldo A, Paccagnella A, Minzoni A. Aspect ratio calculation in n-channel MOSFETs with a gate-enclosed layout. Solid-State Electron, 2000, 44(6): 981

[11] Clark L, Mohr K, Holbert K. Reverse-body biasing for radiation-hard by design logic gates. IEEE International Reliability Physics Symposium Proceedings, 2007: 582

[12] Nowlin R, McEndree S, Alexander D, et al. A new total-dose-induced parasitic effect in enclosed-geometry transistors. IEEE Trans Nucl Sci, 2005, 52(6): 2495

[13] Chen Jianjun, Chen Shuming, Liang Bin, et al. Hot carrier effects of SOI NMOS. Journal of Semiconductors, 2010, 31(6): 074006

[14] Wang Liang, Yue Suge. One layout parameters extraction approach of annular devices. Chinese Patent, No. 101556626A, 2009-10-14