A 14-bit wide temperature range differential SAR ADC with an on-chip multi-segment BGR

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Abstract: A 14-bit low power self-timed differential successive approximation (SAR) ADC with an on-chip multi-segment bandgap reference (BGR) is described. An on-chip multi-segment BGR, which has a temperature coefficient of 1.3 ppm/℃ and a thermal drift of about 100 μV over the temperature range of −40 to 120 ℃ is implemented to provide a high precision reference voltage for the SAR ADC. The Gray code form is utilized instead of binary form mode control to reduce substrate noise and enhance the linearity of the whole system. Self-timed bit-cycling is adopted to enhance the time efficiency. The 14-bit ADC was fabricated in a TSMC 0.13 μm CMOS process. With the on-chip BGR, the SAR ADC achieves an SNDR of 81.2 dB (13.2 ENOB) and an SFDR of 85.2 dB with a conversion rate of 2 MS/s at room temperature and can keep an ENOB of more than 12 bits at a conversion rate of 2 MS/s over the temperature range from –40 to 120 ℃.

Key words: differential successive approximation ADC; self-timed bit-cycling; gray code; on-chip multi-segment BGR

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1. Introduction

As an important component of the interface between analog and digital circuits, the successive approximation (SAR) ADC has advantages of low power consumption, medium conversion speed and high resolution. However, for the common architecture, there are still some limitations such as low time efficiency, sensitivity to noise from the digital part and the need for a high precision outside reference voltage in order to ensure performance[1]. For high precision SAR ADC designs, such as the structures described in Refs. [2, 3], a high precision outside voltage reference is needed to ensure their performance and the temperature coefficient of the outside voltage reference will directly harm the precision of the ADC.

In this design, an on-chip multi-segment BGR is implemented to make the ADC suitable for integration with other ICs on one chip. A differential structure is utilized to improve the PSRR of the whole system. Self-timed bit-cycling is adopted to enhance time efficiency while gray coding form mode control words are used instead of the binary coding form to reduce the circuit noise generation from the digital part.

With the low temperature coefficient (1.3 ppm/℃) low thermal drift (100 μV) reference voltage provided by a BGR, the presented ADC can keep an ENOB of more than 12 bits at a conversion rate of 2 MS/s over a temperature range from −40 to 120 ℃. The power consumption of the ADC core is only 1.2 mW.

2. Architecture design

A block diagram of the differential SAR ADC is shown in Fig. 1. The DAC has been separated into an 8-bit main capacitive DAC and a 6-bit sub resistive DAC in order to guarantee precision while reducing the area. A multi-segment BGR is realized to provide the reference voltage for the system. The remainder of this section describes the optimization of the overall conversion process.

2.1. Conversion plan

Figure 2 shows the conversion plan of this ADC. The purging (PRG) phase is the start of the conversion. During this phase, the top and bottom plates of the capacitive main DAC are both connected to ground in order to eliminate the charge. Then auto-zeroing phase (AZ) is started to cancel the offset of the pre-amplifiers and the latch. The purging and auto-zeroing phases improve the common-mode rejection and the noise performance of the ADC. The sampling phase takes 3 clock cycles and is followed by a period of self-timed bit-cycling.

2.2. Self-timed sequential control

In order to make full use of the clock period, the self-timed scheme proposed in Ref. [4] is used in this design. A synchronous timing scheme for controlling bit-cycling is shown in Fig. 3(a). The DAC and pre-amplifiers settle during the first half of the clock cycle and the latch resolves during the second half. In this instance, the DAC and the preamplifier have $(t_{\mathrm{CLK}}/2) - t_{\mathrm{CK\text{-}Q}}$ to settle to their relevant value. Figure 3(b) shows the self-timed bit-cycling[4]. During the first clock period, the positive edge of the clock triggers the decision of the latch. Since the outputs of the latch CP and the CN are both logic “0” before the latch decision, if the CP and CN become different, the signal COMPLETE will then be high and will reset the latch. Then, the CN and the CP will return to logic “0”.

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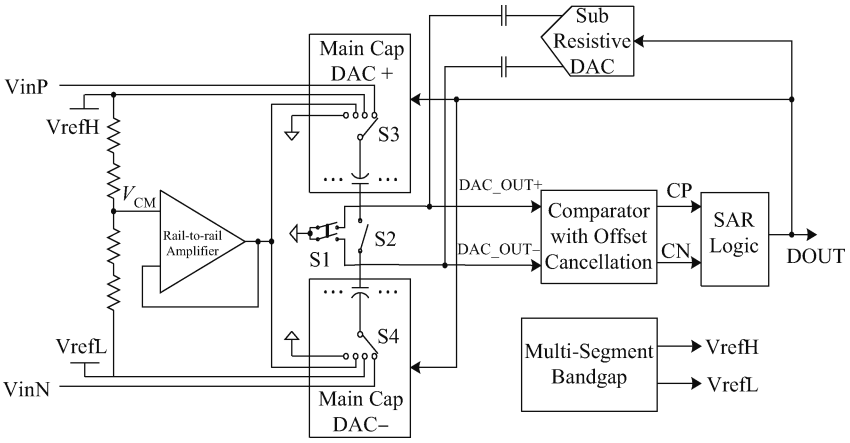

Fig. 1. Block diagram of the differential SAR ADC.

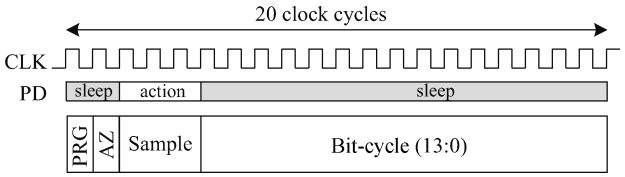

Fig. 2. ADC conversion plan showing.

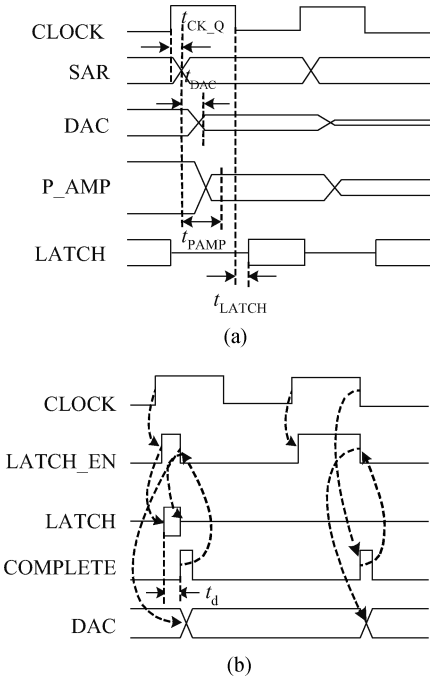

Fig. 3. Timing showing. (a) Synchronous sequential control. (b) Self-timed sequential control.

A small delay t_d is necessary and provides the CN and CP with enough width for the SAR logic to decide which codes should be put out.

2.3. Gray coding form mode control

Figure 4 shows the voltage spike caused by the binary input codes. Assuming input A changes from "0" to "1" while input

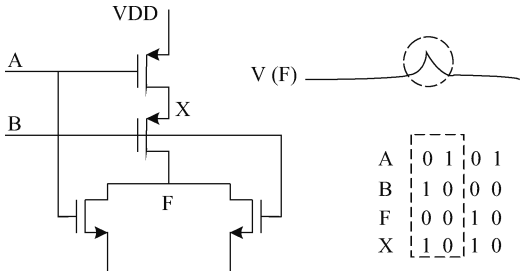

Fig. 4. Voltage spike caused by binary input codes.

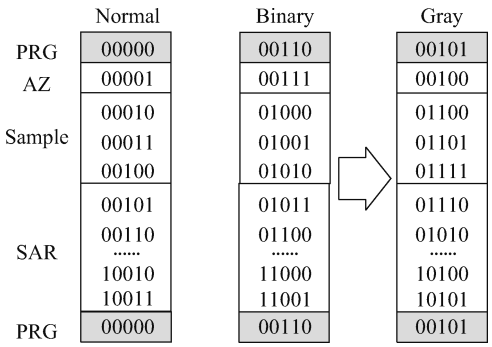

Fig. 5. Gray coding form mode control words.

B changes from "1" to "0", if the changes of input B are a little later than A, there will be a spike on output node F. However, this is not expected.

The unexpected voltage spikes will seriously affect the performance of the SAR ADC. Obviously, reducing noise generation is important for a high precision ADC. The gray coding form can effectively estimate these kinds of spikes.

In this design, gray coding form mode control words are adopted to control the mode of the whole system. Figure 5 shows the normal binary coding form and gray coding form mode control words used in this design. The whole conversion is controlled by 20 5-bit words, of which one is for purging, one is for auto-zeroing, three are for sampling and the remaining 15 are for SAR bit-cycling.

Obviously, each normal binary coding form word has more than one bit different from its adjacent word and this may cause

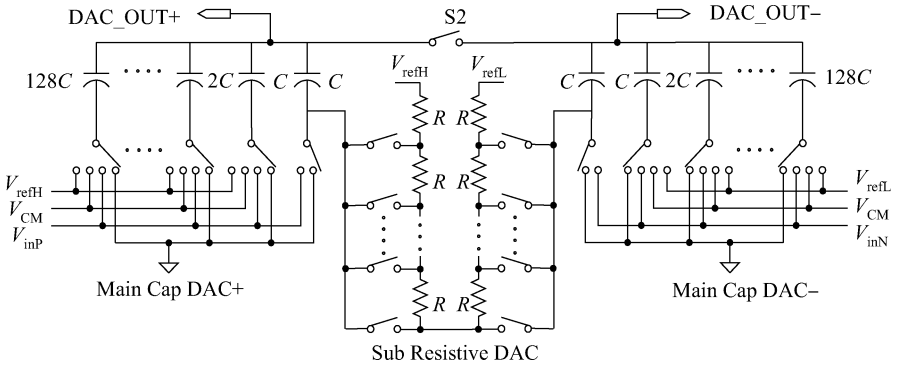

Fig. 6. DAC block diagram.

voltage spikes because of the different signal timing delays.

In this design, the counter recurs in the 20 5-bit binary coding form words and the words are changed to gray coding form mode control words. By doing this, every two adjacent words have only one bit different and this is used to estimate unexpected voltage spikes.

3. Circuit blocks

3.1. DAC circuit

Figure 6 shows the capacitor-resistor combined DAC. The DAC consists of an 8-bit main capacitive DAC and a 6-bit sub resistive DAC. The operation of the DAC is properly treated to ensure the precision of the whole ADC.

As is described in Section 2, purging is implemented in order to eliminate the charges on the capacitor array. Then, auto-zeroing is performed to cancel the offset of the pre-amplifiers and latch. Finally, sampling is performed. During sampling, the top plates of the two capacitor arrays are connected together by switch S_2 while the bottom plates of the main cap DAC+ are connected to the V_{inP} and the bottom plates of the main cap DAC– are connected to the V_{inN}. The voltage of the capacitor array's top plate will then be $(V_{inP} + V_{inN})/2$. When sampling is complete, switch S_2 is turned off and the bottom plate of the capacitor array is connected to V_{cm} ($V_{ref}/2$) voltage. The output voltages of the DAC V_{DAC_OUT+} and V_{DAC_OUT-} will then be $V_{cm} + (V_{inP} + V_{inN})/2$ and $V_{cm} + (V_{inP} + V_{inN})/2$, respectively.

After sampling, the self-timed bit-cycling will be started.

3.2. On-chip multi-segment BGR

The performance of the BGR directly affects the precision of the SAR ADC. The output voltage of a common BGR has a large curvature and cannot meet the requirements of high precision ADCs[5].

In order to ensure the performance of the SAR ADC, the voltage drift v_{drift} of the BGR over the range from – 40 to 120 ℃ should be less than 0.5 LSB. The voltage drift v_{drift} can be defined using the formula below:

$$v_{drift} < 0.5\,\mathrm{LSB} = 0.5\frac{V_{refP} - V_{refN}}{2^N}. \quad (1)$$

For the 14-bit SAR ADC, the BGR should have a voltage drift of less than 100 μV from –40 to 120 ℃.

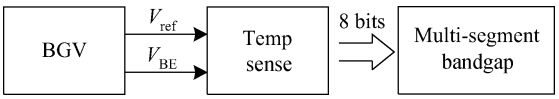

Fig. 7. Blocks of the multi-segment BGR.

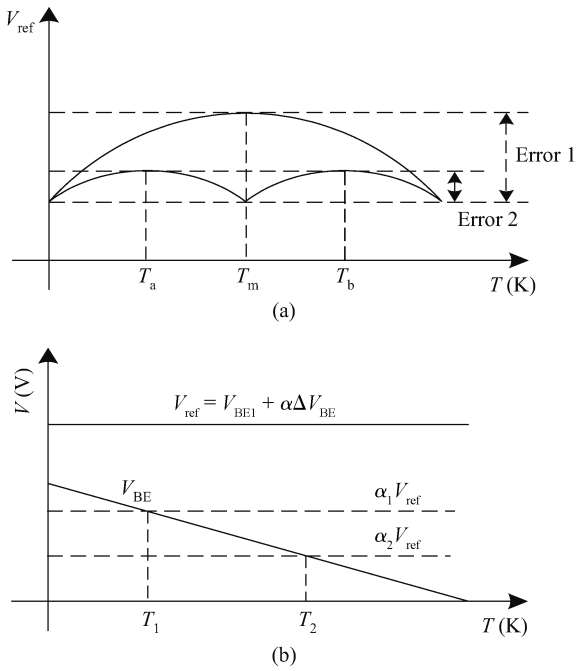

Fig. 8. Temperature variation of (a) voltage reference and (b) base–emitter voltage.

There are some reported approaches to decreasing voltage drift, for example, the design in Ref. [6] employs two resistors of different materials in order to obtain quadratic temperature compensation, and the design in Ref. [7] makes the bandgap reference output a low temperature coefficient voltage. However, these two approaches are both sensitive to process variations and difficult to implement.

In this design, an on-chip multi-segment BGR is realized. The BGR block is shown in Fig. 7. It has three advantages over the normal structure: (1) no continuous and differential nonlinear cancellation is used; (2) it is not sensitive to process variations; and (3) no additional clock signal is needed for temperature sensing and range division.

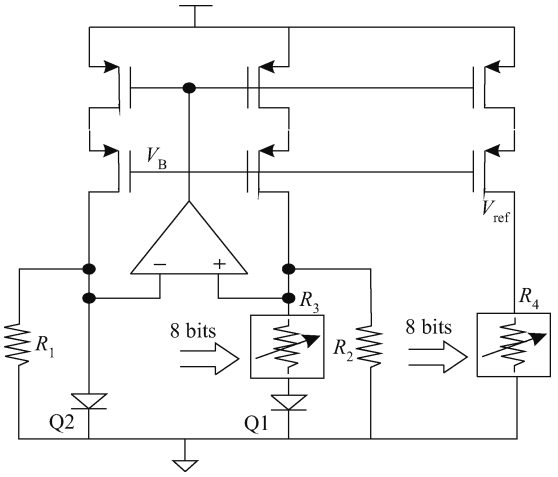

Fig. 9. Circuit of the multi-segment BGR.

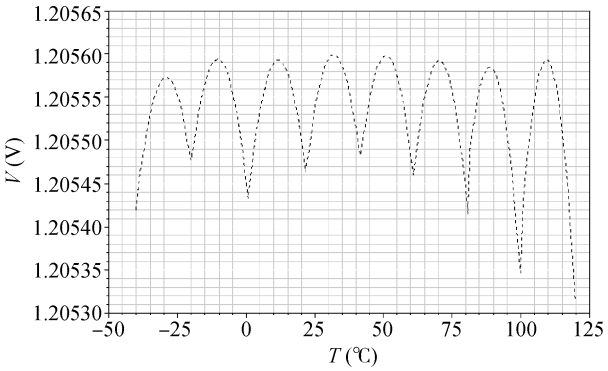

Fig. 10. Output waveform of the multi-segment BGR

Figure 8(a) shows the temperature variation of the voltage reference. It can be noticed that in the common BGR the voltage reference $V_{\rm ref}$ has zero temperature variation at $T = T_{\rm m}$ and has minimal variation with temperature for T around Tm. Therefore, if a BGR circuit has an adaptive Tm that varies over temperature, a $V_{\rm ref}$ with minimal temperature variation over a wide temperature range can be realizable. In this design, the temperature range is divided by several special temperature points, which is called the jump temperature $T_{\rm x}$ and each temperature segment has an appropriate $T_{\rm m}$.

As shown in Fig. 8(b), the base–emitter voltage $V_{\rm BE}$ has a temperature coefficient of about –1.5 mV/K, which decreases almost linearly with temperature. When $a_2 V_{\rm ref} < V_{\rm BE} < a_1 V_{\rm ref}$, it can be deduced that $T_1 < T < T_2$. The temperature range can be divided by the jump temperature $T_{\rm x}$ and each jump temperature has a corresponding jump voltage $a_x V_{\rm ref}$. By real-time comparison of $V_{\rm BE}$ and the jump voltage $a_x V_{\rm ref}$, the corresponding temperature interval can be divided. In this design, the temperature range is divided into 8 segments and each segment is about 20 ℃.

However, this design does not need an additional signal, such as an outside clock signal, such as in Refs. [8, 9]. Temperature sensing is realized by 8 low power comparators connected in parallel to compare $a_x V_{\rm ref}$ with $V_{\rm BE}$ instead of using an additional ADC. The additional clock signal can then be moved, thereby simplifying the design.

The circuit of the multi-segment BGR is shown in Fig. 9. The temperature characteristic of $V_{\rm BE}$ is governed by the following expression[10]:

$$V_{\rm BE}(T) = V_{\rm G0}\left(1 - \frac{T}{T_0}\right) + \frac{T}{T_0}V_{\rm BE0} - \eta\frac{kT}{q}\ln\frac{T}{T_0} + \frac{kT}{q}\ln\frac{J_{\rm C}}{J_{\rm C0}}, \quad (2)$$

where $V_{\rm G0}$ is the silicon bandgap voltage extrapolated to 0 K (–1.206 V), k is Boltzmann's constant, η is a process-dependent constant, T_0 is the reference temperature, $V_{\rm BE0}$ is the base–emitter voltage drop at the reference temperature and $J_{\rm C}$ is the collector current density evaluated at the reference temperature T. According to the formula below:

$$V_{\rm ref} = V_{\rm BE} + \partial\Delta V_{\rm BE}, \quad (3)$$

by adjusting ∂, the first-order temperature coefficient can be cancelled, Equation (3) can be expanded and rewritten as

$$V_{\rm ref} = V_{\rm G0} + (\eta - 1)\frac{kT}{q}\ln\frac{T_0}{T}. \quad (4)$$

It can be deduced that

$$\frac{\partial V_{\rm ref}}{\partial T} = (\eta - 1)\frac{k}{q}\ln\frac{T_0}{T}. \quad (5)$$

Then the change of $V_{\rm ref}$ will be zero when $T = T_0$. So by defining specific $T_{\rm m}$ in a different temperature segment, a $V_{\rm ref}$ with a minimal temperature variation can be realized.

Assuming $T/T_0 = J_{\rm C}/J_{\rm C0}$, an appropriate $T_{\rm m}$ can be obtained by tuning the value of R_3 to change the collector current density of Q1. However, $V_{\rm ref}$ of different segments will be different because of different R_3 and this can be calibrated by adjusting the value of R_4 while changing R_3.

Figure 10 shows the output waveform of the multi-segment BGR. The simulated result shows that the none-clock on-chip multi-segment BGR can obtain a temperature coefficient of 1.3 ppm/℃ over a temperature range from −40 to 120 ℃, and the thermal drift is about 100 μV.

3.3. Comparator architecture

A comparator of immense gain, speed and sensitivity is required for resolving small inputs into full-scale digital values. It is vital for ADC performance.

The comparator and its components are shown in Fig. 11. The comparator is composed of three pre-amplifiers and a latch. The stages are coupled by capacitors. During purging, all the capacitors are purged and all the stages are configured to proper stations. At the same time, the offset of the stages are stored on the coupled capacitors[11]. Then T4, T3 and T2 are turned off sequentially to cancel the offset.

An offset compensating latch presented by Verma N[4] is used to eliminate the effect of the offset of latch, as shown in Fig. 12. During the auto-zeroing phase, $S_{\rm DIFFMD}$, $S_{\rm CSCD}$ and $S_{\rm FB}$ are all closed while a zero-differential input is applied to M1 and M2 to force $V_{\rm SRC1,2}$ to be equal and then $S_{\rm DIFFMD}$ is opened to store and cancel the offset of the input devices. During the first half of bit-decisions, $S_{\rm DIFFMD}$, $S_{\rm SC}$, $S_{\rm R}$ and $S_{\rm AUX}$ are closed

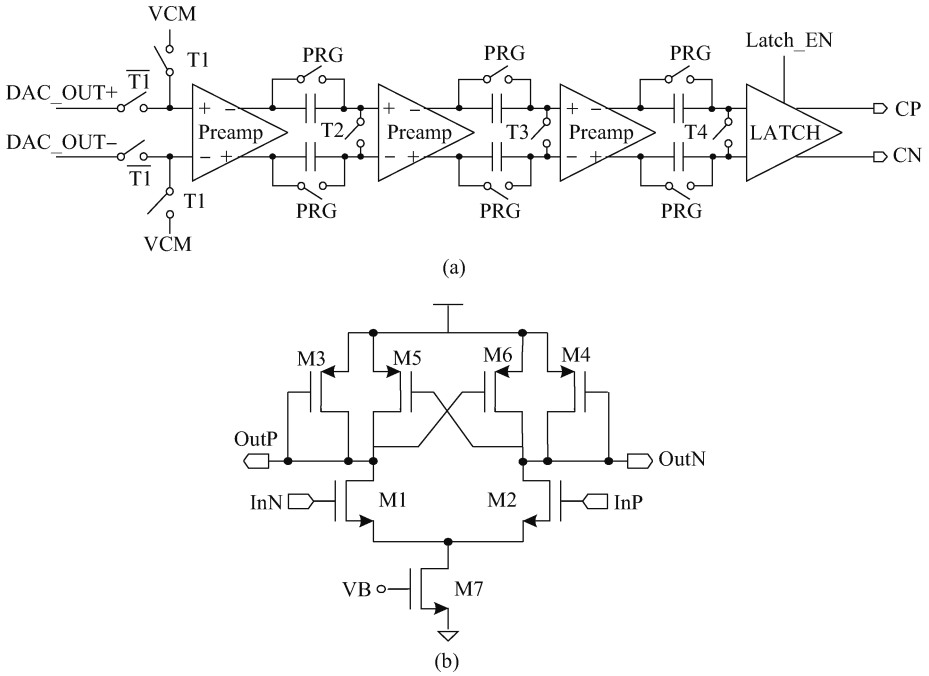

Fig. 11. Schematic diagram. (a) Comparator. (b) Pre-amplifier.

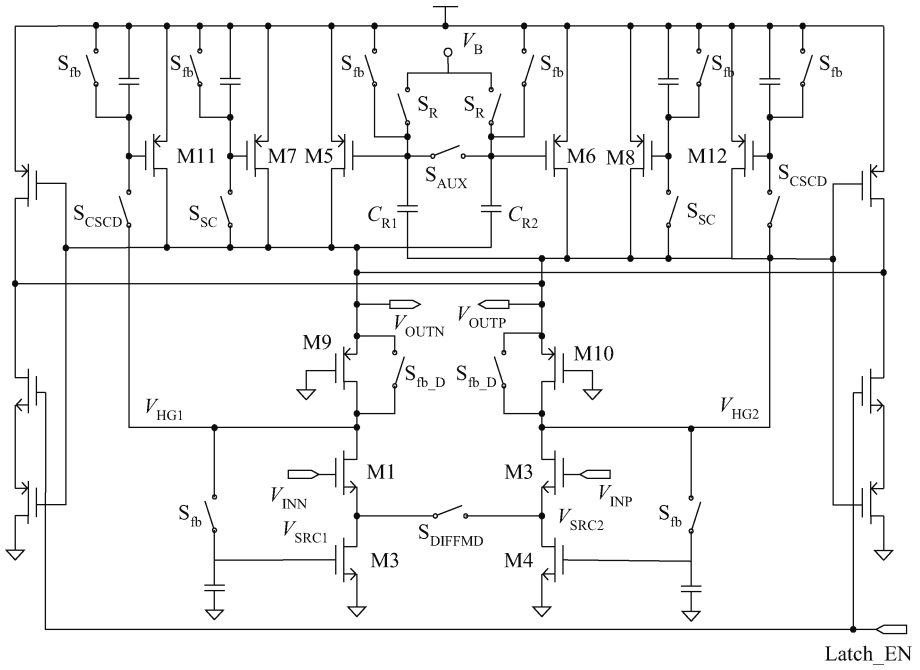

Fig. 12. Schematic diagrams of latch.

and S_{DIFFMD} is initially open. During the second half phase of bit-decisions, S_{SC}, S_R and S_{AUX} are all opened and S_{DIFFMD} is closed to make a decision.

However, there is a small delay between the action of S_{AUX} and S_R in order to minimize the charge injection error caused by mismatch in the S_R switches.

4. Implementation and measurement results

The presented differential SAR ADC was designed and implemented in TSMC 0.13 μm CMOS processing. A micrograph of the entire ADC is shown in Fig. 13. The area of the ADC core is1200 × 800 μm^2.

Figure 14 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) at room temperature. With the reference voltage provided by the on-chip multi-segment BGR, the maximum DNL is 0.42 LSB, while the maximum INL is 0.63 LSB.

The measured SFDR and SNDR versus the input frequency at room temperature are plotted in Fig. 15. At 0.12 MHz input frequency, the SNDR and SFDR are 81.2 dB and 85.2 dB, respectively. In addition, an ENOB of 13.2 bits can be

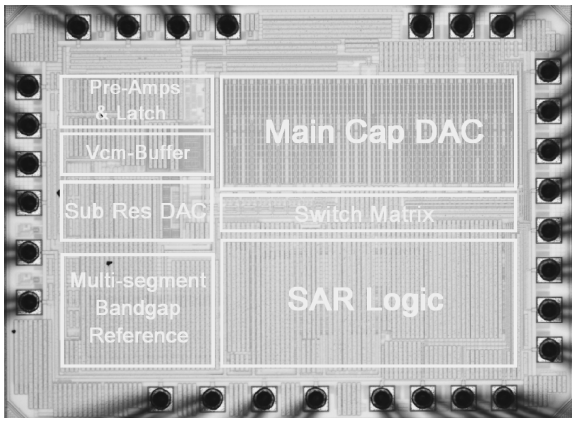

Fig. 13. Micrograph of the entire ADC prototype.

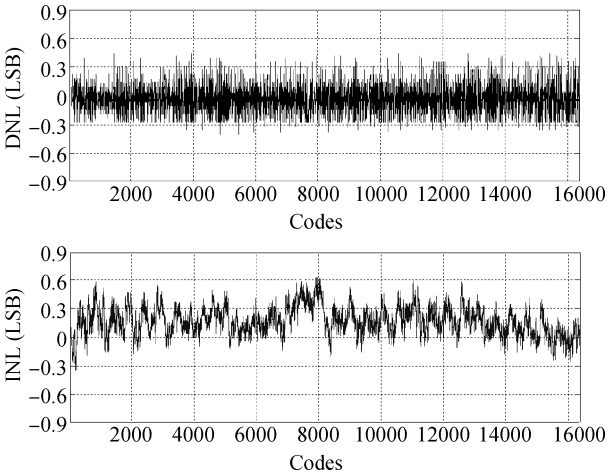

Fig. 14. DNL and INL of the ADC.

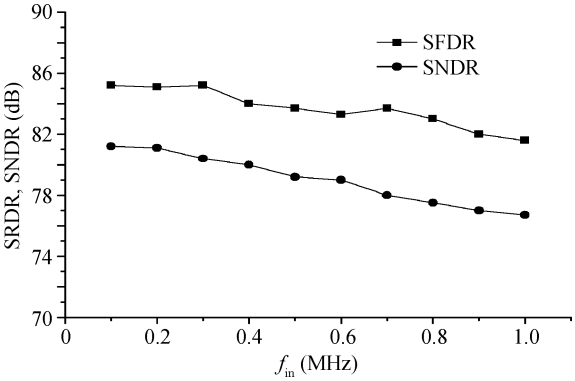

Fig. 15. SFDR and SNDR versus the input frequency.

achieved. When the input frequency reaches 1 MHz (Nyquist frequency), the SNDR and SFDR are 76.9 dB and 82.2 dB, respectively. Figure 16 provides the FFT spectrum of the output signal when the input frequency is close to 0.1 MHz.

Figure 17 plots the temperature performance of the SAR ADC. For a 0.12 MHz 2.6 V_{pp} input signal, it can keep an ENOB of more than 12 bits at a conversion rate of 2 MS/s over the temperature range from –40 to 120 ℃.

The measured performance of the ADC is summarized in Table 1, and is compared with other SAR ADCs, as listed in Table 2. The typical power consumption of the active circuit is 2.23 mW. The SAR ADC draws 1.2 mW. The power consumption of the BGR is 1.03 mW.

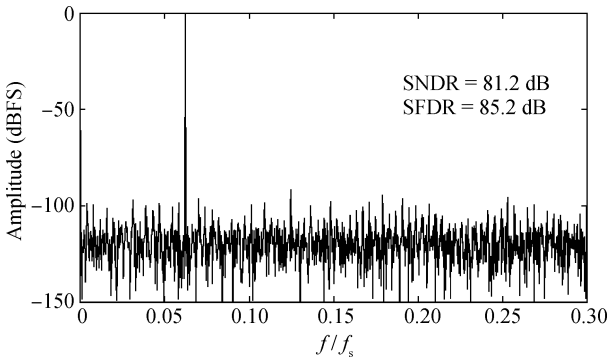

Fig. 16. Dynamic performance of ADC.

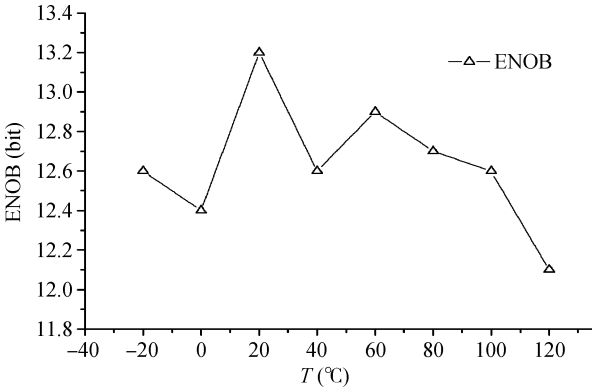

Fig. 17. Temperature performance of the SAR ADC.

Table 1. Specification summary.

Parameter	Value
Resolution	14 bits
Process	0.13 μm CMOS
Power supply	3.3 V
Core area	1200 × 800 μm^2
Conversion rate	2 MS/s
DNL	< 0.42 LSB
INL	< 0.63 LSB
SNDR	81.2 dB (f_{in} = 0.12 MHz)
SFDR	85.2 dB (f_{in} = 0.12 MHz)
Total power consumption	2.23 mW (SAR ADC: 1.2 mW, BGR: 1.03 mW)
FOM	63.8 fJ/conv-step

The figure-of-merit (FOM) is calculated to normalize the ADC power consumption to the sampling rate and the dynamic range it achieves.

According to the formula below:

$$\mathrm{FOM} = \frac{P}{F_S \cdot 2^{\mathrm{ENOB}}}, \tag{6}$$

the 14 bits differential SAR ADC can achieve a FOM of 63.8 fJ/conv-step.

Table 2. Comparison of ADC performance.

Parameter	Ref. [2]	Ref. [12]	Ref. [13]	Ref. [14]	Proposed
Technology (μm)	0.13	0.13	0.13	0.35	0.13
Resolution (bit)	12	12	14	12	14
Sampling rate (MS/s)	22.5	10	40	0.024	2
Supply voltage (V)	1.2	3.3	1.5	3.3	3.3
ENOB (bit)	11.5	9.62	13	11	13.2
Power (mW)	3	3	66	0.08	2.23
FOM (fJ/conv-step)	46	381	101	940	63.8
Temperature sensitive	yes	yes	yes	yes	no

5. Conclusion

A 14-bit low power self-timed differential SAR ADC with an on-chip multi-segment BGR has been presented. Self-timed bit-cycling is adopted instead of a normal synchronous timing scheme in order to enhance time efficiency. Gray coding form mode control words are used instead of binary mode control to reduce substrate noise from the digital part and enhance the linearity of the ADC. An on-chip multi-segment bandgap reference (BGR) with a temperature coefficient of 1.3 ppm/℃ and thermal drift of 100 μV over 160 ℃ is implemented to provide a high precision reference voltage for the SAR ADC. The measurement results show that with the on-chip reference voltage, the differential SAR ADC can achieve an ENOB of 13.2 bits and a FOM of 63.8 fJ/conv-step at 2 MS/s at room temperature and can keep an ENOB of more than 12 bits at a conversion rate of 2 MS/s over the temperature range from –40 to 120 ℃.

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