Effect of annealing process on the surface roughness in multiple Al implanted 4H-SiC*

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Abstract: A P-layer can be formed on a SiC wafer surface by using multiple Al ion implantations and post-implantation annealing in a low pressure CVD reactor. The Al depth profile was almost box shaped with a height of $1 \times 10^{19} cm^{-3}$ and a depth of 550 nm. Three different annealing processes were developed to protect the wafer surface. Variations in RMS roughness have been measured and compared with each other. The implanted SiC, annealed with a carbon cap, maintains a high-quality surface with an RMS roughness as low as 3.8 nm. Macrosteps and terraces were found in the SiC surface, which annealed by the other two processes (protect in Ar/protect with SiC capped wafer in Ar). The RMS roughness is 12.2 nm and 6.6 nm, respectively.

Key words: 4H-SiC; ion implantation; annealing; surface morphology
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1. Introduction

With its outstanding physical properties, silicon carbide (SiC) is a suitable semiconductor for high power, high temperature and high frequency devices. Significant progress in the understanding of SiC material properties, in the growth of single crystals and in the development of a specific SiC device technology has been made in recent years[1]. Among the technological steps still delaying the industrial implementation and the development of unipolar and bipolar power devices, p-type layer realization has to be improved to allow good doping control and ohmic contacts on p-type SiC with low specific resistance[2].

Ion implantation is the most commonly applied method to locally dope SiC with the very slow diffusion of dopants in SiC. With ion implantation, one can precisely control the average depth and dose of the dopants by adjusting the acceleration voltage and ion current during the implantation, respectively. Furthermore, multiple Al and/or B ion implantation is used to obtain uniformly doped p-type wells in 4H-SiC, employed as the active region for power device applications[3]. To activate the implanted impurities, which should migrate into electrically active sites of the SiC target, and to reduce the radiation damage, which is caused by ion implantation, high annealing temperatures are necessary, typically in the 1600–1800 ℃ range and even more[4−6]. However, a high annealing temperature may cause the surface deterioration of the implanted layers due to the Si or SiC evaporation[7]. A serious consequence of the roughened surface is the deleterious effects on inversion layer mobilities and specific on-resistances of many SiC devices[8].

Many effective methods used to protect the SiC surface during high temperature annealing have been reported[9−11]. However, their work cannot be compared with each other, because of different SiC samples and ion-implant processes. In this paper, the samples, which were cut by one wafer after multiple Al ion implantations, were annealed by three different annealing processes. The first process uses Ar as the anneal background atmosphere. The second uses a SiC cap wafer to provide an overpressure of Si vapor. The third uses a carbon cap to protect the surface of the sample. The objective is to examine which annealing process offers the best means of protecting the sample surface, and to investigate how different processes affect the surface morphology. The Al dopant profile and the electrical activation of the implanted layer with increasing annealing temperature are also discussed.

2. Experimental

Samples used were 5 μm thick, n-type epitaxial layer, with a doping concentration of 2×10^{17} cm^{-3}, grown on n-type 8° off-axis 4H-SiC (0001) from Tanke, Inc. Specific energy/dose schedules for the multiple-flux implantations of Al^+ were 550 keV/2.4×10^{14} cm^{-2}, 450 keV/2.0×10^{14} cm^{-2}, 350 keV/1.9×10^{14} cm^{-2}, 250 keV/1.5×10^{14} cm^{-2}, 160 keV/1.3×10^{14} cm^{-2}, 70 keV/7.5×10^{13} cm^{-2}, and 30 keV/3.8×10^{13} cm^{-2}. All implantations were performed at 400 ℃. Following implantation, samples were divided into three parts. All parts of the samples were annealed in argon ambient. Two of these three parts used a SiC cap wafer and a carbon cap to protect the surface, respectively. The carbon cap was formed by

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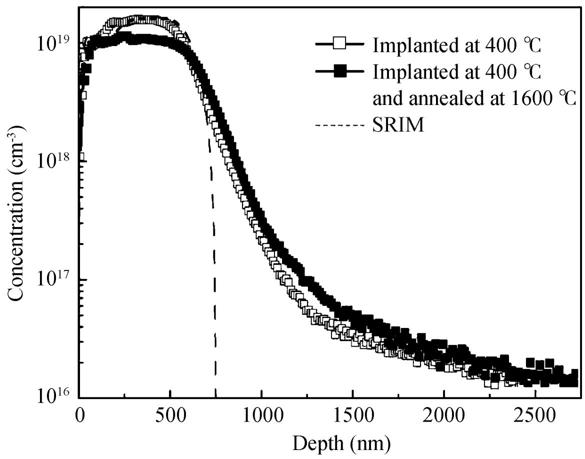

Fig. 1. Aluminum box profile of samples formed by multiple-flux implantation.

spinning on a uniform layer of positive photoresist (3 μm) and then baking at 500 ℃ in argon for 1 h. The root mean square (RMS) roughness of the samples was measured by an atomic force microscope (AFM). The electrical properties were characterized by Hall-effect measurements. Al dopant profiles were determined by secondary ion mass spectrometry (SIMS) before and after annealing the implanted samples.

3. Result and discussion

The aluminum implantation profiles of the implanted samples before and after annealing at 1600 ℃ are shown in Fig. 1. The solid curves are determined by the SIMS and the dotted curve is calculated by the stopping and range of ions in the master (SRIM) simulation program. The distribution of aluminum atoms determined by SIMS agrees well with the calculated Al profile. The p-layer with a consistent concentration was formed on the sample surface by using multiple Al ion implantations. As shown in Fig. 1, compared with the implanted sample, the Al profile in the annealed sample exhibits a small extent of in-diffusion into the bulk SiC. This means that the Al atoms have no obvious re-diffusion after annealing.

Atomic force micrographs were taken from all samples in this study. As an example, Figure 2 shows the surface morphology of implanted SiC, before and after annealing at 1600 ℃ and 1700 ℃ for 30 min. There are no terraces observed on the as-implanted sample surfaces (Fig. 2(a)). On the surfaces of the annealed samples, large macrosteps and terraces can be seen, possibly due to sublimation of the SiC surface. And comparing the RMS value of Figs. 2(b) with 2(c), we also found that surface coarsening increased with temperature. A mechanism of this morphological transformation must be initiated by the dissociation of SiC, leading to the desorption of Si-containing molecules from SiC (sublimation), and the accumulation of mobile species on the surface. In the traditional sense, step bunching occurs during epitaxy and all steps flow in the down-step direction. But this cannot be responsible for the observed roughening because there is a net accumulation of SiC for such an occurrence. However, there are no external Si or C sources needed for growth during high temperature annealing. It is likely that a dynamic step flow process during sublimation contributes to step bunching and the formation of macrosteps, as seen in Fig. 2(b), which was proposed by Capano *et al.*[7].

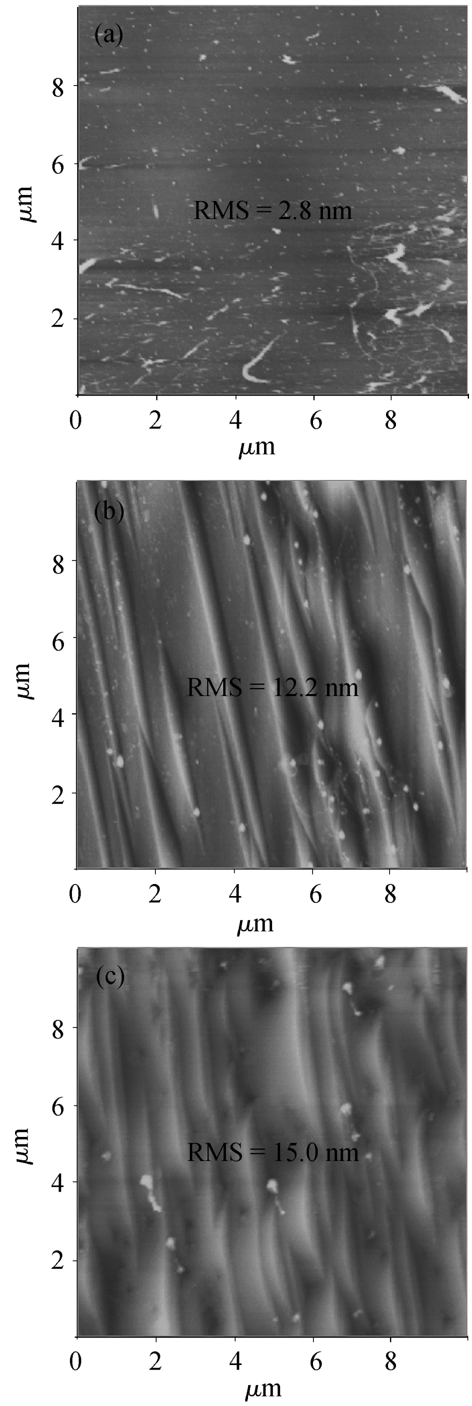

Fig. 2. AFM images of (a) Al as-implanted 4H-SiC (b) after 1600 ℃/30 min annealing and (c) after 1700 ℃/30 min annealing.

In order to prevent deterioration of the SiC surface after annealing, a SiC cap wafer and a carbon cap were considered to use to reduce the surface sublimation problem. In Fig. 3, the comparison between the AFM morphological images of the SiC annealed at 1600 ℃ and 1700 ℃ in two different annealing processes are shown, together with the respective RMS roughness values. Clearly, the surface roughness was dramatically reduced when a SiC cap was used. As shown in Figs. 3(a) and 3(b), compared with Figs. 2(b) and 2(c), the RMS value de-

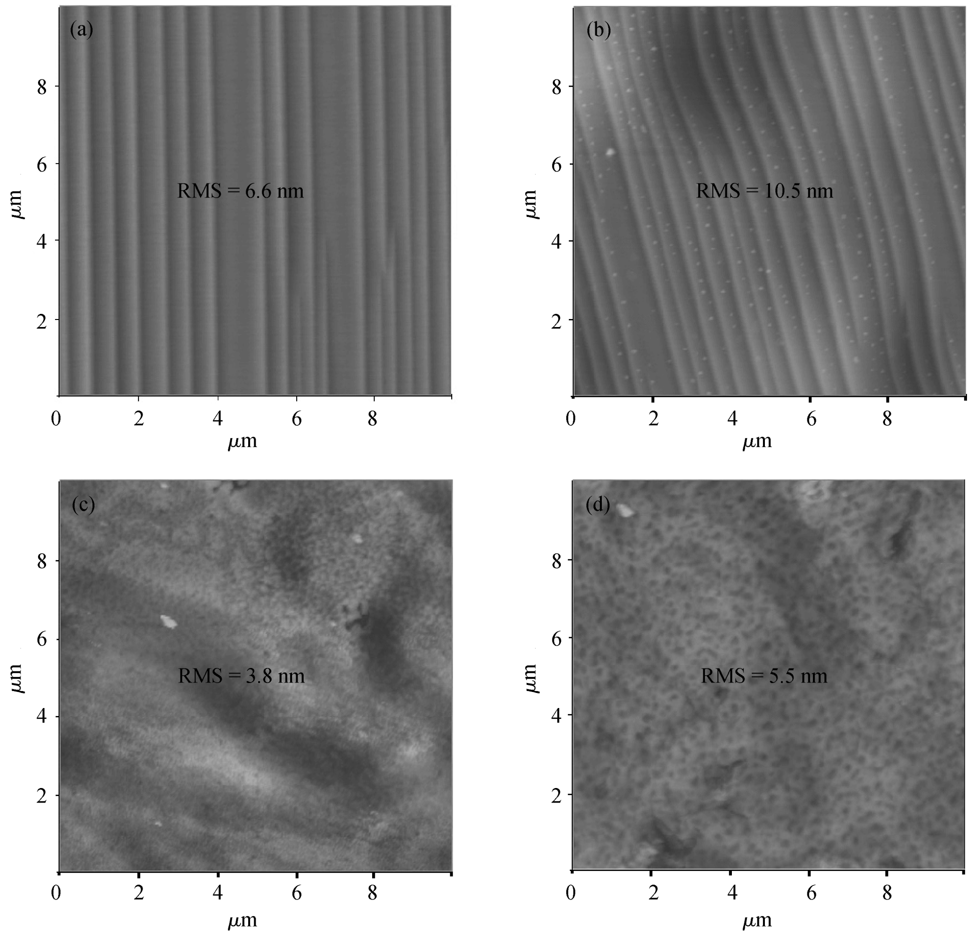

Fig. 3. AFM images of Al-implanted 4H-SiC annealed in argon for 30 min under different conditions. The images are collected following anneals at (a) 1600 ℃ with a SiC capped wafer, (b) 1700 ℃ with a SiC capped wafer, (c) 1600 ℃ with a carbon capped layer and (d) 1700 ℃ with a carbon capped layer.

creased from 12.2 nm (15.0 nm) to 6.6 nm (10.5 nm). However, macrosteps and terraces were also found in the SiC surface. This means that the SiC cap cannot completely prevent Si evaporation. This may be because it cannot form a close contact with the sample surface.

A carbon cap, formed by photoresist, can form a dense barrier layer on the SiC surface, and thereby prevent the evaporation of silicon. As shown in Figs. 3(c) and 3(d), there are no macrosteps and terraces on the SiC surface. Carbon capping is shown to outperform the SiC capping or the sublimation in argon approaches to maintain surface quality, with an RMS roughness for the carbon capping annealed sample being 3.8 nm (5.5 nm).

Electrical characteristics of the SiC, which annealed with a carbon cap, have been performed by Hall-effect measurements. Table 1 shows the free-hole concentration, hole-mobility and resistivity.

Compared with SIMS dates, electrical activation of the dopants was roughly estimated by the ratio of the net acceptor concentration and average implanted-atom concentration. After annealing at 1600 ℃, the electrical activation ratio was only 50%. With the annealing temperature up to 1700 ℃, over 75% of the electrical activation was achieved. The activation ratio with higher temperature will be studied in future work.

Table 1. Electrical characteristics of aluminum-implanted 4H-SiC annealed at 1600 ℃ and 1700 ℃ with carbon capping.

	Resistivity (Ω·cm)	Hole-mobility ($cm^2/(V·s)$)	Free-hole concentration (cm^{-3})
1600 ℃	7.9×10^{-2}	15.1	5.2×10^{18}
1700 ℃	1.02×10^{-2}	10	7.5×10^{18}

4. Conclusions

A study of the 4H-SiC surface morphology of ions implanted and annealed with three different processes has been presented and electrical characteristics were measured by SIMS and Hall-effect measurements. The surface morphology of implanted SiC, before and after annealing, presented significant surface roughening. The RMS value increased from 2.8 to 15 nm. When annealed with a SiC cap, the SiC surface roughness (RMS = 6.6 nm) was dramatically reduced. The implanted SiC, annealed with a carbon cap, maintained a high-quality surface with a RMS roughness as low as 3.8 nm. The dopant profiles of Al, before and after annealing, indicate that the Al atoms undergo no obvious re-diffusion after annealing. With the annealing temperature up to 1700 ℃, over 75% of the electrical activation has been achieved.

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