Two different LNA optimizing techniques

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Abstract: Two different LNA design techniques, namely the classical two-port technique and the Shaeffer technique, have been introduced, compared and implemented for practical design. Their merits and drawbacks are also discussed. This paper mainly focuses on the former technique, which is seldom introduced in traditional papers. Since a parasitic capacitor of the transistor is included in the computation of the former technique, the errors caused by the ignorance of the capacitor have been minimized, which is superior to traditional techniques. Using the former technique, a fully integrated LNA is realized with only 1.4 dB while drawing 1.3 mA DC at 2.4 GHz for simulation results. Another version of the LNA is designed using the latter technique, which has been fabricated.

Key words: LNA; noise optimization; two-port; on-chip inductor

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1. Introduction

Despite the newly emerging radio receiver chain architectures (e.g., passive mixer-first receiver[1]), the low noise amplifier (LNA) is typically the first block after the antenna or the RF filter in most RF applications and, to a great extent, dominates the performance of a radio receiver. A good definition of an LNA is an amplifier that adds minimum noise to the receiver path while providing moderate gain to amplify the varying RF signals and to suppress the noise contributed by subsequent blocks.

The source (emitter) degeneration LNA for a narrow band RF has been paid much more attention due to the best noise performance achievable in the same power dissipation constraint. Many papers have explored different noise optimization techniques. Most of those papers focused on CMOS RF and followed the technique presented by Shaeffer and Lee in 1997[2−4], instead of the classical two-port theory technique. Girlando and Palmisano[5] were the first to introduce an additional capacitor in parallel with the input bipolar transistor in 1999, which simultaneously satisfied noise matching and impedance matching. This architecture is still the most common one in common-source (emitter) LNA design today. In 2001, Andreani[6] theorized the architecture presented by Girlando and Palmisano in CMOS technology, following Shaeffer's technique. In 2002, Goo *et al.*[7] realized an LNA with extremely low noise, only 0.9 dB at 800 MHz. It is remarkable that his optimization technique was based on the concept of noise parameters and the classical two-port technique, which has been ignored for a long time in practical LNA design since the presentation of the noise parameter itself in the classical theory of the two-port system in 1960[8]. In 2004, Nguyen[10] gave a detailed summary of those techniques[9]. In that paper, he derived a series of matching equations that provide a clear insight to LNA designers and allow them to understand the LNA in a more intuitive way. These equations are also based on noise parameters. However, as we will discuss later, both References [7] and [9] neglect the parasitic capacitor C_{gd} (or C_{bc}), which can result in large deviations for bipolar LNAs, because a BJT typically exhibits a larger ratio of C_{bc} and C_{be}, as compared to MOSTs. When the frequency goes higher, however, the deviations are also significant even in CMOS LNAs. In 2006, Belostotski and Sun[11, 12] published their papers, respectively, by taking account of the impact of integrated inductors, realizing that low-Q on-chip inductors have increasingly become a significant noise contributor. In 2007, Belostotski *et al.*[13] realized a sub-0.2 dB noise figure LNA that draws 43 mA DC. This is the lowest noise figure reported to our knowledge. In 2009, Joo *et al.*[14] realized an LNA with resistive feedback. Its performance is quite similar to a source degeneration LNA while having more reliable input matching of resistive feedback topology. The four papers above adopted Shaeffer's technique.

This paper aims to provide a discussion of the two different design techniques, i.e. the classical noisy two-port theory (or noise parameters theory) and Shaeffer's theory, by comparing their merits and drawbacks. We expect that questions about the differences between the two techniques, such as why the latter one is much more common than the former one, will become clear and comprehensive after this paper. On the other hand, most of the papers mentioned above focused on CMOS LNA design. This paper will focus on SiGe BiCMOS technology and can serve as a supplement to LNA design techniques.

2. Classical two-port technique

2.1. Theoretical derivation

Given arbitrary source admittance Y_s (Fig. 1), the noise factor of a noisy two-port can be shown as[15]

$$F = F_{min} + \frac{\overline{v_n^2}}{\overline{i_s^2}}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right], \quad (1)$$

where we have

$$F_{min} = 1 + 2\overline{v_n^2}(G_{opt} + G_c), \quad (2)$$

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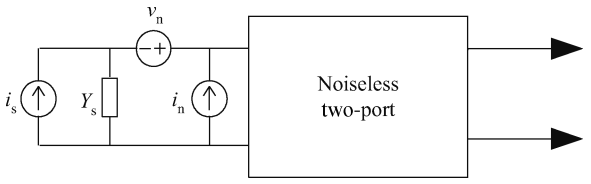

Fig. 1. Linear two-port.

$$G_{\text{opt}} = \sqrt{\frac{\overline{i_u^2}}{\overline{v_n^2}} + G_c^2}, \tag{3}$$

$$B_{\text{opt}} = -B_c, \tag{4}$$

where G_c and B_c are the real and imaginary parts of correlation admittance Y_c of the two-port, respectively. Y_c reflects the correlation between input-referred noise current and noise voltage, i_n and v_n, and can be expressed as $Y_c = i_n/e_n$. Y_c and Y_{opt} are called the noise parameters of the two-port. When the source admittance Y_s is matched to optimum admittance, Y_{opt}, $F_{\min}$ can be acquired.

As shown in Ref. [16], for a single transistor network in common source mode, Y_c can be obtained directly from the definition, namely $Y_c = i_n/e_n$. With correlation coefficient c known, G_{opt} can be calculated, thus enabling calculation of the noise factor. Yet the LNA we discuss here contains at least a source degenerative inductor. The complexity of the correlation between i_n and v_n makes it difficult to directly acquire an analytic expression of Y_c as well as G_{opt}. Nguyen provided an alternative way to calculate noise parameters[7], i.e. to derive F directly from the actual network and then obtain noise parameters by comparing F with the general expression of F in Eq. (1). However, this method will not help to reduce the lengthy computation time. Moreover, neglecting C_{gd} will cause significant error in input admittance, which we will discuss later. To express Y_c in a more useful form, we will derive it from the definition in the form of power spectral density.

$$Y_c = \frac{i_c}{v_n} = \frac{\overline{i_c v_n^*}}{\overline{v_n^2}} = \frac{\overline{i_n v_n^*}}{\overline{v_n^2}}, \tag{5}$$

$$G_{\text{opt}} = \sqrt{\frac{\overline{i_u^2}}{\overline{v_n^2}} + G_c^2} = \sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - |Y_c|^2 + G_c^2} = \sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - B_c^2}. \tag{6}$$

Once we figure out $\overline{i_n^2}$, $\overline{v_n^2}$ and $\overline{i_n v_n^*}$, the noise factor can be evaluated. Figure 2 shows that the noise sources in a bipolar transistor are identical to those in an MOS transistor in structure, although they are generated by different mechanisms (i.e., a BJT exhibits shot noise while an MOST exhibits channel noise and induced gate noise). This identity suggests that i_n and v_n may also be similar to those of MOSTs, except for two differences. First, the two noise sources in MOSTs, channel thermal noise and induced gate noise, exhibit some correlation while there is a neglectable correlation between the two shot noise sources in a bipolar transistor. In fact, the correlation exists even in BJT[16], but can be ignored in our frequency of interest at least (2.4 GHz). Second, the input impedance of an

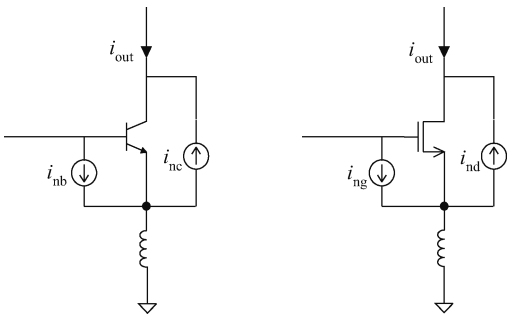

Fig. 2. Comparison of noise sources in a BJT and an MOST.

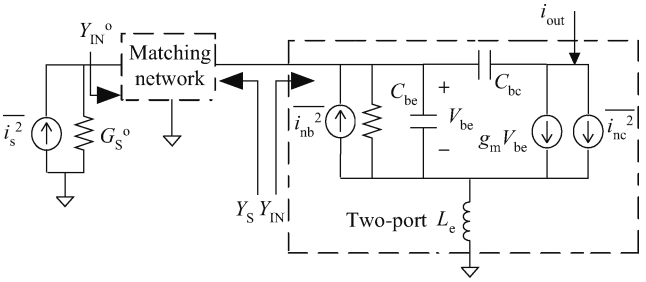

Fig. 3. Small-signal equivalent model for derivation.

MOST is purely capacitive while there is a resistor r_π in parallel with C_{be} in a BJT. This minor difference can be neglected in some cases, however.

Consider the small-signal equivalent in Fig. 3. Notice that we include C_{bc} in the models as well as in the following computations, which is quite different from the traditional method where it is neglected for simplicity. As we will discuss later, neglecting C_{bc} causes significant error in the calculation of input admittance. In addition, a capacitor C_{ex} in parallel with the B–E junction is available if needed. This can be implemented by simply increasing the C_{be} in our model for all practical purposes, although we do not reflect the capacitor explicitly. Actually, this is why we use C_{be} instead of C_π. Indeed, $C_{be} = C_\pi + C_{ex}$. Assuming that the output of the circuit is terminated with the same transistor for the cascode stage as the input transistor, an $1/g_m$ resistor is seen looking up from the output of the two-port. We first reflect the noise sources in the two-port to input-referred noise voltage source and the current source by short-circuiting and opening the input, respectively. Doing so yields

$$\begin{cases} v_{\text{in, i}_{nc}} = i_{nc} Z_{n2}, \\ v_{\text{in, i}_{nb}} = i_{nb} Z_{n1}, \\ i_{\text{in, i}_{nc}} = i_{nc} A_{n2}, \\ i_{\text{in, i}_{nb}} = i_{nb} A_{n1}, \end{cases} \tag{7}$$

where $v_{\text{in, inc}}$ and $v_{\text{in, inb}}$ are input-referred voltage sources caused by collector shot noise i_{nc} and base shot noise i_{nb}, respectively. $i_{\text{in, inc}}$ and $i_{\text{in, inb}}$ are input-referred current sources caused by the same noise sources, respectively. Four coeffi-

cients, namely A_{n1}, A_{n2}, Z_{n1} and Z_{n2}, are defined as

$$\begin{cases} Z_{n2} = \dfrac{(sC_{be} + g_\pi + 1/sL_e)[1 + (sC_i + g_\pi + g_m)sL_e]}{g_m(g_m + g_\pi + sC_{be} + 1/sL_e)}, \\ Z_{n1} = \dfrac{1 + (sC_i + g_\pi + g_m)sL_e}{g_m + g_\pi + sC_{be} + 1/sL_e}, \\ A_{n2} \approx \dfrac{g_\pi + sC_i}{g_m[1 + \lambda(sL_e g_m + 1)]}, \\ A_{n1} \approx 1, \end{cases} \tag{8}$$

which relate the noise sources to the input-referred sources. C_i denotes the input capacitor and is equal to $C_{be} + C_{bc}$. $\lambda = sC_{bc}/(g_\pi + sC_i)$. The approximation is meaningful only if L_e is smaller than 2 nH, which is usually satisfied in the gigahertz frequency range. Now i_n and v_n can be expressed as

$$\begin{cases} v_n = v_{in,\,i_{nb}} + v_{in,\,i_{nc}}, \\ i_n = i_{in,\,i_{nb}} + i_{in,\,i_{nc}}, \end{cases} \tag{9}$$

which can also be expressed in the form of coefficients defined as

$$\begin{pmatrix} v_n \\ i_n \end{pmatrix} = \begin{pmatrix} Z_{n1} & Z_{n2} \\ A_{n1} & A_{n2} \end{pmatrix} \begin{pmatrix} i_{nb} \\ i_{nc} \end{pmatrix}. \tag{10}$$

There is another approximation that must be introduced before we can obtain the expressions of the power spectral densities of i_n, v_n and $i_n v_n^*$, which have been mentioned above: that i_{nc} and i_{nb} are uncorrelated. Readers are referred to Ref. [16] for further theory of their correlation. Here we only adopt the conclusion of the paper.

$$\begin{cases} \overline{i_{nb}^2} = \left[2qI_B + 4qI_C\left(1 - \Re\left\{e^{j\omega\tau_n}\right\}\right)\right]\Delta f \approx 2qI_B\Delta f, \\ \overline{i_{nc}^2} = 2qI_C\Delta f, \\ \overline{i_{nb}^* i_{nc}} = 2qI_C\left(e^{-j\omega\tau_n} - 1\right)\Delta f \approx 0, \end{cases} \tag{11}$$

where τ_n is the transit time and includes both the transit time in the base and in the collector–base junction. I_C and I_B are the DCs of the collector and the base, respectively. According to Ref. [17], τ_n and the base transit time τ_b are of the same order of magnitude, which is picosecond. Taking τ_n as 3 picoseconds yields $e^{-j\omega\tau_n}$ approximates 1 at 2.4 GHz. At present, most simulators adopt the noise model by setting τ_n to zero. For consistency with the simulator, we will employ this model too. In fact, the correlation of the two sources will result in an extremely lengthy calculation. This is the reason why the classical two-port technique is difficult to apply to a CMOS LNA, where there is correlation that can not be ignored. However, as we will see, this problem can be solved by Matlab using a numerical method, which reveals the potential of the technique for CMOS processes.

Setting τ_n to zero yields

$$\begin{cases} \overline{v_n^2}/\Delta f = 2qI_B\left|Z_{n1}\right|^2 + 2qI_C\left|Z_{n2}\right|^2 + 4kTr_b, \\ \overline{i_n^2}/\Delta f = 2qI_B\left|A_{n1}\right|^2 + 2qI_C\left|A_{n2}\right|^2, \\ \overline{i_n v_n^*}/\Delta f = 2qI_B A_{n1}Z_{n1}^* + 2qI_C A_{n2}Z_{n2}^*, \end{cases} \tag{12}$$

where the term $4kTr_b$ in Eq. (12) arises from the lateral voltage drop in base[16]. r_b is a fictitious resistor that accounts for the noise contribution of this effect. Substituting Eq. (12) into Eqs. (4)–(6) yields

$$\begin{aligned} B_{opt} &= -\Im\left\{\frac{2qI_B A_{n1}Z_{n1}^* + 2qI_C A_{n2}Z_{n2}^*}{2qI_B\left|Z_{n1}\right|^2 + 2qI_C\left|Z_{n2}\right|^2 + 4kTr_b}\right\}, \\ G_{opt} &= \left[\frac{2qI_B\left|A_{n1}\right|^2 + 2qI_C\left|A_{n2}\right|^2}{2qI_B\left|Z_{n1}\right|^2 + 2qI_C\left|Z_{n2}\right|^2 + 4kTr_b}\right. \\ &\quad \left. - \left(\Im\left\{\frac{2qI_B A_{n1}Z_{n1}^* + 2qI_C A_{n2}Z_{n2}^*}{2qI_B\left|Z_{n1}\right|^2 + 2qI_C\left|Z_{n2}\right|^2 + 4kTr_b}\right\}\right)^2\right]^{\frac{1}{2}}. \end{aligned} \tag{13}$$

Now, we can obtain the expressions of G_{opt} and B_{opt} by substituting Eq. (8) into Eq. (13). However, these expressions are obviously too long to write as well as to comprehend. Readers are referred to Ref. [16] to reach a simplified version of the optimum admittance for a single transistor network, which is also shown here.

$$\begin{aligned} B_{opt} &\approx -\frac{\omega\left(C_{be} + C_{bc}\right)}{1 + 2g_m r_b}, \\ G_{opt} &\approx \sqrt{\frac{g_m^2}{\beta\left(1 + 2g_m r_b\right)} + \frac{2\omega^2\left(C_{be} + C_{bc}\right)^2 g_m r_b}{\left(1 + 2g_m r_b\right)^2}}, \\ F_{min} &\approx 1 + \sqrt{\frac{1 + 2g_m r_b}{\beta} + \frac{2\omega^2\left(C_{be} + C_{bc}\right)^2 g_m r_b}{g_m^2}}. \end{aligned} \tag{14}$$

However, these equations reveal nothing about how to design a practical LNA with many external passive components. Therefore, only numerical methods are available. The optimum values of the above expressions can be found by sweeping the possible values of the variable with the help of mathematical tools.

2.2. Implementation

From Eq. (1), what we need is the minimum F_{min} available under a given current constraint. Then, by matching source admittance with optimum admittance, the noise factor is optimized to the best noise performance. There are two continuously tunable parameters for the BJTs of a typical BiCMOS process, namely V_{be} and emitter length (or multiplier). With the additional passive components L_e and C_{ex}, and the given power constraint, there are three degrees of freedom for design.

We start our design from F_{min}. For given current constraint, g_m is also fixed by $g_m = qI_c/kT$. Therefore, we should find an optimum emitter length (or multiplier) for F_{min}. Once it is decided, the value of V_{be} is also fixed. Refer to Eq. (14). The optimum value is not so explicit because C_{be} contains an unknown value, C_{ex}. This problem can also be settled by numerical sweeping. Figure 4 shows an example of that. Notice that the multiplier is used instead of emitter length here to ensure that the current is precisely in proportion with the total emitter length. In the contours diagram, the multiplier actually has only a small influence on F_{min}. From 4 to 16 for m, the noise factor has almost no variation. In addition, F_{min} has more dependence on C_{ex}. Therefore, we can choose an arbitrary value of 4–16 for m, while a smaller C_{ex} is preferred, which will be decided later.

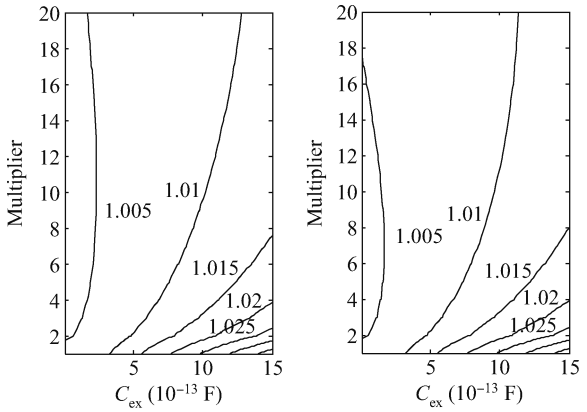

Fig. 4. Noise factor contours versus C_{ex} and m.

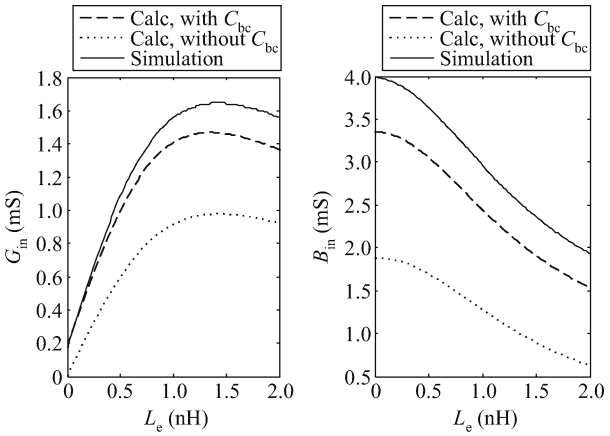

Fig. 5. Comparison of models including and neglecting C_{bc}.

Provided that the value of m and V_{be} are decided, we need to choose different values of C_{ex} and L_e to simultaneously achieve input matching and noise matching. For that purpose, we must ensure $G_{opt} = G_{in}$ and $B_{opt} = -B_{in}$. Thus by matching the source to $G_{opt} + jB_{opt}$, the noise factor is optimized. Recall from Fig. 3. Since we include C_{bc} in our model, the input impedance cannot simply taken be as $Z_{in} = g_m L_e/C_{be} + sL_e + 1/sC_{be}$. Reconsidering Fig. 3 gives us the following input impedance:

$$Z_{in} \approx \frac{1 - \omega^2 L_e C_{be} + sL_e g_m}{(g_\pi - g_m \omega^2 L_e C_{bc}) + s\,(C_{be} + 2C_{bc})}, \tag{15}$$

where the factor 2 of C_{bc} comes from the Miller multiplier of an $1/g_m$ resistor terminated output. As we can expect, by setting $C_{bc} = 0$ and $g_\pi = 0$, Z_{in} degrades back to the familiar one.

Now the input admittance can be written as

$$\begin{aligned} G_{in} &= \Re\{1/Z_{in}\} \\ &\approx \frac{g_m\left[\omega^2 L_e\,(C_{be} + C_{bc}) + \omega^4 L_e^2 C_{be} C_{bc}\right] + g_\pi}{(1 - \omega^2 L_e C_{be})^2 + \omega^2 L_e^2 g_m^2}, \end{aligned} \tag{16}$$

$$\begin{aligned} B_{in} &= \Im\{1/Z_{in}\} \approx \\ &\frac{\omega\left[(C_{be} + 2C_{bc})\left(1 - \omega^2 L_e C_{bc}\right) - g_m L_e\left(g_\pi - g_m \omega^2 L_e C_{bc}\right)\right]}{(1 - \omega^2 L_e C_{be})^2 + \omega^2 L_e^2 g_m^2}. \end{aligned} \tag{17}$$

Figure 5 shows the plot of input admittance versus emitter inductor, including and neglecting C_{bc} in model, respectively. Obviously, both the acceptance (B_{in}) and conductance (G_{in}) of the simplified model deviate significantly from the simulation results, while the deviations are much smaller when C_{bc} is included. The plot of G_{in} shows that g_π also can not be neglected.

This shows the necessity of including C_{bc} in the model.

By comparing the input admittance in Eqs. (16) and (17) with the optimum admittance in Eq. (13), we find it very difficult, if not impossible, to obtain exact analytical expressions of the emitter length and the inductor value. Therefore, numeric methods are again used. In order to find the optimum value of C_{ex} and L_e, we define a function that describes the deviation of the noise factor from F_{min}, namely

$$f_d(C_{ex}, L_e) = (G_s - G_{opt})^2 + (B_s - B_{opt})^2. \tag{18}$$

Provided that the numerical expressions of G_{in}, B_{in}, G_{opt}, and B_{opt} are available from Eqs. (16), (17) and (13), the optimum value of C_{ex} and L_e can be decided by simply sweeping f_d versus C_{ex} and L_e, finding the minimum value of f_d.

Once the value of C_{ex} and L_e are determined, noise matching is completed. Only input and output impedance matching is left. Input matching is easy to achieve. We only need to match the 50 Ω source to Z_{in} (or Y_{in}) by two or three elements, regardless of noise admittance. It can be shown that once the admittance seen looking into the two-port is matched, the admittance seen looking from the source is also matched (i.e., once Y_{in} is matched, Y_{in}^o is also matched).

3. Shaeffer and Lee's technique

As mentioned above, most recent papers and designers use Shaeffer's technique, although in various different forms which are not so explicit. For bipolar transistor LNA, readers are referred to Ref. [5] for detail derivation. The noise factor can be shown as

$$\begin{aligned} F \approx 1 &+ \frac{(r_{b0}/m)\left[1 - \omega^2\,(L_b + L_e)\,C_{ex} + (\omega C_{ex} R_s)^2\right]^2}{R_s} \\ &+ \frac{(g_{m0} m)\,R_s}{2\beta}\left\{1 + \left[\frac{\omega\,(L_b + L_e)}{R_s}\right]^2\right\} + \frac{(g_{m0} m)\,R_s}{2} \\ &\times \left(\frac{\omega}{K\omega_T}\right)^2 + \frac{\left[1 - \omega^2\,(L_b + L_e)\,\dfrac{C_{be0} m + C_{bc0} m}{K}\right]^2}{2\,(g_{m0} m)\,R_s}, \end{aligned} \tag{19}$$

with input impedance matching as a constraint,

$$L_e \omega_T K = R_s, \tag{20}$$

$$\omega^2\,(L_b + L_e)\,\frac{m\,(C_{be0} + C_{bc0})}{K} = 1, \tag{21}$$

and

$$\omega_T = \frac{g_{m0}}{C_{be0} + C_{bc0}}, \tag{22}$$

Table 1. State-of-the-art works in recent years.

Reference	Freq. (GHz)	NF (dB)	DC (mA)	Process
Girlando *et al.*[5]	0.9	1.4[ab]	3.5	Bipolar
Goo *et al.*[7]	0.8	0.9[b]	3.75	0.24 μm CMOS
Nguyen *et al.*[9]	0.9	1.4[b]	1.6	0.25 μm CMOS
Belostotski *et al.*[13]	0.8–1.4	0.2[b]	43	0.09 μm CMOS
Joo *et al.*[14]	2.4	2[c]	2.2	0.13 μm CMOS
This work	2.4	1.4[ac]	1.3	0.18 μm BiCMOS

[a] Simulation result. [b] partially integrated. [c] fully integrated.

$$K = \frac{m\,(C_{be0} + C_{bc0})}{m\,(C_{be0} + C_{bc0}) + C_{ex}}, \tag{23}$$

where all symbols with the subscript 0 are the parameters of one single transistor. For transistors with the multiplier m, those parameters will be multiplied or divided by m, respectively, depending on whether it is conductive or resistive. Notice that K is another parameter that is different from λ, which is used before. Clearly, it is an analytic expression of the noise factor, which is quite different from the one in the classical two-port technique. However, it is the ignorance of C_{bc} that enables the analytic expression. This will introduce some error.

The additional power constraint determines g_m, as mentioned before. It can be expressed as

$$g_m = g_{m0} m = I_c / V_t, \tag{24}$$

with $V_t = kT/q$. Substituting Eqs. (20)–(23) into Eq. (19) eliminates ω_T, K, L_e and L_b. Now we get a function with two variables, namely C_{ex} and m. By simply taking the deviation of Eq. (19) versus C_{ex} and m, respectively, the optimum value is found. This can be done using Matlab.

4. Examples and comparison

Now these design equations, which use two different techniques, can be implemented into practical design. The state-of-the-art works are shown in Table 1. Most of them typically achieved a 2–3 dB noise figure, 2–5 mA current consumption for a single-end LNA at frequency of 1.8–5.8 GHz, or 1–2 dB at lower frequency. Most of these LNAs still use at least one off-chip inductor at the gate or at base of the transistor to achieve input matching. Therefore, the current constraint for an LNA in this paper is set to 1.3 mA, which is quite lower than the state-of-the-art works. Both the on-chip and the off-chip versions are given for comparison. The LNA was designed using NPN transistors of IBM 0.18 μm BiCMOS 7HP technology. All simulations are done in a SpectreRF environment. In addition, a 1.8 GHz fully integrated differential LNA was designed and fabricated under an HH-NEC 0.35 μm SiGe BiCMOS process.

Table 2. Parameters for the BJTs used in the design.

Parameter	Value
I_c	1.28 mA
g_m	46.6 mS
C_μ	49 fF
C_π	125 fF
β_{DC}	271
g_π	178 μS
f_T	48.6 GHz

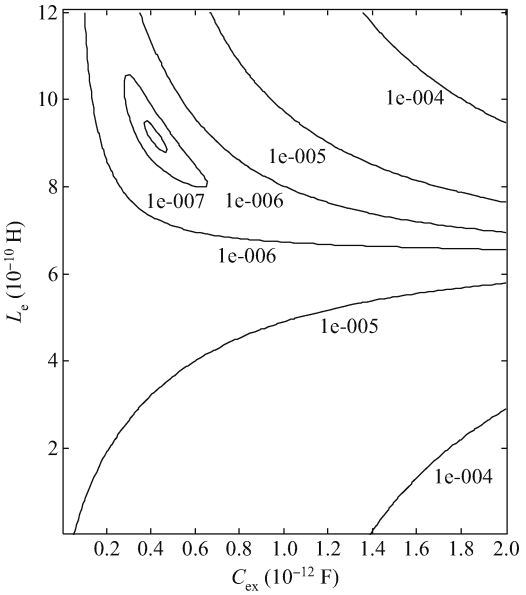

Fig. 6. Contours of f_d versus C_{ex} and L_e.

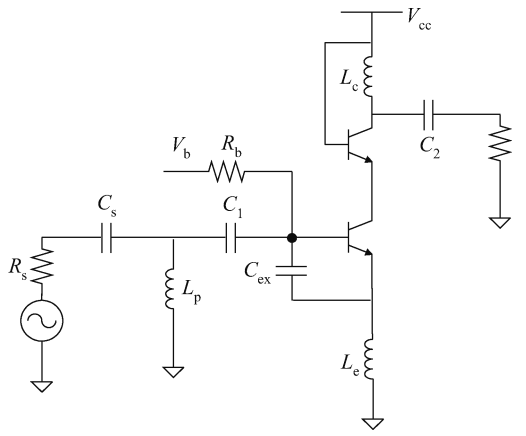

Fig. 7. LNA circuit for the classical two-port technique.

4.1. Classical two-port technique

Under $I_c = 1.3$ mA current constraint, we immediately get $g_m = 50$ mS, where the SpectreRF simulation gives 46.6 mS. The multiplier is chosen to be 10 for a middle value. Now that the transistor is decided, SpectreRF gives the following parameters, shown in Table 2.

With these parameters known, the contour diagram of f_d versus C_{ex} and L_e is available. Figure 6 shows the contours with C_{ex} varying from 0 to 2 pF and L_e varying from 0 to 1.2 nH. These ranges shall cover the number of interest of the de-

Table 3. Practical value of components.

Components	Value 1 (ideal ind)	Value 2 (non-ideal)
L_e (nH)	0.9	1.3
C_{ex} (pF)	0.42	0.21
L_p (nH)	3.8	4.6
C_s (pF)	0.78	0.85
C_1 (pF)	50	50
C_2 (fF)	244	244
L_c (nH)	10.1	10.1
M	10	10

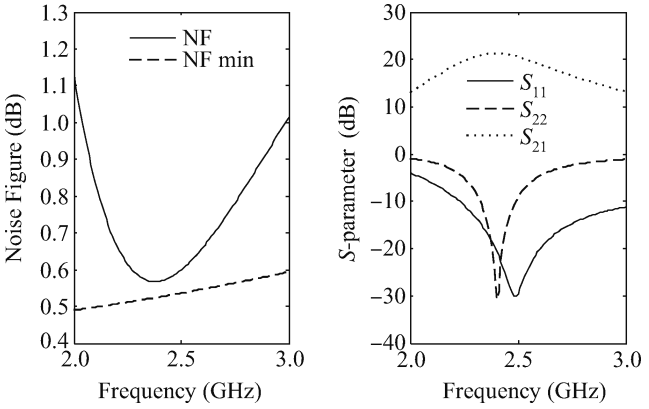

Fig. 8. Simulated results of an ideal inductor LNA for the classical two-port technique.

sign. The smaller value is better for f_d.

The best value is clear from the contours. We can read from the coordinates that L_e is around 0.9 nH and C_{ex} is around 0.4 pF.

SpectreRF gives an input impedance of (58.9 – j 93.3) Ω seen from the base of the input transistor. Therefore, we can match the 50 Ω source with a serial capacitor and a 3.8 nH parallel inductor, which is a acceptable value. With the output matched, the design is complete.

The complete circuit of the LNA is shown in Fig. 7. The practical values of the components are shown in Table 3. These values have been carefully adjusted and simulated many times and are shown to be the best values. It is almost unbelievable that only C_{ex} is slightly different from our calculation, namely $C_{ex} = 0.42$ pF. The other values are precisely equal to the ones we calculated. Notice that C_1 is a DC canceling capacitor and should be as large as possible. This will consume a large area of the layout, which is the drawback of matching topology. The node between C_1 and C_2 suffers from ground noise, however this problem can be settled by using a differential version of this circuit to increase PSRR.

The simulation result is shown in Fig. 8. The noise figure is only 0.56 dB. This is owing to an ideal inductor, of course. The forward gain is about 21 dB.

When the ideal inductors are replaced by on-chip inductors, their best values, also shown in Table 3, are no longer the ones we calculated. The simulation results are shown in Fig. 9, where we can see that the noise figure is much larger, namely 1.4 dB. It is, nonetheless, a good value indeed for a fully integrated LNA.

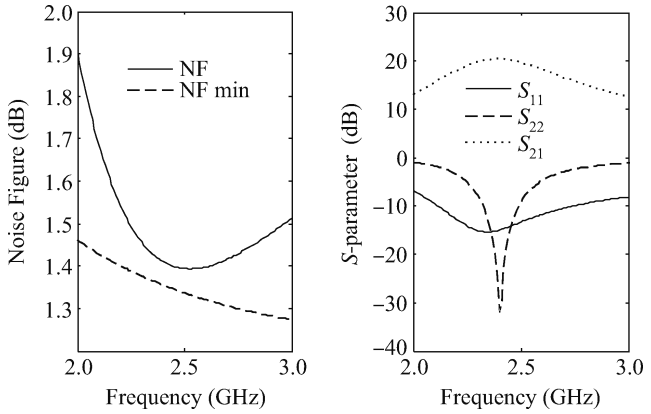

Fig. 9. Simulated results of fully integrated LNA for the classical two-port technique.

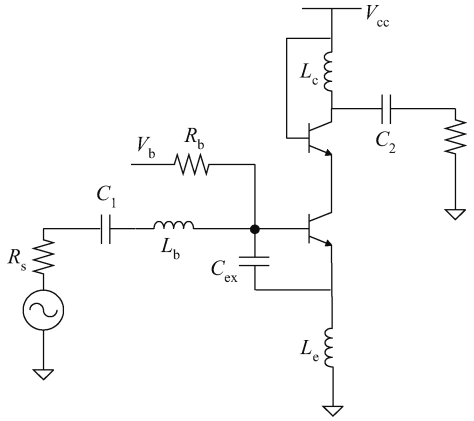

Fig. 10. LNA circuit for Shaeffer's technique.

Table 4. Practical value of the components.

Component	Value 1 (ideal ind)	Value 2 (non-ideal)
L_e (nH)	0.54	0.54
C_{ex} (pF)	0.41	0.36
L_b (nH)	8.4	6.9
C_1 (pF)	50	50
C_2 (fF)	0.24	0.24
L_c (nH)	11	11
m	5	5

4.2. Shaeffer and Lee's technique

Using the method shown in section III and the parameter in Table 2, the values of C_{ex} and m are found to be 0.41 pF and 5, respectively. The other components can be decided by Eqs. (20) and (21), which gives $L_e = 0.53$ nH and $L_b = 8.4$ nH. The circuit is shown in Fig. 10 is a little different in its input matching. Also, C_1 is a DC canceling capacitor that can be implemented off-chip. This will save a lot of area in layout. The practical optimized values are shown in Table 4. Also, these values are almost the same as the calculated ones. The simulated results are shown in Fig. 11, which are identical to those of the previous LNA.

When the inductors are replaced by on-chip inductors, however, the advance of the previous LNA becomes obvious. Since the input matching of the second technique is fixed by

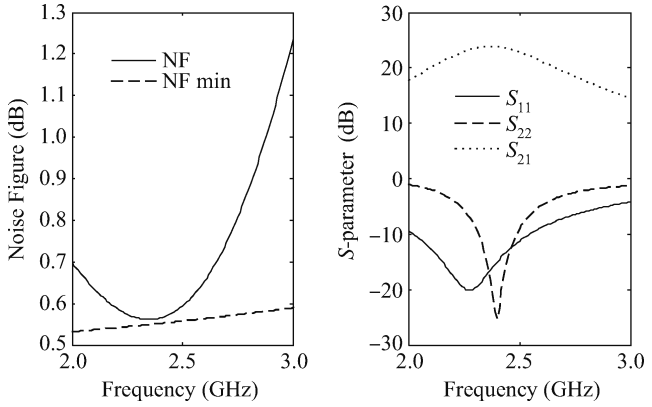

Fig. 11. Simulated results of an ideal inductor LNA for Shaeffer's technique.

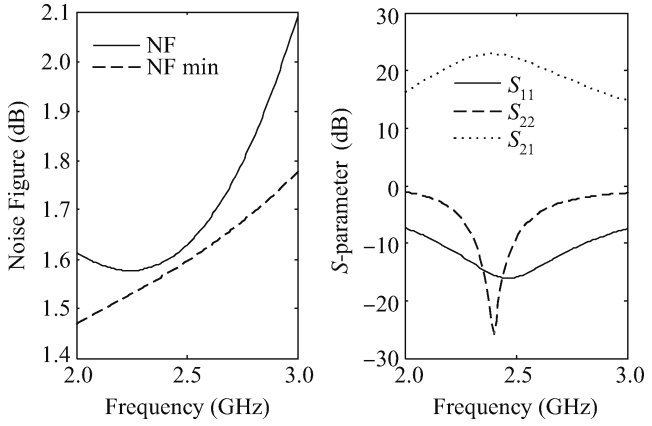

Fig. 12. Simulated results of the fully integrated LNA using Shaeffer's technique.

Eqs. (20) and (21), a larger inductor is unavoidable. The 7 nH inductor at the base of transistor (compared with 4.6 nH of the previous LNA) directly increase the noise figure by 0.2 dB. Figure 12 shows the simulation results.

4.3. Die photo of the LNA

Using Shaeffer's technique, a 1.8 GHz fully integrated differential LNA was designed under an HH-NEC 0.35 μm SiGe BiCMOS process. The die photo of the LNA is shown in Fig. 13. The inductors of that process can not be continuously tunable. This is why there are actually six single inductors with a differential inductor in the real design. The seven inductors are clearly visible in the photo. Figure 14 shows the measurement results. The noise figure is 3.9 dB, which is quite larger than in the simulation (2.4 dB). This problem is mainly caused by the coupling capacitor between the supply and ground, which is not large enough (about 2 pF, parasitic capacitor between V_{cc} and ground only). If we consider the 50 Ω coaxial line and the coupling capacitor as an RC filter, it gives a cutoff frequency of only 1.6 GHz. Clearly that is not enough to completely filter out the noise from the power supply at 1.8 GHz. This can be proved by observing the noise plotting in Fig. 14. The noise figure is very large before 1 GHz, while it is only moderately large after 2 GHz, which is mainly caused by the insufficient power gain of the LNA, not by the power supply.

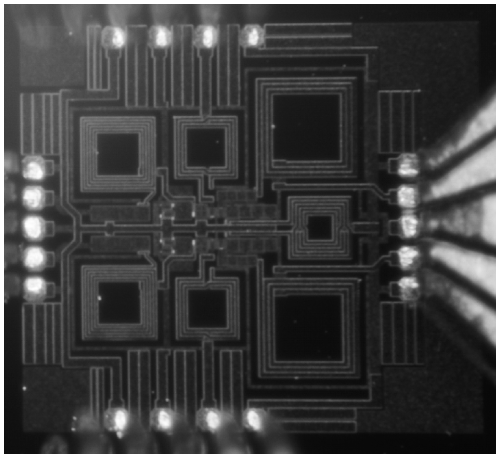

Fig. 13. Die photo of the LNA using Shaeffer's technique.

Table 5. Simulation and measurement result summary.

Term	Post-simulation result	Measurement result
DC (mA)	4	4.3
S_{11} (dB)	–35	–27
S_{21} (dB)	11.3	10.7
S_{22} (dB)	–15.5	–11.1
IIP3 (dBm)	–7.5	–6.3
P_{1dB} (dB)	–16	–15.3
NF (dB)	2.4	3.9

Table 5 gives a summary and comparison of LNA performance between the post-simulation and measurement result.

4.4. Discussion and comparison

As a final summary, we will compare the two techniques from the view of designers.

According to Eq. (1), by matching F to F_{min}, the source admittance will in theory not affect the noise factor at all. This is the major advance of the classical two-port technique as compared to the Shaeffer's technique. It means that we can achieve noise matching first and then impedance matching, instead of achieving the two simultaneously, which usually makes it difficult for designers to decide the trade-off. Moreover, it also suggests that more flexible input matching plans are available. In other words, we can choose either two or three matching components according to different situations. This flexibility is very important for integrated inductors. Indeed, fully integrated LNAs suffer a lot from the noise contributed by the large inductors used for input matching. These inductors are as large as 5–15 nH for a typical value or even reach 36 nH at lower frequency[7], which is impossible to be integrated. However, now, with the help of three matching components, we can replace them with smaller ones or change the matching topology. Either will help to reduce noise. In addition, it provides more intuitive design guidance to designers with regard to noise parameters. The process of noise optimizing now becomes the process of optimum admittance matching, which can be done by numerical methods. Input matching can be achieved after noise matching.

However, one of the major advances is also a drawback.

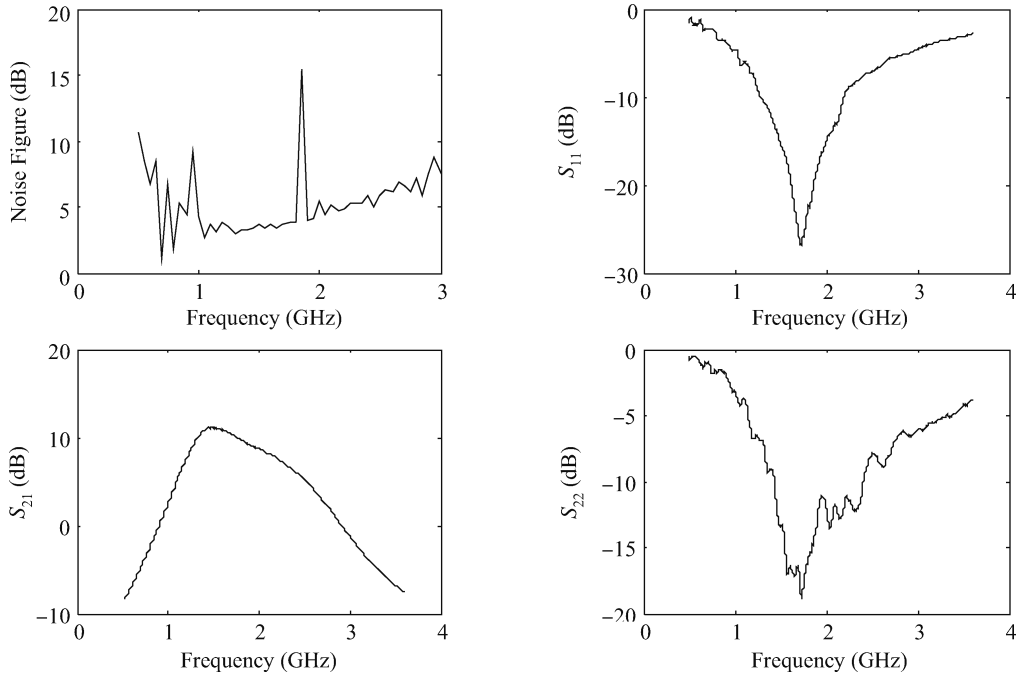

Fig. 14. Measured results of the LNA.

More complicated matching topology also makes it difficult to predict the variance of input impedance using the Smith Chart diagram. Moreover, we lack an analytic expression from the very beginning to the end, which makes it difficult to observe the varying trend of any parameter versus any other one. However, once C_{bc} is neglected, the analytical expressions are available, at least for an approximate version. This should not be a major problem for CMOS LNAs, as the ratio of C_{gd} and C_{gs} is smaller compared to BJTs. Instead, it is the correlation between channel noise and induced gate noise that causes the technique to be seldom applied to CMOS processes. We think this problem could be settled by numerical methods in the same way, though we do not show it in this paper.

Shaeffer's technique is still useful today. Although the technique relies heavily on mathematical derivations, it gives a direct relation between the power constraint and circuit design, which is very convenient for designers to quickly evaluate an LNA's performance. In addition, by neglecting C_{gd}, an approximate analytic expression of the noise figure is available, which means that these design equations can be amended according to different situations and demands. Actually, many designers have published many improved versions of the technique. References [11] and [12] are examples of that, by taking parasitic resistor of on-chip inductors into account.

The major disadvantage of this technique should be input matching problems, as the optimizing process usually results in an unacceptably large L_g. In fact, at the time of Shaeffer's paper (1997), most receiver front-ends employed superheterodyne architecture, usually with off-chip inductors to ensure good performance. Therefore, a large L_g does not matter at all. At present, zero-IF and low-IF with fully integrated inductors are more common. So the problem continues. However, as mentioned above, more and more papers have begun to include the parasitic effect of inductors in the optimizing process, thus demonstrating the potential of the technique.

5. Conclusion

Two different LNA design techniques have been introduced, compared and implemented for practical design. Their merits and drawbacks were also discussed. Since C_{bc} is included in the small-signal model, more accurate computation is available, as compared to traditional methods. Using the classical two-port technique, we have realized a fully integrated LNA with very good performance, which achieves a 1.4 dB noise figure while consuming only 1.3 mA DC.

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