A 102-dB-SNR mixed CT/DT ΣΔ ADC with capacitor digital self-calibration for RC spread compensation

Liu Yan(刘岩)†, Hua Siliang(华斯亮), Wang Donghui(王东辉), and Hou Chaohuan(侯朝焕)

Institute of Acoustics, Chinese Academy of Sciences, Beijing 100190, China

Abstract: This paper provides a mixed continuous-time/discrete-time, single-loop, 4th-order, 4-bit audio-band sigma delta ADC with capacitor digital self-calibration for RC spread compensation. This ADC combines the benefits of CT and DT circuits, and the self-calibration control circuits compensate for the variation of the RC product in the continuous-time integrator and for variation in the sampling frequency. Measurement results show that the peak SNR of this ADC reaches 102 dB and the total power consumption is less than 30 mW.

Key words: continuous-time; discrete-time; self-calibration; sigma delta ADC
DOI: 10.1088/1674-4926/32/8/085004 **EEACC:** 1265H; 6130

1. Introduction

Sigma delta (ΣΔ) ADCs provide a means to achieve high resolution and low distortion at a relatively low cost compared to Nyquist converters. The high resolution is achieved by oversampling the input signal and shaping the quantization noise in the band of interest into a higher frequency region. The higher frequency noise can then be digitally filtered out by the subsequent digital filter stages. The resulting data is then down sampled to the desired sample rate at the output of the converter[1].

Typically, an audio-band sigma delta ADC is implemented using discrete-time (DT) circuits such as switched capacitors, because switched capacitor circuits offer low sensitivity to clock jitter and are readily scalable with the sampling rate[2]. However, due to the nature of DT, the converter suffers from harmonic distortion primarily caused by signal-dependent glitches captured by the sampling capacitors of the first integrator. Furthermore, for high performance converters, the sampling capacitors of the first integrator have to be large in order to reduce the thermal noise and therefore need a driver in front of the first integrator to load the sampling capacitors. Instead of implementation by switched capacitors, the first integrator can be implemented using a continuous-time (CT) integrator. A CT integrator has significant advantages over a DT integrator, notably an implicit anti-aliasing filter, no front-end sample and hold S/H, and the absence of kT/C noise[3].

A major drawback associated with the combination of CT and DT implementation is that the RC time constant in the continuous-time integrator varies significantly with process, temperature and power supply variation. Variation in the RC product changes the noise transfer function of the loop and leads to a degradation in performance of the converter. Another disadvantage is that the RC time constant also changes with the period of the master clock of the converter. This essentially limits the converter operation to one particular sampling rate.

So this paper provides a mixed CT/DT audio-band sigma delta ADC with capacitor digital self-calibration for RC spread compensation. This ADC combines the benefits of CT and DT circuits, and the self-calibration control circuits compensate for the variation of the RC product in the continuous-time integrator and for variation in the sampling frequency. The ADC uses chopper stabilization; the IDAC can be connected to the branches via chopping switches and the integrator amplifier can also be chopper-stabilized. Chopper stabilization can remove the flicker noise especially problematic in deep submicron MOS devices[4].

2. Mixed CT/DT audio-band sigma delta ADC

An audio-band ΣΔ ADC requires a set of two transfer functions: high-pass noise transfer function (NTF) and low-pass signal transfer function (STF). The architecture of the mixed CT/DT, single-loop, 4th-order, 4-bit, audio-band ΣΔ ADC with capacitor digital self-calibration is shown in Fig. 1.

This architecture allows for good control of the NTF as well as for good control of STF by using the feedback coefficient c_1 and the feed-forward coefficients b_1, b_2, b_3, b_4. No feed-forward coefficient is connected at the input of the modulator, leaving only the first CT integrator to load the audio input. The integrator coefficients a_1, a_2, a_3, a_4 can be chosen as freedom degrees so the designer can control these integrator's outputs within 20% to 80% of the voltage between ground and the supply voltage when the ADC is not overloaded. Only one feedback path connected to CT integrator is used in this architecture. The feedback path for the CT integrator can be implemented with current sources, which do not need reference voltages and voltage buffers.

A digital decimation filter decimates and filters the high-speed data stream of the modulator's output, attenuates the noise outside of the input signal bandwidth and changes the modulator output sampling frequency down to the signal Nyquist frequency. The circuit complexity of the digital decimation filter is decided by its pass-band ripple coefficients, stop-band attenuation coefficients and transition zone width. In this paper, we design a digital decimation filter using a cascaded integrator comb (CIC) filter, a compensation filter and two half-band filters that are cascaded together.

In baseline deep-submicron CMOS technology, RC time

† Corresponding author. Email: liuyan@mail.ioa.ac.cn
Received 25 February 2011, revised manuscript received 30 March 2011

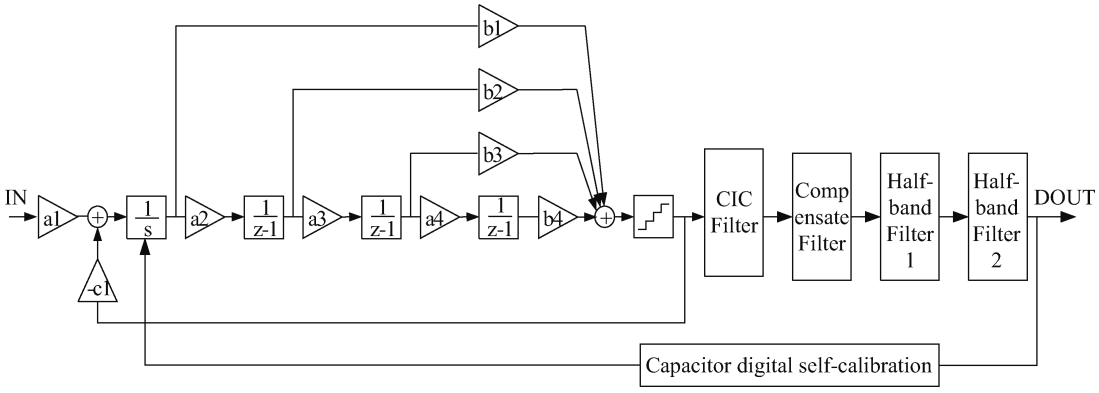


Fig. 1. Mixed CT/DT audio-band sigma delta ADC architecture.

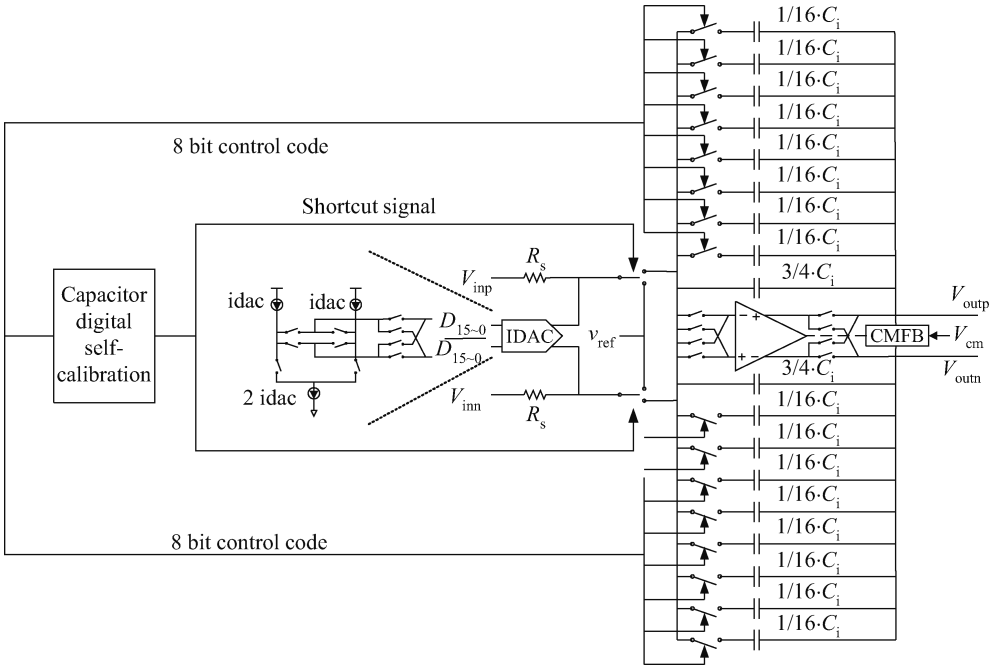


Fig. 2. First order CT integrator.

Table 1. Architecture comparison.

Parameter	Ref. [4]	Ref. [3]	Ref. [2]	This work
Architecture	Full-DT	Mixed CT/DT	Full-DT	Mixed CT/DT
Chopper-stabilization	Yes	No	No	Yes
Quantizer	4 bit DAC	4 bit DAC	5 bit DAC arrays	4 bit DAC
Calibration	Dynamic element matching	No	DSP calibration	Capacitor digital self-calibration

constant in the first CT integrator varies significantly with process, temperature and the period of the converter clock. The RC time constant variations modify the ΣΔ ADC output spectrum in two different ways. Firstly, when the RC time constant is too large, the quantization noise shifts to the bandwidth and reduces the signal-to-noise ratio (SNR) performance. Secondly, when the RC time constant is too small, the loop filter becomes unstable because the noise transfer function is too aggressive. In both situations, the in-band noise increases and, consequently, the SNR decreases. Capacitor digital self-calibration means are provided in this paper. The means are arranged to estimate the band noise (IBN) from the filtered digital signals and modify the value of the first integrator capacitor until the IBN reaches minimum.

Table 1 shows architecture comparison between different designs and this work.

3. Circuit design

3.1. CT integrator

An active-RC circuit is used for the first CT integrator, which is shown in Fig. 2. This should be preferred for high-linearity applications since the operational amplifier holds the

voltage between its inputs ideally equal, turning the R_s resistors into linear voltage-to-current converters. The DAC of this CT integrator is implemented as a set of 16 current sources controlled by a thermometer-coded, 16-bit word supplied by the quantizer. The variable capacitance means consists of 8 couples connected in parallel and each comprising a capacitor, with a chosen capacitance, and a two-sate switch mounted in series with the capacitor. Each two-state switch is controlled by one bit value of the control word generated by a CDS module[6].

A 4-bit feedback current digital-to-analog (IDAC) generates a 16-level feedback current which depends on the 16-bit feedback signal supplied by the quantizer. An integrator integrates a sum of the generated current and the input signal current on a continuous-time basis. The IDAC has a first output branch including a first biasing current source and a second output branch including a second biasing current source. The biasing current sources supply a bias current to a respective branch of the IDAC to bias the input stage. The biasing current sources are connected to the branches via chopping switches which alternately connect the biasing current sources to the branches in a first configuration and a second, reversed, configuration. Additionally, the integrator amplifier can also be chopper-stabilized.

The amplifier differential inputs are connected via chopping switches. The outputs are also chopped via chopping switches. The polarity within the amplifier alternates during each of the two cycles of operation. This has the effect of swapping the inputs and outputs between alternate cycles. The chopping switches within the amplifier and IDAC can operate over a wide range of clock rates. In general, the chopping switches can operate at the same rate as the main clock for the sigma delta modulator or at binary subdivisions of the modulator clock rate.

The R_s, C_i, and I_{dac} of the first CT integrator can be calculated according to the integrator coefficients a_1, c_1 and the conversion from DT to CT. The conversion formula from DT to CT is shown as

$$H(z) = \frac{1}{z-1} \Rightarrow H(s) = \frac{f_{clk}}{s}, \tag{1}$$

where f_{clk} denotes the DT integrator sampling frequency. The transfer function of the DT integrator and the conversion from DT integrator to CT integrator is calculated as

$$\begin{aligned} Y(z) &= \frac{a_1}{z-1}X(z) \pm \frac{c_1}{z-1}E(z) \\ &\Rightarrow \begin{cases} H_X(z) = \dfrac{a_1}{z-1} \Rightarrow H_X(s) = \dfrac{a_1 f_{clk}}{s}, \\ H_E(z) = \dfrac{c_1}{z-1} \Rightarrow H_E(s) = \dfrac{c_1 f_{clk}}{s}. \end{cases} \end{aligned} \tag{2}$$

With an ideal operational amplifier, the transfer function of the first CT integrator is

$$\begin{aligned} \frac{V_{in}}{R_s} \pm I_{dac} &= C_i \frac{dV_{out}}{dt} \\ &\Rightarrow \begin{cases} H_X(s) = \dfrac{1}{sR_sC_i}, \\ H_E(s) = \dfrac{I_{dac}}{sC_i}. \end{cases} \end{aligned} \tag{3}$$

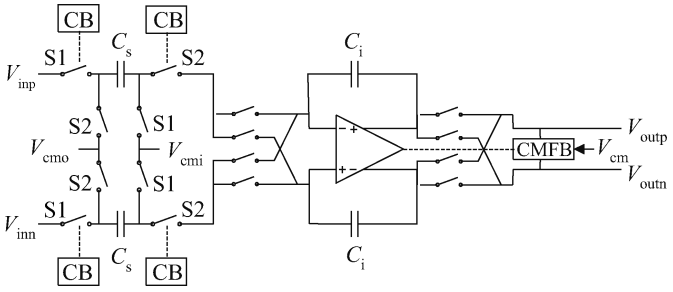


Fig. 3. Higher order SC integrators.

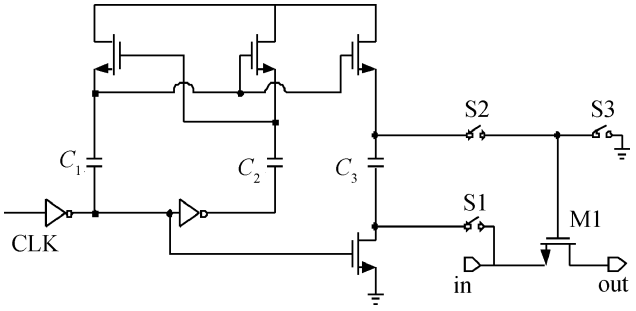


Fig. 4. Clock bootstrap circuit.

According to Eqs. (2) and (3), the R_s, C_i, and I_{dac} can be calculated by

$$R_s = \frac{1}{a_1}\frac{1}{C_i f_{clk}}, \tag{4}$$

$$I_{dac} = \frac{c_1}{a_1}\frac{1}{R_S} = c_1 C_i f_{clk}. \tag{5}$$

The nine capacitors mounted in parallel together offer a maximum capacitance value equal to 5/4 of a starting capacitance C_i. The first of the nine capacitors has a value equal to 3/4 of the starting capacitance, each one of the eight other capacitors has a value equal to 1/16 of the starting capacitance. The CDS module may be arranged to generate a control word having a first value corresponding to a first capacitance equal to a chosen starting capacitance C_i with a chosen increase step $C_i/4$. The starting capacitance C_i may correspond to a given spread of the integrator RC product, the chosen increase step $C_i/4$ may be equal to 25% of the starting capacitance. The decrement may be equal to $C_i/16$ of the starting capacitance, depending on the process variation value, temperature spread and the final targeted accuracy[6].

3.2. SC integrator

The higher-order integrators are fully differential switched-capacitor (SC) circuits, which are shown in Fig. 3. They consist of sampling capacitors C_s, integrating capacitors C_i and an operational amplifier.

One advantage of the SC integrator is the decoupling of the input signal common-mode V_{cmi} and the operational amplifier common-mode input V_{cmo}. The two values, V_{cmi} and V_{cmo}, are independently set with V_{cmi} tied to the middle of the supply voltage to take advantage of the rail-to-rail output capability of

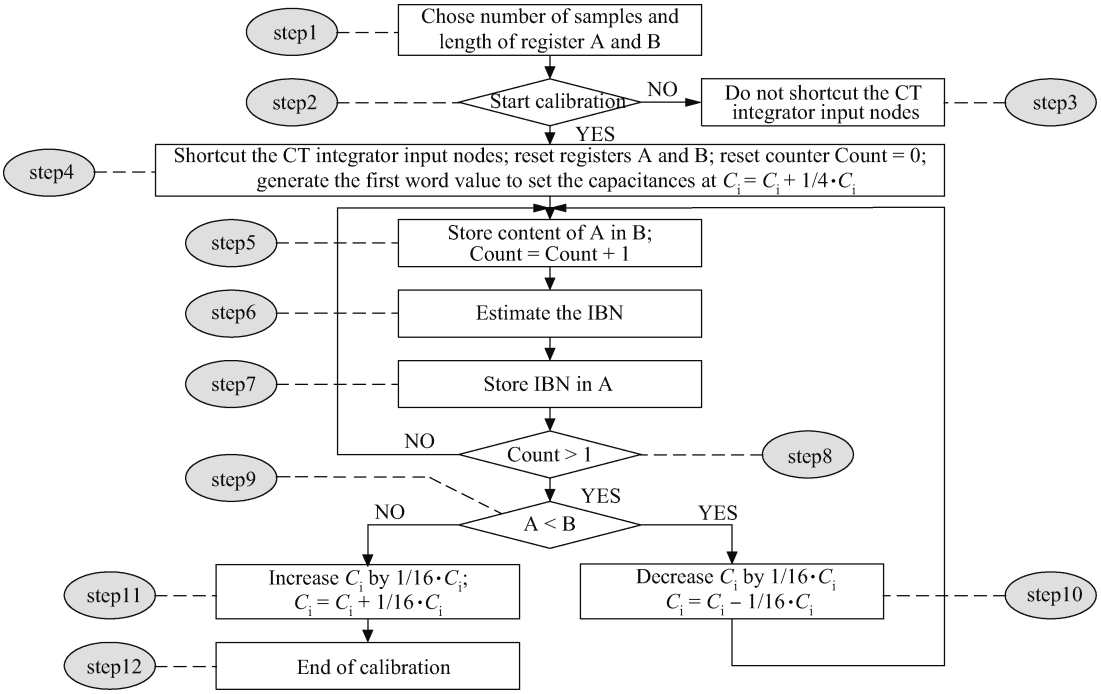


Fig. 5. Capacitor digital self-calibration algorithm.

the previous integrator while V_{cmo} has a low value falling inside the common-mode input range of the PMOS-input amplifier. Another advantage of the SC integrator is the good control of capacitor ratios. In a sigma delta modulator, the better control of each path gain means that the decrease of the modulator performance can be minimized due to the impact of coefficient deviation.

Because the modulator has only one feedback path connected to the CT integrator, the higher-order SC integrators are designed simply and do not need feedback sampling capacitors or reference voltage.

In order to suppress distortion and noise, the sampling switches have to offer a low on-resistance during the sampling phase. Through the clock bootstrap circuit in Fig. 4, the gate-to-source voltage of transistor M1 is bounded within V_{DD} in the sampling phase, and hence the on-resistance of the sampling switch is linear, so reducing the signal distortion.

3.3. Capacitor digital self-calibration

The CDS algorithm arranged:

(1) To generate a first control word. (2) Then to estimate in-band noise IBN(n) from the filtered digital signals and to compare this in-band noise IBN(n) to the preceding in-band noise IBN($n-1$). (3) Then to modify the value of the control word in order to decrease the capacitance of the CT integrator when IBN(n) is small than IBN($n-1$). (4) Then to iterate steps (2) and (3) till IBN(n) is equal to or greater than IBN($n-1$), and to choose as a calibration control word value the value corresponding to the preceding in-band noise IBN($n-1$) in order to set the calibration state of the variable capacitance means.

The IBN is estimated by calculating the variance P_Q of the filtered digital signals cm $\pm$ dm(n), defined by the following relation:

$$P_Q = \frac{1}{N_S}\sum_{n=0}^{N_S-1}|\mathrm{cm} \pm \mathrm{dm}(n)|^2 - \left|\frac{1}{N_s}\sum_{n=0}^{N_S-1}[\mathrm{cm} \pm \mathrm{dm}(n)]\right|^2, \quad (6)$$

where N_S is the number of samples used for estimation of IBN.

A more detailed CDS algorithm is described with reference to Fig. 5.

In the preliminary starting step 1, one specifies the number N_s and the length of two registers, A and B respectively, intended for storing the current IBN estimate and the preceding IBN estimate.

In step 2, the digital capacitor self-calibration module (CDS) carries out a test to determine whether a calibration must be started or not. If there is no need to start the calibration, then the calibration algorithm ends in step 3, in which the CDS may decide not to shortcut the differential input nodes.

If the calibration must be started, then in step 4, the CDS may start shortcutting the differential input nodes. Then the CDS resets the value of registers A and B and the value of a counter, and generates a control word with a chosen first value. The first value of the control word sets the capacitance value of variable capacitance means to $5C_i/4$.

In step 5, the CDS stores the value of register A in register B, and increments the value of the counter by 1.

In step 6, the CDS estimates the IBN from the filtered digital signals.

In step 7, the CDS stores the estimated IBN value in register A.

In step 8, the CDS carries out a test to determine if the value of the counter is greater than 1. If this counter value is smaller than 1, then the CDS comes back to step 5.

If the counter value is greater than 1, then the CDS carries out another test in step 9 to determine whether the value stored

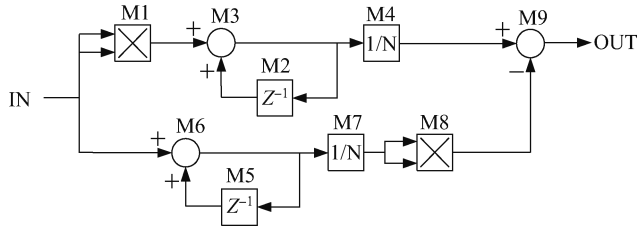
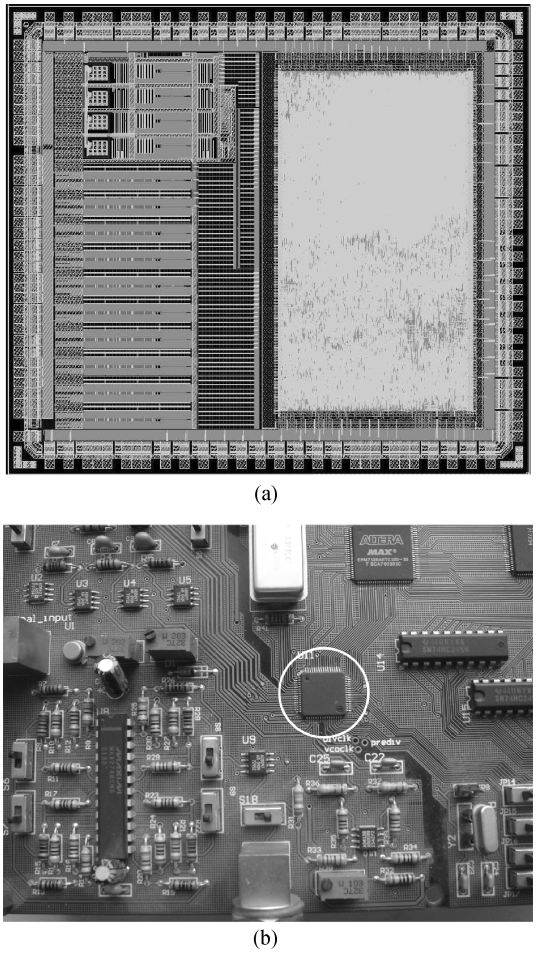


Fig. 6. Hardware implementation of the CDS algorithm.



(a)

(b)

Fig. 7. (a) Layout of mixed CT/DT audio-band sigma delta ADC. (b) Test board of mixed CT/DT audio-band sigma delta ADC.

in register A is smaller than the value stored in resister B. If the A value is smaller than the B value, this means that the final calibration value has not been found yet. Then the CDS carries out step 10, in which it modifies the value of the control word generated last in order to decrease the current capacitance value C_i from a chosen decrement $C_i/16$. So each new capacitance value C_i becomes equal to $C_i - C_i/16$. Then the CDS comes back to step 5 for a new iteration.

If the A value is greater than the B value, this means that the calibration value has just been passed. Then the CDS carries out step 11, in which it chooses the value that corresponds to IBN($n-1$), stored in register B, as the final calibration value of the control word. So it generates the final calibration value and the calibration algorithm ends at step 12.

In order to implement such a variance computation, the

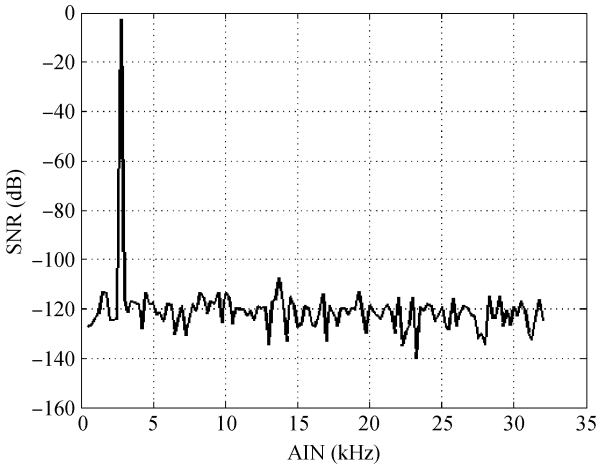


Fig. 8. FFT spectrum with –3 dBFS 3.35 kHz input.

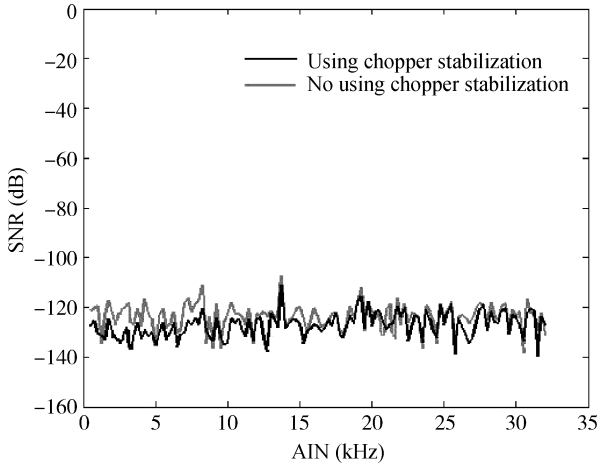


Fig. 9. FFT spectra with noise.

CDS module is as shown in Fig. 6. The M1–M4 determine the first member of the right part of the relation (P_Q) cited above, the M5–M8 determine the second member of the right part of the relation cited above and the combiner M9 subtracts the value provided by M5–M8 of the second branch from the value provided by M1–M4 of the first branch.

4. Layout and results

The mixed CT/DT audio-band ΣΔ ADC is fabricated in an SMIC 0.18 μm one-poly four-metal CMOS process. The chip area is approximately 2×2 mm^2. The whole ADC chip is shown in Figs. 7(a) and 7(b). The ADC chip includes a mixed CT/DT modulator, the digital decimation filter and capacitor digital self-calibration circuits.

Figure 8 shows FFT plot with a –3 dBFS 3.35 kHz input. The SNR is measured to be around 100 dB. Figure 9 shows the FFT plots with noise between using and no using chopper stabilization. The flicker noise of the ADC using chopper stabilization is lower than that not using chopper stabilization. Figure 10 shows the measured SNR and signal noise distortion ratio (SNDR) for a 3.35 kHz input signal.

An example of calibration is illustrated in Fig. 11. The example corresponds to a RC spread of 20%. The calibration

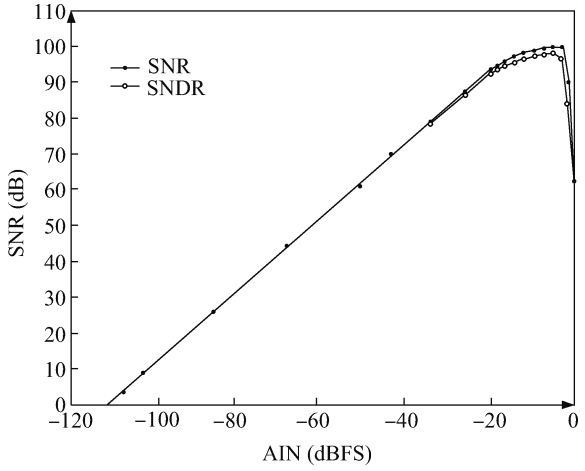


Fig. 10. The measured SNR and SNDR.

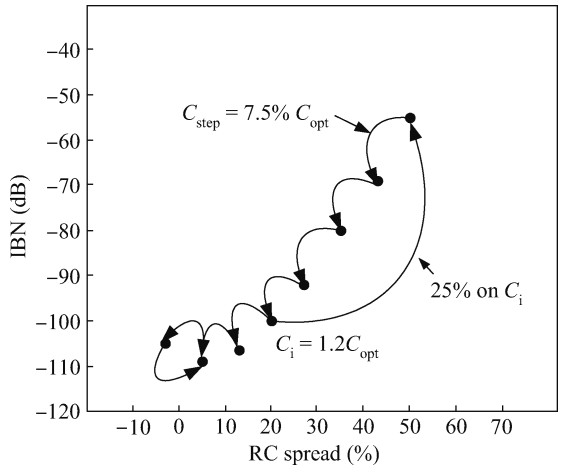


Fig. 11. An example of calibration.

starts with a 25% increase of the starting capacitance C_i and is followed by seven iterations, each corresponding to a decrease of the current C_i value by a decrement $C_{step} = 1/16$, $C_i = 7.5\%C_{opt}$, and ends by an increase of the C_i value by an increment C_{step}. Within the variation of the RC spread of $\pm$ 25%, the algorithm can calibrate it to an appropriate value.

Figure 12 shows the measured SNR for a 3.35 kHz input signal with and without using the capacitor digital self-calibration algorithm. The proposed calibration algorithm can compensate for the variation of the RC product in the CT integrator and improve of SNR. The peak SNR of 102 dB is achieved in a 20 kHz signal bandwidth.

The figure of merit (FOM) of the converter is determined as

$$\mathrm{FOM_{SNR}} = \frac{P}{2 \times f_B \times 2^{(\mathrm{peakSNR}-1.76)/6.02}}, \qquad (7)$$

where P, f_B, peakSNR, denote the power consumption, signal bandwidth and peak SNR, respectively.

Table 2 shows a performance comparison between different designs and this work. The mixed CT/DT audio-band sigma delta ADC of this work operates at 20 kHz signal bandwidth with 30 mW power dissipation and achieves $\mathrm{FOM_{SNR}}$ = 7.29 pJ.

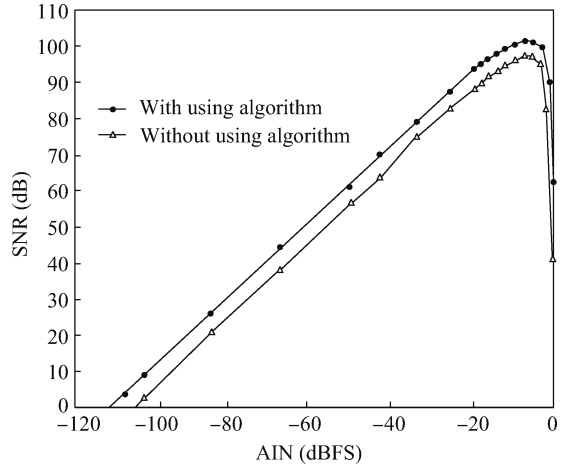


Fig. 12. The measured SNR with and without using algorithm.

Table 2. Performance comparison.

Reference	Ref. [4]	Ref. [3]	Ref. [2]	This work
Tech. (μm)	0.35	0.18	0.18	0.18
f_B (kHz)	20	20	20	20
Power (mW)	68	37.3	34.7	30
Peak SNR (dB)	105	102	107.4	102
SNDR (dB)	100	95	102	99
$\mathrm{FOM_{SNR}}$ (pJ)	11.69	9.06	4.53	7.29

5. Conclusion

Measurement results show the mixed CT/DT audio-band sigma delta ADC offers a better SNR and lower power consumption. With such competitive advantages, the mixed CT/DT audio-band sigma delta ADC will become a preference in new audio-band ADC implementations.

References

[1] Rabii S, Wooley B A. The design of low-voltage, low-power sigma–delta modulators. Boston: Kluwer Academic Publisher, 1999

[2] Wu J Y, Zhang Z Y, Subramoniam R. A 107.4 dB SNR multi-bit sigma delta ADC with 1-PPM THD at −0.12 dB from full scale input. IEEE J Solid-State Circuits, 2009, 44(11): 3060

[3] Morrow P, et al. A 0.18 μm 102 dB-SNR mixed CT SC audio-band ADC. IEICE Tech Rep, 2005, 105(96): 35

[4] Yang Y Q, Chokhawala A. A 114-dB 68-mW chopper-stabilized stereo multibit audio ADC in 5.62 mm^2. IEEE J Solid-State Circuits, 2003, 38(12): 2061

[5] Ortmanns M, Gerfers F, Manoli Y. On the synthesis of cascaded continuous-time $\Sigma\Delta$ modulators. IEEE International Symposium on Circuits and Systems, 2001, 5: 419

[6] Cherry J, Snelgrove W M. Continuous-time delta–sigma modulators for high-speed A/D conversion. Kluwer Academic Publishers, 2000