Design of 700 V triple RESURF nLDMOS with low on-resistance*

Yin Shan(银杉)[1,2,†], Qiao Ming(乔明)[1], Zhang Yongman(张永满)[1], and Zhang Bo(张波)[1]

[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China
[2]School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, 639798, Singapore

Abstract: A 700 V triple RESURF nLDMOS with a low specific on-resistance of 100 mΩ·cm^2 is designed. Compared with a conventional double RESURF nLDMOS whose P-type layer is located on the surface of the drift region, the P-type layer of a triple RESURF nLDMOS is located within it. The difference between the locations of the P-type layer means that a triple RESURF nLDMOS has about a 30% lower specific on-resistance at the same given breakdown voltage of 700 V. Detailed research of the influences of various parameters on breakdown voltage, specific on-resistance, as well as process tolerance is involved. The results may provide guiding principles for the design of triple RESURF nLDMOS.

Key words: nLDMOS; triple RESURF; breakdown voltage; specific on-resistance; charge sharing
DOI: 10.1088/1674-4926/32/11/114002 **EEACC:** 2560

1. Introduction

To improve the breakdown voltage (BV) of a lateral double-diffusion MOSFET (LDMOS), conventionally the drift length (L_{d}) is increased. However, this greatly increases the specific on-resistance ($R_{\mathrm{on.\,sp}}$), as Equation (1) illustrates[1].

$$R_{\mathrm{on.\,sp}} \propto \frac{L_{\mathrm{d}}^2}{Q_{\mathrm{epi}}}. \tag{1}$$

In Eq. (1), Q_{epi} stands for the doping dose of the epitaxial layer. In this paper, the optimal Q_{epi} stands for the value of Q_{epi} when the BV obtains a maximum. It is also found that a larger optimal Q_{epi} promises a lower $R_{\mathrm{on.\,sp}}$, at the same time the BV still maintains a high value. Therefore, the basic strategy in the design of high BV and low $R_{\mathrm{on.\,sp}}$ LDMOS is to increase the optimal Q_{epi}.

The reduced surface field[2−5] (RESURF) principle offers a way to design high voltage devices with low on-resistance on the thin epitaxial layer. Compared with single RESURF LDMOS, the epitaxial layer of a multiple RESURF LDMOS can be more heavily doped at the same given BV. As a result, the optimal Q_{epi} will be larger and that provides the LDMOS with a more superior performance in the compromise of high BV and low $R_{\mathrm{on.\,sp}}$.

In works carried out by the previous researchers, the double RESURF LDMOS[6−14] has been studied thoroughly and is widely applied in power IC products. It helps to reduce $R_{\mathrm{on.\,sp}}$ by about 50% lower than single RESURF LDMOS. Seldom does anyone mention the triple RESURF LDMOS, which is also called a lateral MOSFET with dual conduction paths[15, 16]. In this paper, this structure is studied in detail by using the MEDICI numerical simulation tool. The influences of various parameters on BV, $R_{\mathrm{on.\,sp}}$, as well as process tolerance are studied to establish basic rules for the design of the triple RESURF LDMOS.

2. Device structure

Figure 1(a) shows the structure of the double RESURF N-channel LDMOS (nLDMOS) whose P-type top layer (P-tl) is located on the surface of the drift region. It exhibits excellent performance in the compromise of BV and $R_{\mathrm{on.\,sp}}$. A 750 V, 180 mΩ·cm^2 double RESURF nLDMOS has been put onto the market[7]. However, the distance between P-tl and P-well must be kept large enough to avoid high JFET resistance, which will cause $R_{\mathrm{on.\,sp}}$ to increase drastically. Furthermore, during the local oxidation of silicon (LOCOS) formation process, parts of the P-tl and the N-type epitaxial (N-epi) layer will be eaten, which will cause charge balance difficulties.

Figure 1(b) shows the structure of a triple RESURF nLDMOS whose P-type buried layer (P-bl) is located in the drift region via high energy ion implantation. Therefore, unlike the double RESURF nLDMOS, it will not be affected by LOCOS.

The basic parameters of the two devices are given as below: the concentration of the P-type substrate (P-sub) is 2×10^{14} cm^{-3}, the thickness of the N-epi is 15 μm and the length of field plate is 10 μm.

3. Results and discussion

The BV is the paramount parameter representing the off-state blocking capability. Figure 2 illustrates that at any given P-tl dose (Q_{tl}) or P-bl dose (Q_{bl}), the BV has a bell-shaped pattern with a plateau while the doping concentration of the N-epi varies. Compared with the double RESURF nLDMOS, the

* Project supported by the National Natural Science Foundation of China (No. 60906038), the Pre-Research Foundation, China (No. 9140A08010309DZ02), and the Science-Technology Foundation for Young Scientist of University of Electronic Science and Technology of China (No. L08010301JX0830).
† Corresponding author. Email: syin1@e.ntu.edu.sg
Received 2 March 2011, revised manuscript received 5 July 2011 © 2011 Chinese Institute of Electronics

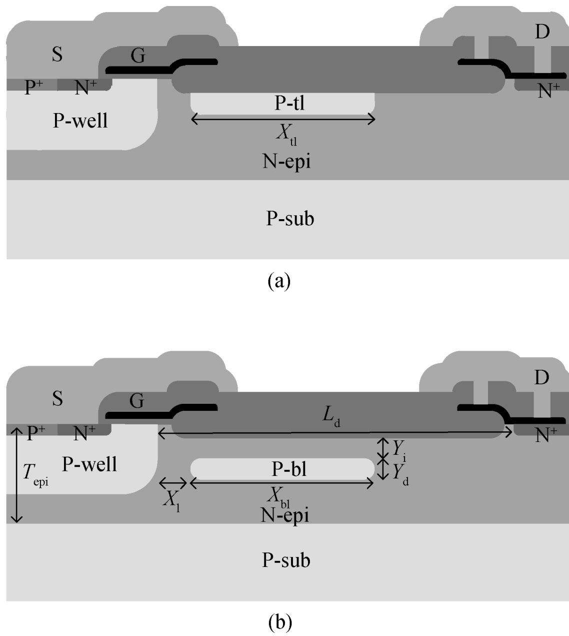

Fig. 1. Cross sections of RESURF devices. (a) Double RESURF nLDMOS. (b) Triple RESURF nLDMOS.

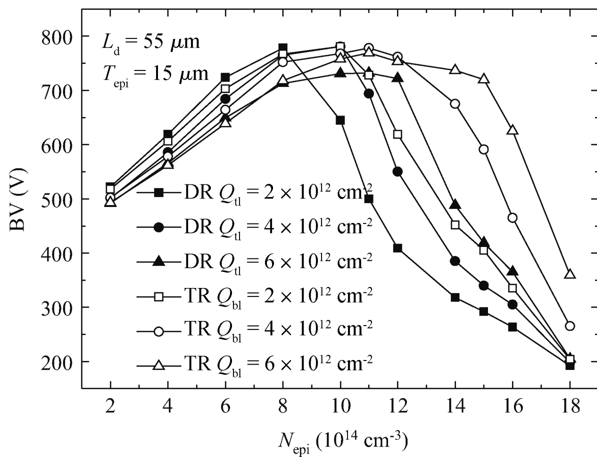

Fig. 2. Relationship between the BV and the N-epi doping concentration with P-tl and P-bl dose variations.

triple RESURF nLDMOS allows a larger optimal $Q_{\rm epi}$ and a wider range of process tolerance in the situation that $Q_{\rm bl}$ is equal to $Q_{\rm tl}$. Compared with itself, according to the charge sharing concept[5, 6], a larger $Q_{\rm bl}$ promises similar advantages as mentioned above. Since the P-bl is located in the drift region, there are three parallel P/N junctions in the vertical direction. When the drain electrode is applied with high voltage, the two junctions close to the P-bl will deplete it vertically from top and bottom. Compared with a double RESURF nLDMOS with only one P/N junction close to the P-tl in the vertical direction, it can deplete more completely and the value of the optimal $Q_{\rm epi}$ can be increased. Therefore a better performance of $R_{\rm on.\,sp}$ will be achieved.

Figure 3 illustrates the distribution of the horizontal electric field with $Q_{\rm bl}$ variations. If $Q_{\rm bl}$ is too small ($Q_{\rm bl} = 1 \times 10^{12}$ cm^{-2}), the P-bl cannot provide enough holes for the depletion process of the N-epi and avalanche breakdown will occur under the gate field plate. However, if $Q_{\rm bl}$ is too large ($Q_{\rm bl} = 1 \times 10^{13}$ cm^{-2}), avalanche breakdown will take place at the P-bl/N-epi junction because this junction becomes very vulnerable to high voltage.

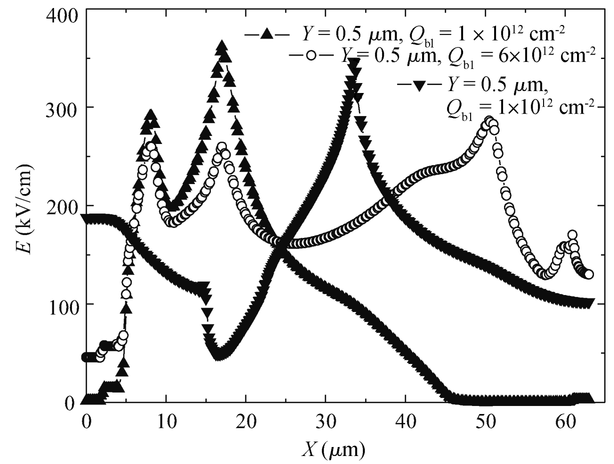

Fig. 3. Distribution of the horizontal electric field with P-bl dose variations.

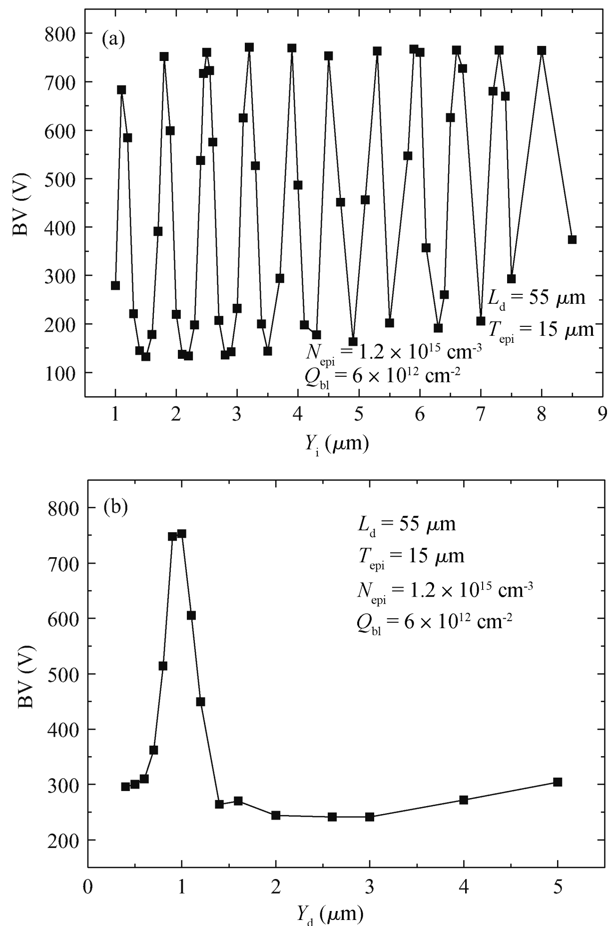

Fig. 4. Sensitivity of BV to variations of vertical dimensions of the P-bl. (a) Implantation depth. (b) Diffusion thickness.

A new problem is brought in: for a triple RESURF nLDMOS, the BV is very sensitive to the vertical dimensions of the P-bl. Even if the implantation depth ($Y_{\rm i}$) or diffusion thick-

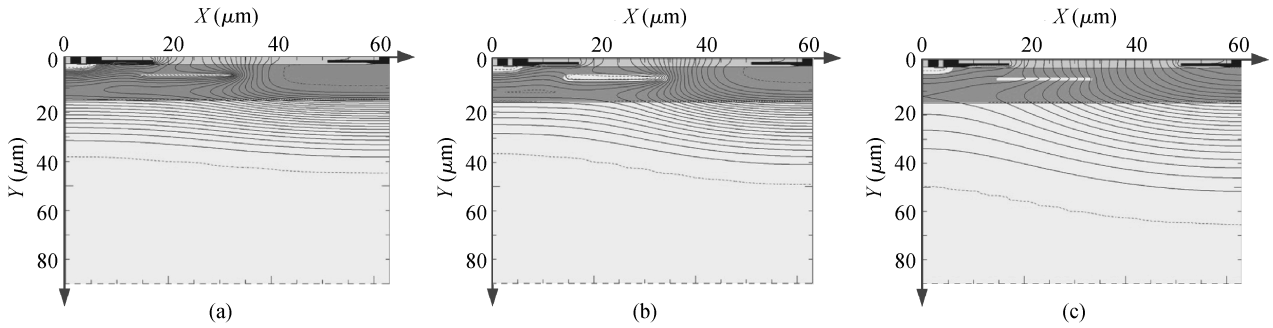

Fig. 5. Distribution of potential contours for different vertical dimensions of the P-bl. (a) $Y_{\rm i} = 4.8$ μm, $Y_{\rm d} = 1$ μm, BV = 177 V. (b) $Y_{\rm i} = 5$ μm, $Y_{\rm d} = 1.4$ μm, BV = 264 V. (c) $Y_{\rm i} = 5$ μm, $Y_{\rm d} = 1$ μm, BV = 753 V.

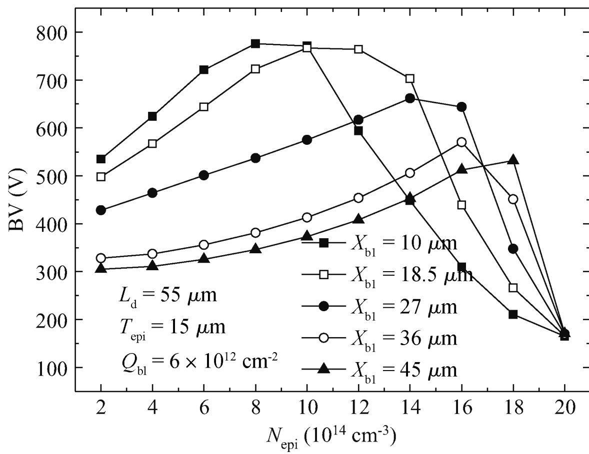

Fig. 6. Relationship between BV and doping concentration of the epitaxial layer with P-bl length variations.

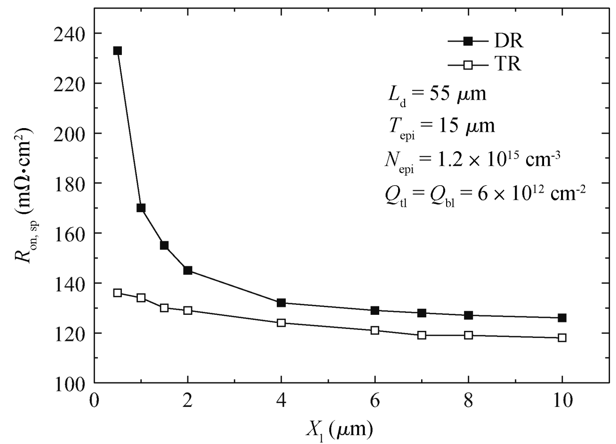

Fig. 7. Relationship between $R_{\rm on.\,sp}$ and the distance of the P-well and the P-bl.

ness ($Y_{\rm d}$) of the buried layer fluctuates slightly from the optimal value, the block characteristics will deteriorate very seriously. This will result in a very high demand of process tolerance.

Figure 4(a) illustrates that there are a series of peaks of the BV with $Y_{\rm i}$ variations. These peaks merely reach the same value of the BV by an equal space of about 0.7 μm. Figure 4(b) illustrates that there is only a peak of BV with $Y_{\rm d}$ variations. In addition, if $Y_{\rm d}$ is too large, avalanche breakdown will occur at the same point of the P-bl/N-epi junction. Figure 5 shows the distribution of potential contours when avalanche breakdown occurs. These contours centralize in a very narrow region near the buried layer if $Y_{\rm i}$ or $Y_{\rm d}$ fluctuates from the optimal value.

The length of the buried layer ($X_{\rm bl}$) is also discussed. The distance between the P-well and the P-bl ($X_{\rm l}$) is fixed and then $X_{\rm bl}$ is altered to study this relationship. Figure 6 illustrates that a larger $X_{\rm bl}$ allows for a larger optimal $Q_{\rm epi}$, but at the expense of a lower BV. Furthermore, if $X_{\rm bl}$ becomes too large, the plateau of the curve squeezes seriously. As a result, an optimized value promises a higher BV, a lower $R_{\rm on.\,sp}$ and also a wider range of process tolerance.

$R_{\rm on.\,sp}$ is the paramount parameter representing the on-state power consumption. It is simulated in the situation where the gate electrode is applied with 5 V and the drain electrode is applied with 0.1 V. The sectional area of the current conduction channel will decrease with the increase of $Y_{\rm d}$, leading to the increase of $R_{\rm on.\,sp}$. However, due to the sensitivity between the

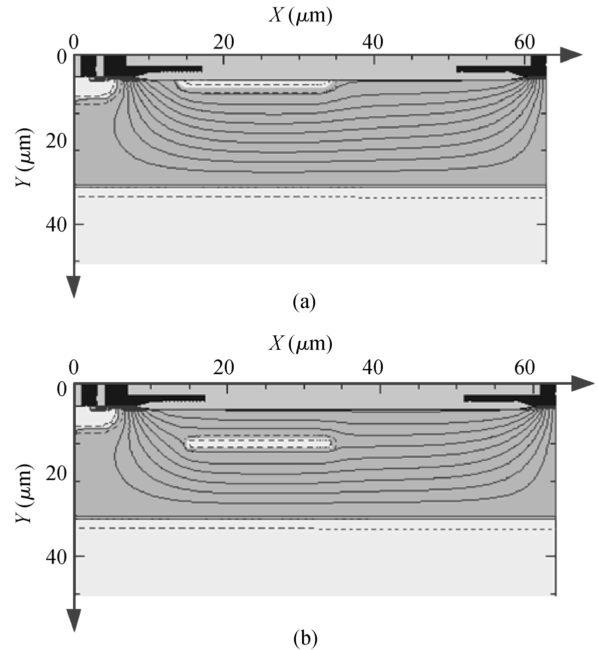

Fig. 8. Distribution of current contours. (a) Double RESURF nLDMOS. (b) Triple RESURF nLDMOS.

BV and $Y_{\rm d}$, $Y_{\rm d}$ must be carefully controlled and cannot vary over a wide range. Therefore its influence can be neglected.

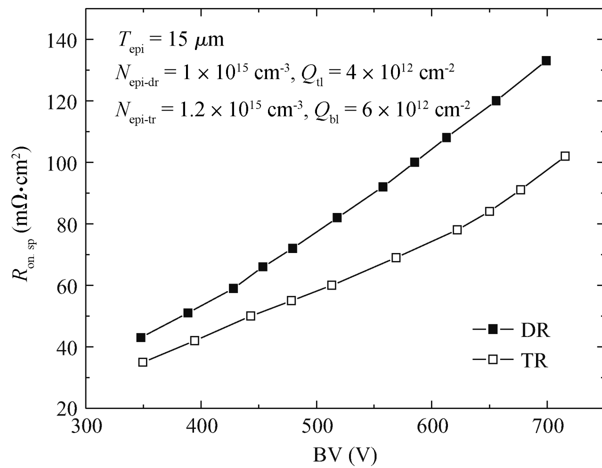

Fig. 9. Relationship between $R_{on.\,sp}$ and the BV.

Compared with a double RESURF nLDMOS, since the buried layer is located in the body, the JFET resistance effect is not so obvious. When the distance of the P-well and the P-bl varies, $R_{on.\,sp}$ will maintain at a low value without obvious variation, unlike the conventional structure, just as Figure 7 illustrates. As a result, it helps to eliminate JFET resistance. Figure 8 shows the distribution of the current contours of the two types of devices. For the double RESURF nLDMOS, there is only one current conduction path along the drift region. While for triple RESURF nLDMOS, there are two parallel paths.

The relationship between $R_{on.\,sp}$ and the BV can be achieved by altering L_d, P-tl length (X_{tl}) and X_{bl} under the precondition that the BV is linearly proportional to L_d. Figure 9 illustrates the quadratic relationship between $R_{on.\,sp}$ and the BV. The lower slope of the triple RESURF nLDMOS promises a better performance of a lower $R_{on.\,sp}$ in a wide range of BV. By altering L_d and X_{bl}, a series of devices with a BV ranging from 300 to 700 V can be obtained.

4. Conclusion

A triple RESURF nLDMOS with a BV of 700 V and $R_{on.\,sp}$ of 100 mΩ·cm^2 has been achieved by simulation. It has a better performance in the compromise of BV and $R_{on.\,sp}$. Under the same BV of 700 V, $R_{on.\,sp}$ is 30% lower compared with a conventional double RESURF nLDMOS. Furthermore, it helps to eliminate JFET resistance and offers a wider range of process tolerance for the epitaxial layer dose. However, it is hard to overcome the sensitivity of the BV to variations in the vertical dimensions of the P-bl. Therefore it asks for a much stricter demand on the process tolerance control during the implantation and diffusion process.

References

[1] Ludikhuize A. A review of RESURF technology. International Symposium on Power Semiconductor Devices and IC's, 2000: 11
[2] Appels J, Vaes H, Verhoeven J, et al. High voltage thin layer devices (RESURF devices). International Electron Devices Meeting, 1979: 238
[3] Ludikhuize A. Performance an innovation trends in RESURF technology. European Solid-State Device Research Conference, 2001: 35
[4] He Jin, Zhang Xing. Analytical model of surface field distribution and breakdown voltage for RESURF LDMOS transistor. Chinese Journal of Semiconductors, 2001, 22(9): 1102
[5] Imam M, Quddus M, Adams J, et al. Efficacy of charge sharing in reshaping the surface electric field in high-voltage lateral RESURF devices. IEEE Trans Electron Devices, 2004, 51(1): 141
[6] Imam M, Hossain Z, Quddus M, et al. Design and optimization of double-RESURF high-voltage lateral devices for a manufacturable process. IEEE Trans Electron Devices, 2003, 50(7): 1697
[7] Hossain Z. Determination of manufacturing RESURF process window for a robust 700 V double RESURF LDMOS transistor. International Symposium on Power Semiconductor Devices and IC's, 2008: 133
[8] Li Q, Li Z J. A new analytical model for the surface electrical field distribution of double RESURF LDMOS. International Power Electronics and Motion Control Conference, 2006: 1
[9] Qiao M, Li Z J, Zhang B, et al. Realization of over 650 V double RESURF LDMOS with HVI for high side gate drive IC. International Conference on Solid-State and Circuit Technology, 2006: 248
[10] Wu J, Fang J, Zhang B, et al. A novel double RESURF LDMOS with multiple rings in non-uniform drift region. International Conference on Solid-State and Circuit Technology, 2004: 349
[11] Li Z J, Guo Y F, Zhang B, et al. A new 2D analytical model of double RESURF in SOI high voltage devices. International Conference on Solid-State and Circuit Technology, 2004: 328
[12] Parthasarathy V, Khemka V, Zhu R, et al. SOA improvement by a double RESURF LDMOS technique in a power IC technology. International Electron Devices Meeting, 2006: 75
[13] Gao S, Chen J M, Ke D M, et al. Analytical model for surface electrical field of double RESURF LDMOS with field plate. International Conference on Solid-State and Circuit Technology, 2006: 1324
[14] Souza D, Narayanan S. Double RESURF technology for HVICs. Electron Lett, 1996, 32(12): 1092
[15] Disney D R, Paul A K, Darwish M, et al. A new 800 V lateral MOSFET with dual conduction paths. International Symposium on Power Semiconductor Devices and IC's, 2001: 399
[16] Hua T T, Guo Y F, Sheu G. A 2D analytical model of bulk-silicon triple RESURF devices. International Conference on Solid-State and Circuit Technology, 2010: 1850