Effect of charge sharing on the single event transient response of CMOS logic gates*

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Abstract: This paper presents three new types of pulse quenching mechanism (NMOS-to-PMOS, PMOS-to-NMOS and NMOS-to-NMOS) and verifies them using 3-D TCAD mixed mode simulations at the 90 nm node. The three major contributions of this paper are: (1) with the exception of PMOS-to-PMOS, pulse quenching is also prominent for PMOS-to-NMOS and NMOS-to-NMOS in a 90 nm process. (2) Pulse quenching in general correlates weakly with ion LET, but strongly with incident angle and layout style (i.e. spacing between transistors and n-well contact area). (3) Compact layout and cascaded inverting stages can be utilized to promote SET pulse quenching in combinatorial circuits.

Key words: single event transient; charge sharing; pulse quenching; 3-D TCAD simulation; radiation hardening
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1. Introduction

With the continuous scaling of bulk CMOS processes, single event transients (SETs) have become a significant source of error and are cause of great concern for digital circuit designers[1]. Critical charge and propagation delay have both decreased with scaling, so ions with a small linear energy transfer (LET) can deposit enough charge to generate SET pulses, which can propagate unattenuated through subsequent circuits and corrupt downstream logic and latches.

The decreasing feature size has also enabled single event charge sharing, i.e. multiple devices collecting charge from the charge cloud created by an incident ion[2, 3]. While charge sharing can be detrimental to storage cells[4, 5], it can be beneficial in combinatorial circuits in which pulse quenching occurs. Heavy-ion experiments have shown the existence of pulse quenching at high angles of ion strikes in 130 nm technology[6]. 3-D TCAD mixed mode simulations at the 90 nm node have shown that pulse quenching can occur at a normal incidence for minimally spaced circuits[6]. Experimental data for a 65 nm process have shown that pulse quenching is more prevalent in the common n-well design than in the separate n-well design[7].

The above research is restricted to PMOS-to-PMOS pulse quenching in the n-well for inverter chains. Previously, Amusan *et al.*[3] have shown that charge sharing also exists between NMOS transistors and between PMOS and NMOS transistors. This indicates that pulse quenching is also present in these circumstances, which is not negligible in an advanced process. It is imperative for circuit designers to fully understand how an SET pulse width will change in propagation through pulse quenching in order to accurately assess and harden their designs in a radiation environment.

In this paper, we present four types of pulse quenching mechanism (NMOS-to-PMOS, PMOS-to-NMOS, PMOS-to-PMOS, NMOS-to-NMOS) for the first time, in commonly used logic gates (NAND2, NOR2, AND2, OR2) and verify them using 3-D TCAD mixed mode simulations in a commercial 90 nm CMOS process. We then investigate the impact of ion LET, incident angle and layout style on each of the pulse quenching mechanisms. Finally, we will discuss the implications of our findings to the radiation characterization and hardening of CMOS circuits.

2. Charge collection mechanism

In our study, we characterize the SET pulse as the voltage glitch at the output of a logic gate, which is determined by the amount of charge deposited, charge collection efficiency and the rate of charge removal[8]. In addition to classical drift and diffusion, many parasitic effects, such as bipolar amplification[9] and the removal of charge by substrate/well contacts[10], play an ever-increasing role in advanced processes. In the following study, we carefully isolate charge sharing from the other determining factors, and discuss the interaction of charge sharing with other factors when necessary.

In bulk CMOS circuits, the transistor is only sensitive to charge collection when reverse biased in the OFF state. In the ON state, charge collected in the reversed junction is simply shunted to the power rail. Depending on the hit location of the incident ion, there are two types of single event hits: n-hit and p-hit, as illustrated in Fig. 1. An n-hit creates a high-to-low voltage transition at the sensitive node, while a p-hit creates a low-to-high voltage transition.

3. Analysis of the pulse quenching mechanism

At 130 nm and smaller technology nodes, charge sharing between adjacent transistors and signal propagation between adjacent nodes can occur with similar time constants. At the same time as the SET voltage pulse is transmitted through the top metal interconnects, the charge will also diffuse through

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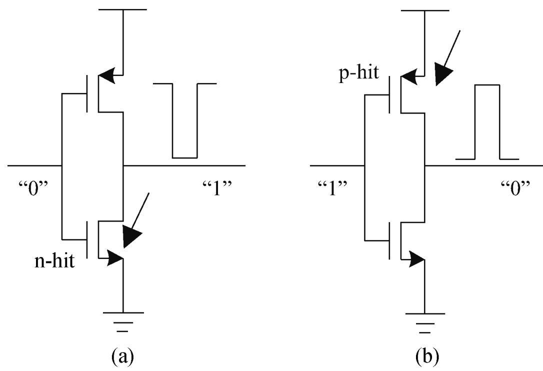

Fig. 1. (a) n-hit and (b) p-hit.

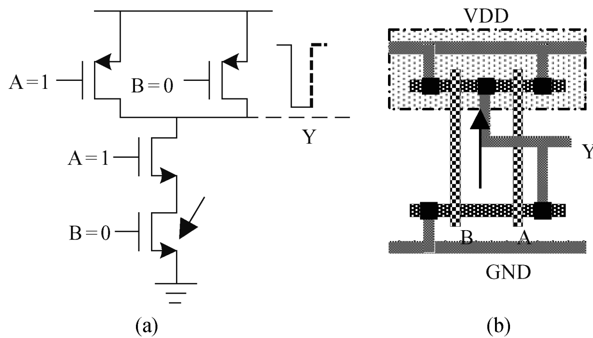

Fig. 2. NAND2 (a) schematic and (b) layout.

the substrate and is collected by other sensitive nodes. The combination of these two effects causes the SET pulses to be shortened through multiple node charge collection—an effect called pulse quenching. Depending on the sequence of the hit (either n-hit or p-hit), there are four types of pulse quenching: NMOS-to-PMOS, PMOS-to-NMOS, NMOS-to-NMOS, PMOS-to-PMOS. NMOS-to-PMOS, for example, refers to the case in which an n-hit happens first, and a p-hit happens thereafter. Next, we will explain each type in detail.

3.1. NMOS-to-PMOS

NMOS-to-PMOS pulse quenching is demonstrated with an NAND2 gate, as shown in Fig. 2. Input A is biased to a HIGH state, input B is biased to a LOW state, and output node Y is initially in a HIGH state. In this configuration the NMOSB is the only sensitive transistor. When an ion strikes the drain of the NMOSB, Y is driven to LOW by the collected charge and a HIGH-to-LOW pulse is generated at Y. As a result, the PMOSA becomes sensitive to charge collection. Charge from the drain area of the NMOSB can diffuse upward to the drain area of the PMOSA and get collected, as illustrated in Fig. 2(b). Charge collected by the PMOSA will drive Y back to a HIGH state and effectively truncate the SET pulse.

3.2. PMOS-to-NMOS

PMOS-to-NMOS pulse quenching is similar to the above NMOS-to-PMOS case. It is demonstrated with a NOR2 gate, as shown in Fig. 3, with input A biased as LOW and input B biased as HIGH. In this configuration a p-hit on the PMOSB

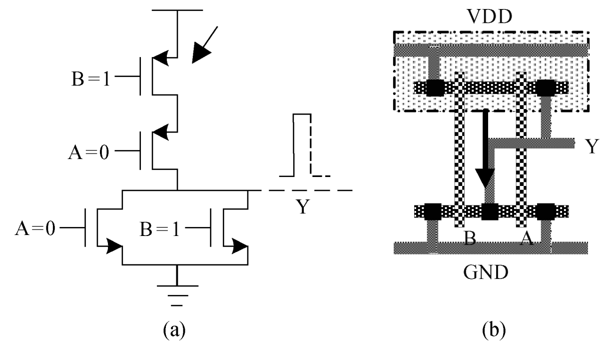

Fig. 3. NOR2 (a) schematic and (b) layout.

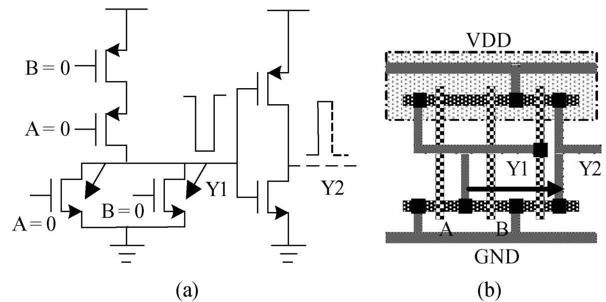

Fig. 4. OR2 (a) schematic and (b) layout.

will happen first and Y is driven to HIGH. Then, the NMOSA will become sensitive to charge collection and drive Y back to the LOW state.

3.3. NMOS-to-NMOS

NMOS-to-NMOS pulse quenching is demonstrated with an OR2 gate, as shown in Fig. 4. Both inputs A and B are biased to a LOW state, node Y1 is initially HIGH and node Y2 is initially LOW. In this configuration, both the NMOSA and NMOSB are susceptible to charge collection. When an ion strikes the common drain area of NMOSA and NMOSB, Y1 is driven LOW by the collected charge and a HIGH-to-LOW pulse is generated at Y1. This pulse will propagate to the inverter and generate a LOW-to-HIGH transition at Y2. As a result, the NMOS inverter becomes sensitive to charge collection. Charge can diffuse rightwards to the drain area of NMOS inverter and get collected, as illustrated in Fig. 4(b). Charge collection by the NMOS inverter will reset Y2 to a LOW state and effectively truncate the SET pulse.

3.4. PMOS-to-PMOS

PMOS-to-PMOS pulse quenching is similar to the above NMOS-to-NMOS case. It is demonstrated with an AND2 gate, as shown in Fig. 5, with both inputs A and B biased as HIGH. In this configuration, a p-hit on PMOSA and PMOSB will happen first, Y1 is driven HIGH and Y2 is driven LOW. Then, the PMOS inverter will become sensitive to charge collection and reset Y2 to a HIGH state.

As demonstrated above, two requirements have to be satisfied for pulse quenching to occur. The first one is that the charge sharing time constant must be on the same scale as the

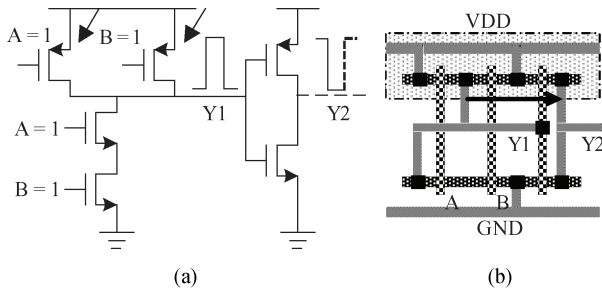

Fig. 5. AND2 (a) schematic and (b) layout.

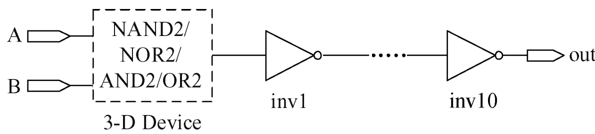

Fig. 6. Mixed mode simulation circuit.

node-to-node electrical propagation time. In older technologies, charge sharing is either too weak or too slow to catch up with the electrical signal, so pulse quenching would be insignificant. The second requirement is that in the propagation path of the SET pulses, there must be other transistors either forward biased in the OFF state (in the case of NMOS-to-PMOS and PMOS-to-NMOS) or reverse biased in the ON state (in the case of NMOS-to-NMOS and PMOS-to-PMOS), so that when the SET pulse arrives, the transistors will become sensitive to charge sharing and counteract the original voltage pulses.

4. Simulation methodology

To understand and verify the presence of the four pulse quenching mechanisms, 3-D TCAD mixed mode simulations are carried out at 90 nm technology node using Synopsys Sentaurus. The simulation circuit is shown in Fig. 6. Logic gates (NAND2, NOR2, AND2, OR2) are modeled fully or partly in 3-D device models, and use layouts as shown in Figs. 2–5 with the minimum spacing specified in the design rules. The 3-D device models are carefully calibrated to match the DC and AC characteristics (e.g. I_d–V_d and I_d–V_g) of the SMIC 90 nm mixed signal 1P9M PDK. The rest of the design uses compact SPICE models. The SET pulse is first examined at the gate direct output to ensure that pulse quenching did happen (whether its shape has changed). Then, the SET pulse width is measured after going through a 10-stage inverter chain (to account for electrical masking) as FWHV (full width at half VDD).

Charge sharing takes place due to the diffusion of the carriers in the substrate/well and therefore cannot be modeled at a circuit level. Taking advantage of this property, we model the passive node (the sensitive node collecting charge after the original SET pulse is generated) at both the circuit and device level, and compare their results to account for the effect of charge sharing. Take the NMOS-to-PMOS case (in Fig. 2) for example. We first simulate NMOSA, NMOSB and PMOSB of NAND2 at device level, as shown in Fig. 7(a), and PMOSA at circuit level without charge collection. Then NAND2 is simulated as a full device, as shown in Fig. 7(b), such that the effect of charge sharing from NMOSB to PMOSA is added. We use

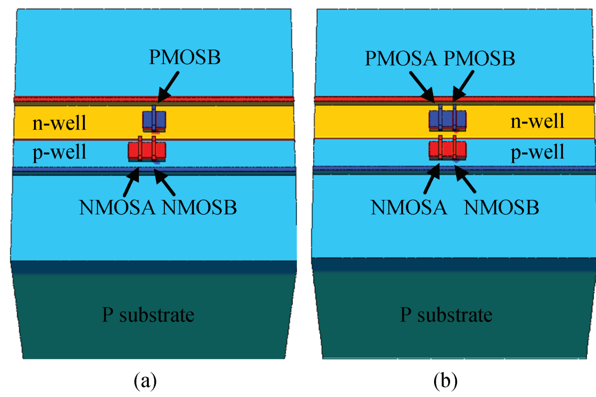

Fig. 7. NAND2 (a) partial and (b) full device model.

this technique throughout our simulations.

The following physical models are used in our simulations: Fermi–Dirac statistics, the band-gap narrowing effect, doping dependent SRH recombination and Auger recombination, and the mobility model, which includes doping, electric field and carrier–carrier scattering dependence. Ion strikes with constant LET versus depth are modeled using a Gaussian radial profile with a characteristic 1/e radius of 0.05 μm, and a Gaussian temporal profile with a characteristic decay time of 2 ps.

5. Simulation results

To investigate the pulse quenching mechanism, simulations are run with ion LET from 10 to 50 MeV·cm^2/mg at normal incidence (0°) and at n incident angles from 30° to 75° at 10 MeV·cm^2/mg. In the case of NMOS-to-PMOS and PMOS-to-NMOS charge sharing, the strike is along the width of the device, while in the case of NMOS-to-NMOS and PMOS-to-PMOS charge sharing, the incident angle is along the length of the device. In each simulation the design is struck in the same location—the drain of the sensitive transistor. The final result is represented as the ratio of the SET pulse width with charge sharing to the SET pulse width without charge sharing. So a ratio of 1.0 means no pulse quenching has occurred, while a ratio of 0 indicates a complete truncation of the original SET pulse. Next, we investigate each type in detail.

5.1. NMOS-to-PMOS

NMOS-to-PMOS pulse quenching is modeled in the NAND2 gate shown in Fig. 2, and the simulation results with ion LET and the incident angle are shown in Figs. 8(a) and 8(b). It can be seen that charge sharing is minimal at normal incidence and that prominent pulse quenching only occurs at high incidences (> 60°). In the case of NMOS-to-PMOS charge sharing, charge is diffused from the p-well (substrate) to the n-well. The n-well/p$^+$-implant junction acts as a natural barrier to the collection of holes and the mobility of the holes is small compared to that of electrons. So most charges simply diffuse out, recombine or get collected by the substrate contact. As a result, NMOS-to-PMOS pulse quenching would not be prominent in most cases.

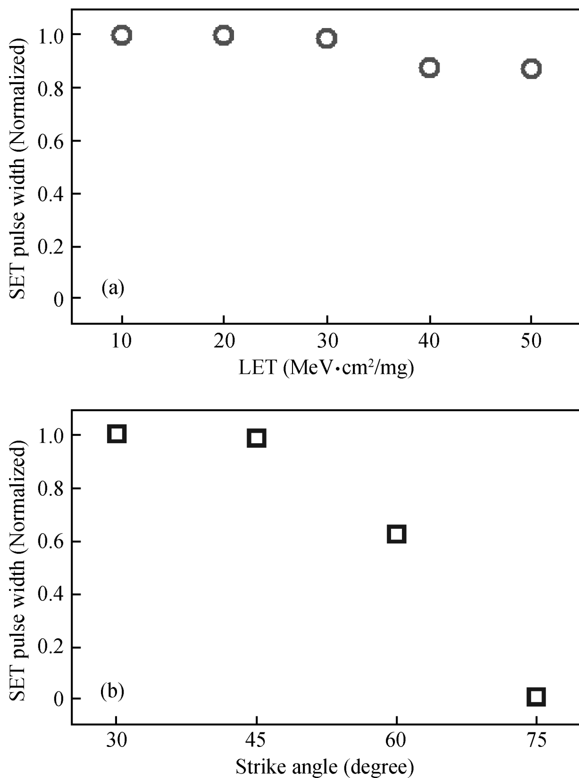

Fig. 8. (a) SET pulse quenching versus LET for NMOS-to-PMOS. (b) SET pulse quenching versus strike angle for NMOS-to-PMOS.

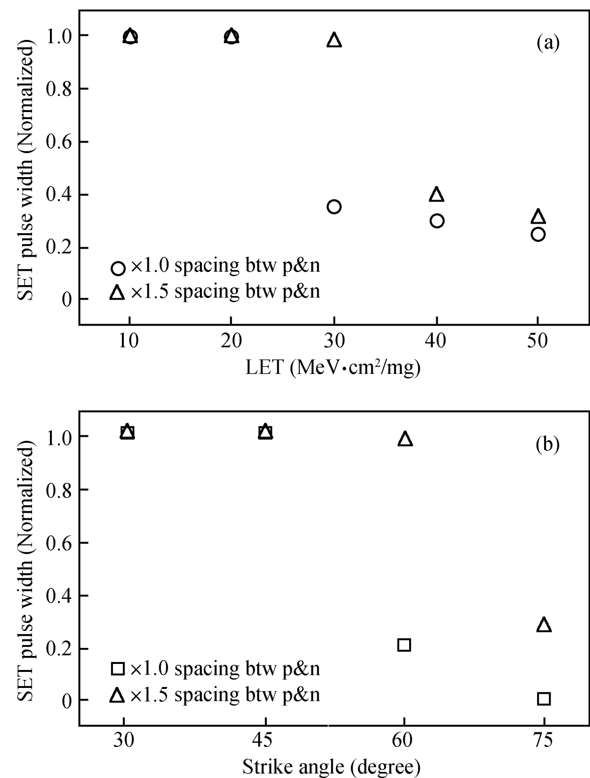

Fig. 9. (a) SET pulse quenching versus LET for PMOS-to-NMOS. (b) SET pulse quenching versus strike angle for PMOS-to-NMOS

5.2. PMOS-to-NMOS

PMOS-to-NMOS pulse quenching is modeled in an NOR2 gate and depicted in Fig. 3, and simulations are run for layouts with minimum spacing between the PMOS and the NMOS and 1.5 times minimum spacing between the PMOS and the NMOS, as shown in Figs. 9(a) and 9(b). It can be seen that pulse quenching depends weakly on ion LET once pulse quenching occurs, but strongly on incident angle. In this case, charge is mainly shared through diffusion, and its efficiency does not change with ion LET. Also, PMOS-to-NMOS pulse quenching is more prominent than for NMOS-to-PMOS, this is mainly due to the increased collection volume of NMOS transistors and the increased mobility of electrons. When the spacing between the PMOS and NMOS is increased to 1.5 times, the pulse quenching effect is reduced, because charge sharing efficiency will decline as the diffusion distance increases.

5.3. NMOS-to-NMOS

NMOS-to-NMOS pulse quenching is modeled in an OR2 gate, and simulations are run for two layouts with different spacing between the charge sharing NMOS pair. The first layout is shown in Fig. 4(b), with minimum spacing between the NMOS pair. The second layout is shown in Fig. 10, with two times the minimum spacing and STI oxide between the NOR2 stage and the inverter stage.

The simulation results for both layouts with ion LET and incident angle are shown in Figs. 11(a) and 11(b). It is evident that NMOS-to-NMOS pulse quenching exists even at low ion LET ($<$ 10 MeV·cm^2/mg) and low incident angles ($<$ 30°) for minimum sized layouts. Similar to the PMOS-to-NMOS case, pulse quenching depends weakly on ion LET beyond a threshold, but strongly on incident angle. When the distance increases by a factor of two between the charge sharing NMOS pair, the pulse quenching effect is reduced, since NMOS transistors share charge mainly through a diffusion process[3]. However, the correlation with spacing for NMOS-to-NMOS cases is weaker than for PMOS-to-NMOS cases, as shown in Figs. 9(a) and 9(b).

5.4. PMOS-to-PMOS

PMOS-to-PMOS pulse quenching is modeled in an AND2 gate, and simulations are run for two variants of the layout, as shown in Fig. 5. One has a long n-well contact similar to that shown in Fig. 7 and the other has a short n-well contact equivalent to the length of S/D diffusion, and is about one eighth of the length of the former.

From the simulation results shown in Figs. 12(a) and 12(b), it can be seen that PMOS-to-PMOS pulse quenching is prominent in the 90 nm process, as identified previously by Ahlbin *et al.*[6]. Unlike the previous cases, the normalized SET pulse width is nearly the same across different ion LETs and incident angles for the layout with long n-well contact. Such results, we believe, is due to the effect of bipolar amplification being the dominant charge sharing mechanism between the PMOS transistors[3]. Since bipolar amplification is a parasitic effect related to the fabrication process and design layout, which remains the same across different ion LETs and incident angles, charge sharing efficiency, thus pulse quenching will also be fixed. This also explains why pulse quenching is less prominent in the layout with a long n-well contact: a longer n-well

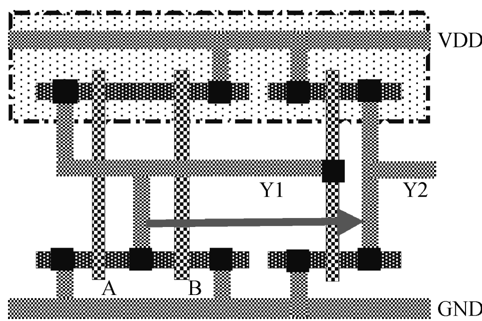

Fig. 10. OR2 separated layout.

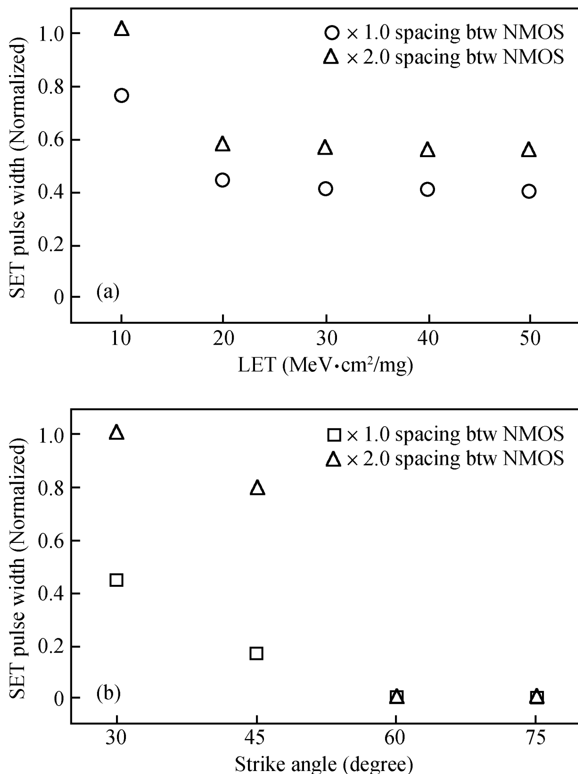

Fig. 11. (a) SET pulse quenching versus LET for NMOS-to-NMOS. (b) SET pulse quenching versus strike angle for NMOS-to-NMOS.

contact helps to maintain the n-well potential and reduce the charge shared between PMOS transistors, and its function becomes more visible as ion LET increases.

6. Discussion

The simulation results show that in addition to the PMOS-to-PMOS case identified previously, pulse quenching is also prominent for PMOS-to-NMOS and NMOS-to-NMOS cases in a 90 nm process. Also, pulse quenching in general depends weakly on ion LET, but strongly on incident angle and layout style (i.e. spacing between transistors and n-well contact area). As the process further scales down, a single charge cloud will encompass more transistors and the circuit response will be determined by the complex interactions between proximal transistors, rather than a single transistor, as in older technology.

As the effect of charge sharing increases, it is also necessary to use 3-D TCAD simulations (although very time con-

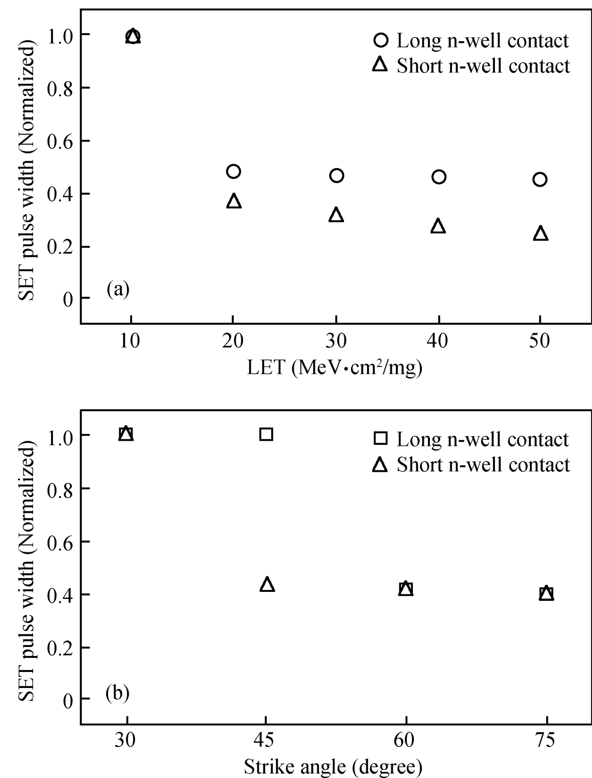

Fig. 12. (a) SET pulse quenching versus LET for PMOS-to-PMOS. (b) SET pulse quenching versus strike angle for PMOS-to-PMOS.

suming) when characterizing circuits for radiation hardness. The incident angle also needs to be considered: nodes that may not share charge at normal incidence are sensitive to charge sharing at higher angles of incidence. Charge sharing may have a lower upset threshold in a DICE cell[11], and it may contribute to pulse quenching in combinatorial circuits.

Finally, our findings suggest several techniques for radiation hardening in combinatorial circuits. First, layouts of the logic gates for combinatorial circuits should be as compact as possible, as opposed to nodal separation in memory cells. For example, the PMOS and NMOS transistors should be placed in close proximity, and the fanout stage should be incorporated as much as possible (OR rather than NOR + INV). Second, it can be seen in Sections 3.3 and 3.4 that PMOS-to-PMOS and NMOS-to-NMOS pulse quenchings only happen between inverting stages. Therefore, the more sensitive gates in combinatorial circuits (with low logical masking probability) could be synthesized with cascading inverting stages as fanouts (such as inverters) to promote pulse quenching. The effect of the n-well contact in PMOS-to-PMOS case, however, is worth further discussion. While a small n-well contact contributes to pulse quenching through enhanced bipolar amplification, it also increases the absolute SET pulse width by an average of 52%, and even more in other configurations when pulse quenching does not happen. Therefore, a long n-well contact would be a better choice in most cases.

In the future, we plan to validate our simulation results in heavy-ion microbeam experiments. In reality, charge sharing always exists and cannot be eliminated entirely as in our simulations. As a result, the current experiments can only validate pulse quenching indirectly[6, 7], that is, they compare the

case with strong pulse quenching with the case with weak pulse quenching (e.g. no guard band versus guard band, common n-well versus separate n-well). In addition, they are restricted to PMOS-to-PMOS pulse quenching in inverter chains. We plan to investigate all four pulse quenching mechanisms in 2-input logic chains at the 90 nm node, and measure the SET pulse distribution with ion LET and incident angle for various layout styles (different spacing between charge sharing transistors or different n-well contact area, etc.), so that we can validate the results of our simulations.

7. Conclusion

In this paper, four types of pulse quenching mechanisms (NMOS-to-PMOS, PMOS-to-NMOS, NMOS-to-NMOS and PMOS-to-PMOS) are identified respectively in NAND2, NOR2, OR2, AND2 logic gates, and then verified using 3-D TCAD mixed mode simulations for a commercial 90 nm process. Specifically, in the NMOS-to-PMOS case, pulse quenching only occurs at high incidence; in the PMOS-to-NMOS case, pulse quenching depends weakly on ion LET, but strongly on incident angle along the width of the transistor and spacing between PMOS and NMOS transistors; in the NMOS-to-NMOS case, pulse quenching also depends weakly on ion LET, but strongly on incident angle along the length of the transistor and spacing between NMOS transistors; in the PMOS-to-PMOS case, pulse quenching depends weakly on both ion LET and incident angle, but strongly on the n-well contact. These findings indicate that charge sharing needs to be considered when characterizing circuits for radiation hardness in sub-90 nm processes. Combinatorial circuits can be hardened for SET pulse quenching through the use of compact layouts and cascaded inverting stages.

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