Design and optimization of a 2.4 GHz RF front-end with an on-chip balun

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Abstract: A 2.4 GHz low-power, low-noise and highly linear receiver front-end with a low noise amplifier (LNA) and balun optimization is presented. Direct conversion architecture is employed for this front-end. The on-chip balun is designed for single-to-differential conversion between the LNA and the down-conversion mixer, and is optimized for the best noise performance of the front-end. The circuit is implemented with 0.35 μm SiGe BiCMOS technology. The front-end has three gain steps for maximization of the input dynamic range. The overall maximum gain is about 36 dB. The double-sideband noise figure is 3.8 dB in high gain mode and the input referred third-order intercept point is 12.5 dBm in low gain mode. The down-conversion mixer has a tunable parallel R–C load at the output and an emitter follower is used as the output stage for testing purposes. The total front-end dissipation is 33 mW under a 2.85 V supply and occupies a 0.66 mm^2 die size.

Key words: front-end; LNA; balun; mixer; direct-conversion
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1. Introduction

A single RF front-end operating in 2.4 GHz band, incorporating a three-gain steps LNA with an on-chip balun for single-to-differential conversion and a double balanced Gilbert mixer for wireless communication applications has been proposed. By introducing an on-chip balun, the off-chip balun is eliminated so a 1 dB noise figure improvement is achieved and costs are reduced. Optimization techniques are critical for meeting the high performance requirements of a system incorporating such a front-end. In this paper, by way of architecture design and a balun optimization technique, we describe a low-cost, low-power and high-performance front-end that contains the most important elements required to realize the ratio frequency (RF) reception paths of wireless communication receivers. A novel LNA is proposed that has three variable gain modes and uses only one on-chip balun without any other inductors. A balun optimization design technique for improved gain performance is introduced in the front-end.

Direct conversion architecture is the prevalent choice in most modern radio receivers because of its high level of integration and relatively low cost, as shown in Fig. 1. Therefore, direct-conversion architecture is adopted in this 2.4 GHz band front-end design. In the design of the single-ended LNA, a differential double-balanced Gilbert down-converter is used with an on-chip balun for single-to-differential conversion at the output of the LNA.

2. RF front-end circuit optimization design

2.1. Architecture of the dual-band front-end

Figure 2 shows the architecture adopted in this design. The receiver realizes the single-to-differential conversion at the output of the LNA and the input of the following down-converter with an on-chip balun. The tunable RC tank at the output of the down-conversion mixer enables tuning of the low pass cut-off frequency of the output signal in order to provide the following baseband channel-select filter with the most suitable signal.

It is known that most antennas are single-ended. To minimize costs and to use a minimal amount of off-chip components, the input of the LNA should be single-ended, and the single-to-differential conversion could be realized on chip. In fact, a single-balanced mixer can be used for the down-conversion with a single input and a differential output. However, a single-balanced mixer has poor rejection of LO to IF leakage. A double-balanced mixer could be adopted, with one of the inputs connected to ground, but this method is not chosen when high linearity is required. Finally, the use of an on-chip balun for the single-to-differential conversion in the input stage of an LNA has been proven to be a good solution for high linearity applications. However, extra noise degradation due to the power loss of the input balun weakens its validity in high-sensitivity radio design. Thus, an on-chip balun at the output of the LNA has been widely adopted for providing both

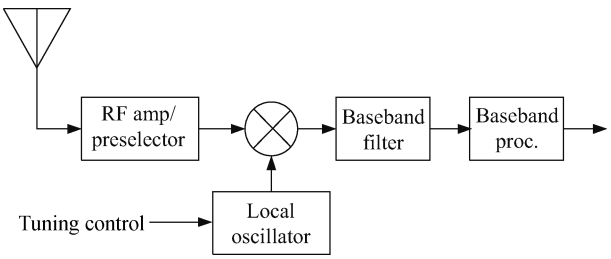

Fig. 1. Block diagram of the direct conversion architecture.

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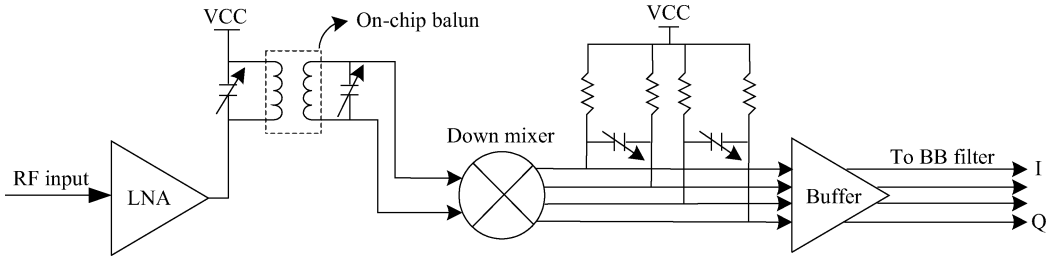


Fig. 2. Block diagram of a 2.4 GHz RF receiver front-end architecture.

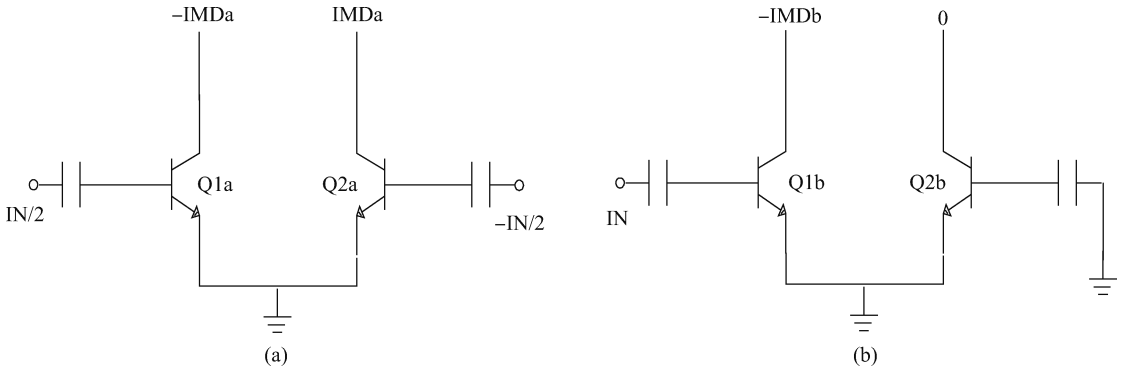


Fig. 3. Schematic for IIP3 analysis. (a) Differential input. (b) Single-ended input.

good noise and linearity performance, and it is used in this design[1]. In this method, the loss of the balun will not degrade the noise performance of the receiver a great deal as long as the gain of the LNA is large enough. As a pseudo-differential down-converter is used in this design, the differential input signals improve the linearity of the mixer by 6 dB as compared to a single-ended input signal.

As shown in Fig. 3, input signals with equal amplitude are added to the pseudo differential pairs in different ways. Ignoring other contributions of nonlinearity, and only considering the third-order intermodulation terms of the input transistors, we get

$$\mathrm{IMDoutb} = \mathrm{dB}(-\mathrm{IMDb} - 0) = \mathrm{dB}\left[a_3 \cdot (\mathrm{IN})^3\right], \quad (1)$$

$$\begin{aligned}\mathrm{IMDouta} &= \mathrm{dB}(-\mathrm{IMDa} - \mathrm{IMDa}) = \mathrm{dB}\left[a_3 \cdot 2 \cdot \left(\frac{\mathrm{IN}}{2}\right)^3\right] \\ &= \mathrm{dB}\left[a_3 \cdot (\mathrm{IN})^3\right] - 12,\end{aligned} \quad (2)$$

$$\mathrm{IMDouta} = \mathrm{IMDoutb} - 12, \quad (3)$$

where IMDouta and IMDoutb are the differential output third-order intermodulation terms. By calculating the IIP3 without extrapolation, we have

$$\mathrm{IIP3a} = (\mathrm{Pfunda} - \mathrm{IMDouta})/2 + \mathrm{Pina}, \quad (4)$$

$$\mathrm{IIP3b} = (\mathrm{Pfundb} - \mathrm{IMDoutb})/2 + \mathrm{Pinb}, \quad (5)$$

where Pfunda and Pfundb are the fundamental linearity output terms, and Pina and Pinb represent the input voltage in dB terms. Suppose Pina = Pinb, and that the gain is linear, Pfunda = Pfundb. Then we get

$$\mathrm{IIP3a} = \mathrm{IIP3b} + 6. \quad (6)$$

As mixer nonlinearity dominates the linearity performance of the front-end, improving the linearity of the mixer by 6 dB means that the linearity of the front-end will increase almost 6 dB. The test result shows that the linearity of this front-end in HG mode is –15 dBm, which is a large increase when compared to the front-end without an on-chip balun.

2.2. Low-noise amplifier with on-chip balun design

As the first stage and one of the most important stages of a typical receiver, the LNA functions mainly to provide enough gain to overcome the noise from the subsequent stages while generating least noise itself. The LNA design is a trade off between gain, input impedance, noise figure and power consumption. To accommodate the high dynamic range requirement of typical receivers, a novel LNA with three gain modes is put forward. The LNA provides 26 dB high gain, 10 dB middle gain (MG) and –3 dB low gain, respectively.

The presented LNA is shown in Fig. 4, which uses the cascode stage for amplification and passive devices and a switch for by-pass with the primary turn of the balun and a tunable capacitor as the output tank. The secondary of the balun transmits the power of the LNA to the following mixer. There are three gain branches to provide a large input dynamic range. The HG branch is a cascode stage with a downbond inductor for degeneration, while the MG branch uses a resistor for degeneration of another cascode stage, which is aimed at reducing gain and improving linearity. For the LG mode, a by-pass is used for high-linearity applications. The current of the HG and MG branches is biased at the best noise performance.

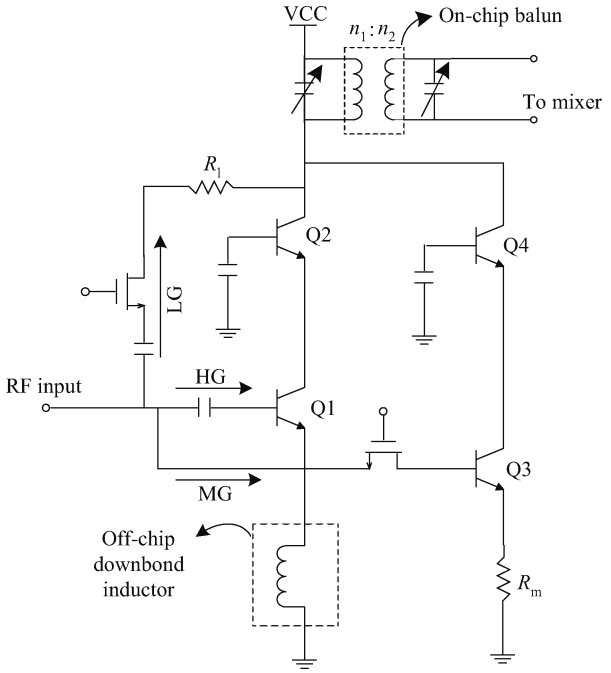


Fig. 4. Block diagram of the presented LNA.

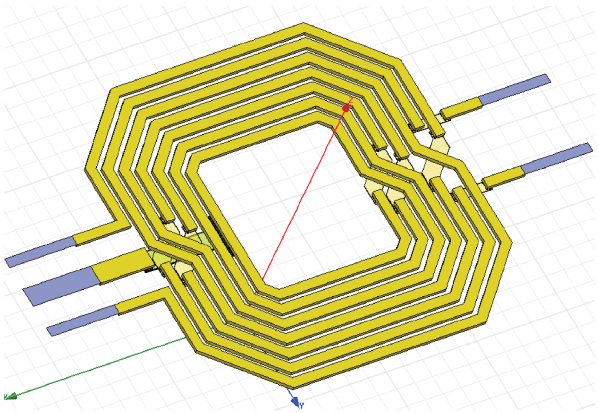


Fig. 5. Balun used in the design.

The design of the balun should aim at optimizing the performance of the front-end[2]. Figure 5 shows the designed balun using the HFSS three-dimentional simulation tool. As is known, a normal technique for designing a balun is to achieve the largest power gain or the least power loss for the balun. However, largest power gain does not mean largest voltage gain. Voltage gain is critical for noise performance in narrowband circuits with more than one stage. So, in this design, a novel method is put forward to improve the voltage gain of the LNA through balun optimization in order to obtain the best noise performance of the front-end. The LNA with the balun in the presented front-end receiver is designed to achieve the largest voltage gain possible for better noise performance of the front-end. which needs the balun to be designed properly. Using a simple balun model, we can write the gain of the LNA with a balun as follows:

$$\text{Gain\_LNA} = g_m \cdot Z_1 \cdot \text{Gain\_balun}, \tag{7}$$

where g_m is the transconductance of the cascode stage and Z_1

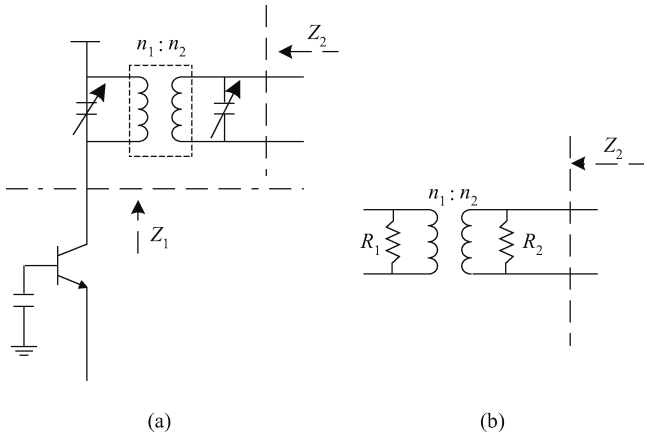


Fig. 6. The simplified model for calculation of voltage gain.

is the input impedance of the load seen from the collector of the cascode transistor, as shown in Fig. 6(a). For an ideal transformer, Gain_balun equals the ratio of n_2 to n_1. While,

$$Z_1 = Z_2 \frac{n_1^2}{n_2^2}, \tag{8}$$

so, the gain can be expressed as

$$\text{Gain\_LNA} = g_m Z_2 \frac{n_1}{n_2}. \tag{9}$$

To obtain the Gain_LNA using the parameters of the balun and the transistors, Z_2 should be expressed using balun parameters. As shown in Fig. 6(b),

$$Z_2 = R_2 \| \left(R_1 \frac{n_2^2}{n_1^2} \right), \tag{10}$$

$$R_1 = \omega L_1 Q_1, \quad R_2 = \omega L_2 Q_2. \tag{11}$$

When

$$\frac{n_1}{n_2} = \sqrt{\frac{L_1 Q_1}{L_2 Q_2}}, \tag{12}$$

we get the maximum gain of the LNA as

$$\text{Gain\_LNA\_max} = \frac{1}{2} g_m \sqrt{R_1 R_2} = \frac{1}{2} g_m \omega \sqrt{L_1 L_2 Q_1 Q_2}. \tag{13}$$

As shown, the gain is directly related to the inductance and quality factor of the primary and secondary coil of the balun. Thus, to improve the gain of the LNA, we try to improve the product of the parallel parasitic resistance of the inductors. Proper geometry design of the balun and choice of $n_1 : n_2$ help to achieve this. In the presented front-end, the simulated voltage gain of the LNA is as high as 29 dB. The test results of a low noise figure and high linearity prove the feasibility of the method.

2.3. Down-conversion mixer design

The quadrature mixer shown in Fig. 7 has been developed to provide an improved image rejection ratio (IRR) and a reduced phase error[3]. The local signals turn on in the order: LOQp, LOIp, LOQn, LOIn. For example, when the RF signal

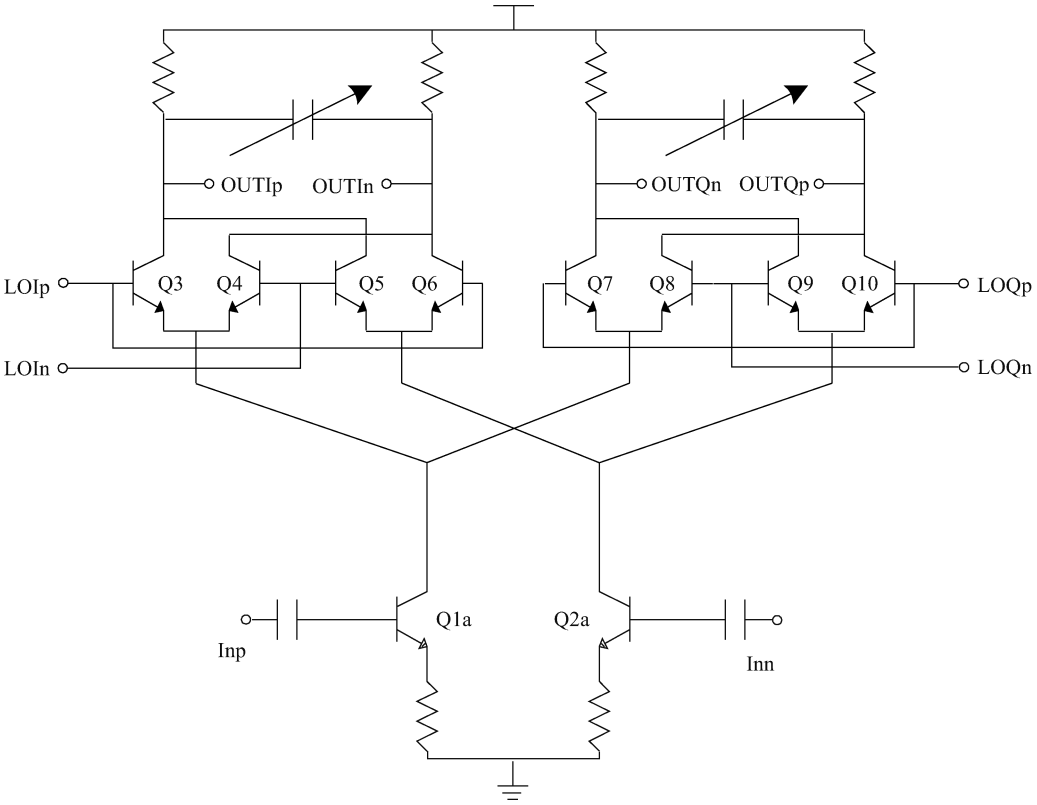


Fig. 7. Quadrature down-conversion mixer.

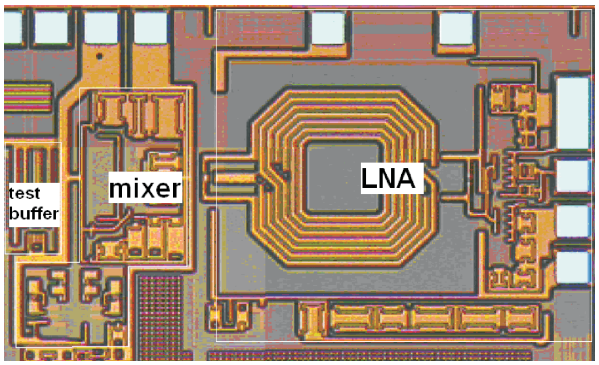


Fig. 8. Die micrograph of the front-end receiver.

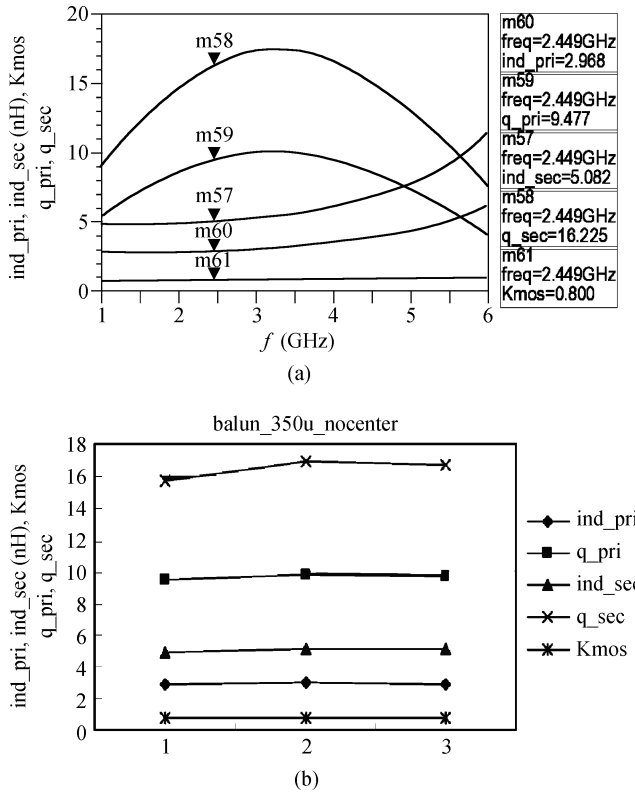


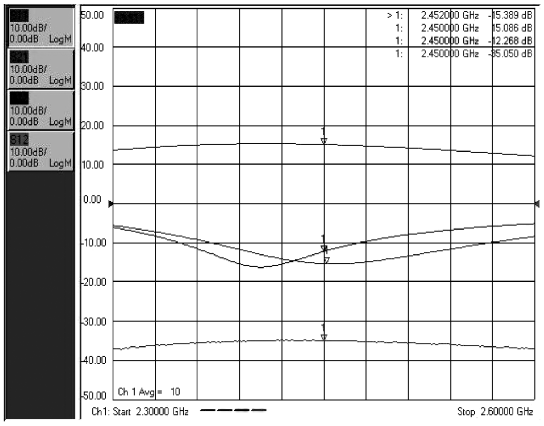
Fig. 9. On-wafer test results of the on-chip balun. (a) Characteristic of a typical balun. (b) Characteristic of three measured balun.

on transistor Q1 is high and the LOQp signal on Q7 is high, the voltage of the collector terminal of Q1 is pulled high and the transistors Q3, Q4, and Q8 are shut off. In this way, the total available current ($I_{c1} + I_{c2}$) must flow through only a selected transistor according to the local signal sequence.

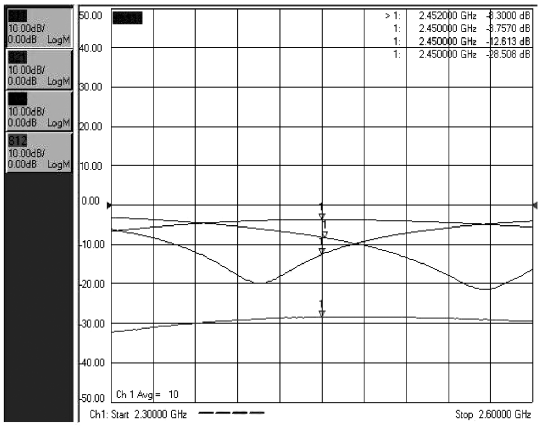
In Fig. 7, the tuned capacitors in the output load of the mixer are used to filter out the RF-to-IF and LO-to-IF leakage and their harmonics. In order to obtain a good quality of signal from the subsequent baseband filter and digital processor, the capacitors can be tuned to a favorite value for the best performance of the whole system.

3. Measurement results

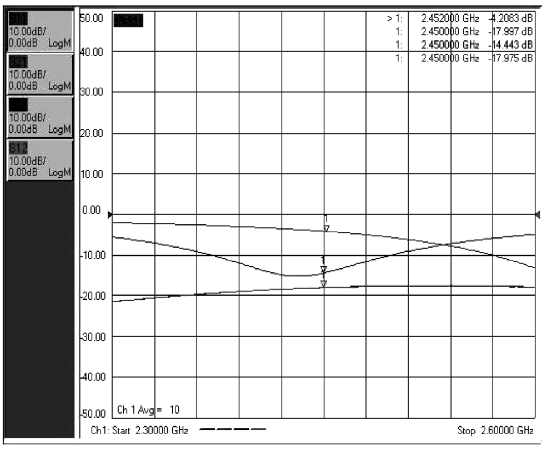
The front-end receiver has been implemented in 0.35-μm SiGe BiCMOS technology, and the die micrograph is shown in Fig. 8. The chip consumes 33 mW for a 2.85 V supply and



(a)



(b)



(c)

Fig. 10. The measured S-parameters of the LNA in HG/MG/LG modes. (a) HG mode. (b) MG mode. (c) LG mode.

occupies 0.66 mm^2 of die area. It uses a balun for single-to-differential conversion and power transmission between the LNA and the following down-converter. As shown in Fig. 9, the on-chip balun has a coefficient of magnetic coupling $k_{\rm m}$ of 0.8. The inductor of the primary and secondary coil is 2.968 nH and 5.082 nH at 2.45 GHz, respectively, and the quality factor of the Q coils is 9.477 and 16.225, respectively. From Fig. 9(b), the on-wafer test[4] results of three baluns have almost the same characteristics, which proves the consistency.

The LNA with the balun taped out by itself has a noise figure of 2.8 dB and consumes only 8.55 mW of power. Figure 10 shows the S-parameter of the LNA in three gain modes. The S_{21} is 15/–3.8/–18 dB, respectively, with S_{11} lower than –10 dB in HG mode. The LNA has a high linearity performance of –7.5 dBm in HG mode. The measured linearity is 7.5 dBm/15 dBm in MG/LG, respectively.

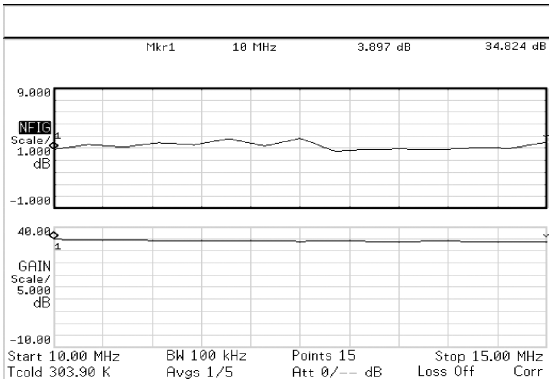


Fig. 11. Measured front-end receiver noise figure in HG mode.

Table 1. Summary of the front-end measurement results.

LNA performance	
Noise figure @ HG	2.8 dB
IIP3 (HG/MG/LG)	–7.5/7.5/1f5 dBm
S_{21} (HG/MG/LG)	15.1/–3.8/–18 dB
Receive path (LNA + mixer) performance	
Noise figure @ HG	3.8 dB
IIP3 (HG/MG/LG)	–15/3/12.5 dBm
Voltage gain (HG/MG/LG)	35.5/16.9/2 dB
Power dissipation	
LNA	8.55 mW
Mixer	22.8 mW
Total power @ 2.85 V	33 mW
Implementation	
Die area	0.66 mm^2
Technology	0.35-μm SiGe BiCMOS

Table 2. Comparison of measurement results with and without balun.

Performance	With balun	Without balun
Noise figure @ HG	3.8 dB	4.0 dB
IIP3 (HG/MG/LG)	–15/3/12.5 dBm	–21.5/–2/7 dBm
Voltage gain (HG)	35.5 dB	33 dB

Figures 11 and 12 show the measured performance of the front-end receiver. As shown, with S_{11} under –16 dB in 2.45 GHz frequency, the noise figure of the front-end in HG mode is 3.8 dB only. The measured IIP3 of the front-end is calculated with the following equation to be –15/3/12.5 dBm in HG/MG/LG modes, which are lower than those of the LNA. This can be well explained by the down-conversion mixer dominating the front-end linearity performance.

$$\mathrm{IIP_3}|_{\rm dBm} = \frac{\Delta P|_{\rm dBm}}{2} + P_{\rm in}|_{\rm dBm}. \tag{14}$$

The high linearity of –15 dBm in high gain mode proves the conclusion that the balun with a differential output proves the linearity of the pseudo-differential mixer, and then proves the linearity of the front-end receiver chip. Table 1 shows the measured results summary of the front-end chip.

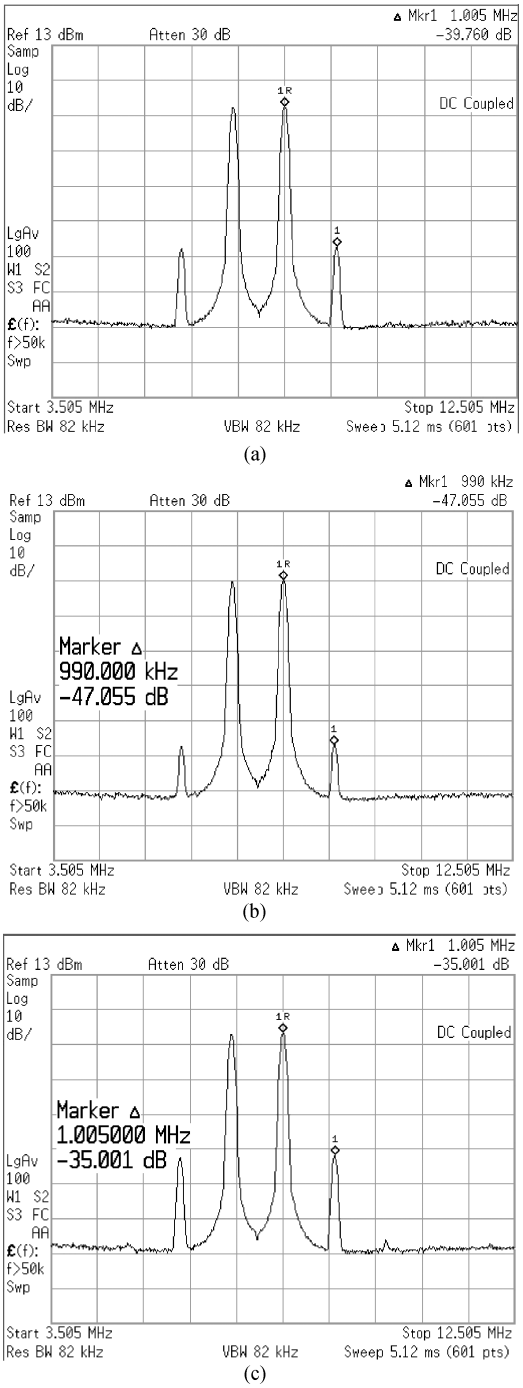


Fig. 12. Two-tone IIP3 measurement for the RF front-end in three gain modes. (a) HG in −35 dBm input. (b) MG in −20 dBm input. (c) LG in −5 dBm input.

For comparison, another front-end without a balun is also taped out. In this chip, the output of the LNA is an LC tank, and one input of the double-balanced mixer is ac-coupled to ground for single-to-differential conversion. Table 2 shows the compared test results of the two chips. As can be seen, the use of a balun greatly helps to improve the performance of the front-end.

4. Conclusion

A novel low-power, low-noise and highly linear front-end for a 2.4-GHz wireless communication receiver has been presented. In this design, BiCMOS technology is used. However, the same technique can be used in CMOS as well. The front-end receiver uses only one balun for both power transmission and the single-to-differential conversion between LNA and mixer. The high linearity of –15 dBm and the low noise figure in high gain mode proves the advantage of the technique of single-to-differential conversion. The novel three-gain LNA achieves low-noise and high linearity simultaneously. The on-chip balun is simulated using the HFSS three-dimensional simulation tool and tested on-wafer. The on-wafer test results prove good characteristics for the application. The total front-end chip consumes 33 mW of power under 2.85-V supply.

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