A novel monolithic ultraviolet image sensor based on a standard CMOS process

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Abstract: We present a monolithic ultraviolet (UV) image sensor based on a standard CMOS process. A compact UV sensitive device structure is designed as a pixel for the image sensor. This UV image sensor consists of a CMOS pixel array, high-voltage switches, a readout circuit and a digital control circuit. A 16 × 16 image sensor prototype chip is implemented in a 0.18 μm standard CMOS logic process. The pixel and image sensor were measured. Experimental results demonstrate that the image sensor has a high sensitivity of 0.072 V/(mJ/cm^2) and can capture a UV image. It is suitable for large-scale monolithic bio-medical and space applications.

Key words: UV image sensor; standard CMOS process; floating gate

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1. Introduction

Solid state ultraviolet (UV) image sensors have attracted increasing interest for both civilian and military applications. Wide band gap semiconductor materials[1−6] are usually used to fabricate UV image sensors because the UV wavelength is relatively short. They have advantages of wavelength selectivity and high responsivity with low dark current. In practical applications, the signal of the UV image sensor should be outputted by a CMOS readout circuit. As a result, flip bonding technology should be used to connect the image sensors with the readout chip. Moreover, a sensor has wide performance variations from batch to batch and is difficult to manufacture in mass. Recently, silicon-based UV detectors have been studied for some applications, such as space ionizing radiation detection[7−10], personal radiation protection[11], semiconductor process control[12] and biological detection[13−15]. Silicon-based UV detectors can be integrated with readout circuits and signal processing circuits on one single chip. Recently, a monolithic UV detector based on a Si CMOS process has been proposed by the Bruno Riccò group from the University of Bologna, Italy[16]. However, no reference is available for this kind of UV sensor array so far. One of the challenges for silicon-based UV detectors is to develop monolithic UV image sensors in a standard CMOS process.

This paper presents a silicon-based monolithic UV image sensor based on a standard CMOS process. The sensor consists of a UV pixel array, a control logic circuit, a row decoder, a column decoder and image output modules. This compact architecture can be embedded into other systems.

2. UV image sensor architecture

The architecture of the proposed UV image sensor is schematically shown in Fig. 1. It consists of a sensor array, a control logic circuit, a row decoder, a column decoder and image output blocks. The sensor consists of 16 × 16 pixels. The pixel has three operation modes: reset, exposure to UV and readout. The logic block provides the timing and control signals for other blocks and generates the synchronization with an external data acquisition system. The column decoder and the row decoder generate the 16-bit address of the pixel array. An image output stage is to readout the analog signal of every pixel and output it.

3. Design of the UV sensor pixel

The UV sensitive pixel is formed by a Si–SiO_2–polySi (Floating-gate (FG))–SiO_2–Si device. A simple band diagram of this pixel is shown in Fig. 2. It is well known that the photon energy threshold is about 3.2 eV for photoemission from the bottom of the conduction band of Si to the conduction band of SiO_2, corresponding to UV with a 388 nm wavelength. Therefore, electrons can be erased when the FG is illuminated by UV light with a wavelength of shorter than 388 nm. Firstly, electrons are injected into the FG through Fowler–Nordheim (FN)

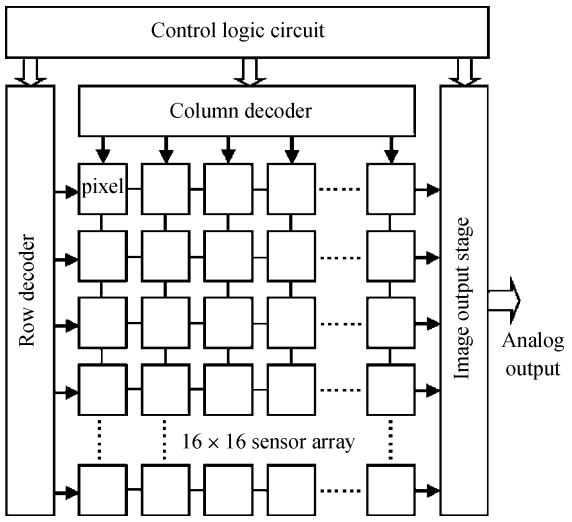

Fig. 1. Architecture of the proposed UV image sensor.

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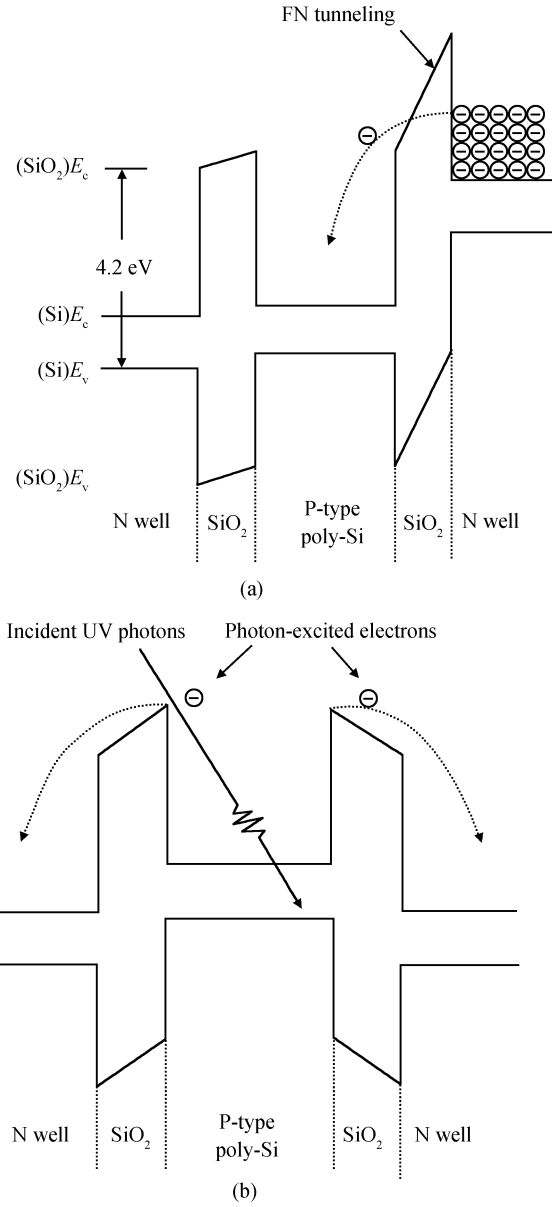

Fig. 2. Band diagram of the UV pixel. (a) Injecting electrons into the FG region. (b) Electrons exceed the bottom of the conduction band of SiO_2 into the Si region by UV photons.

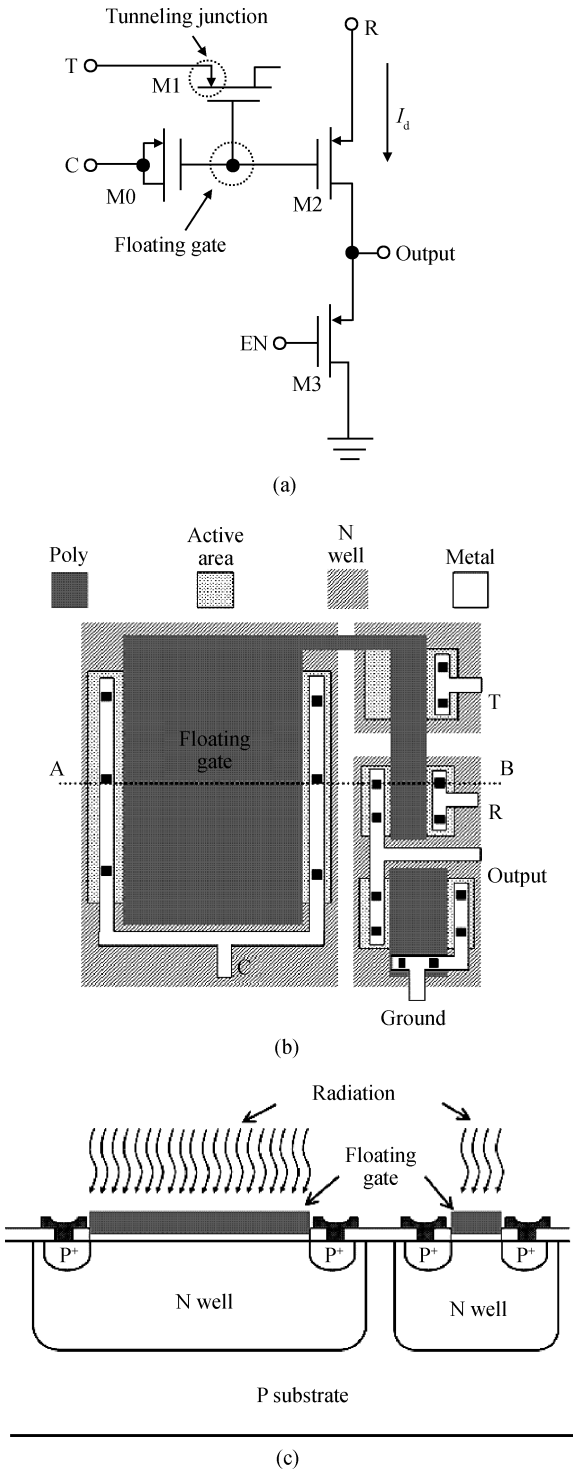

Fig. 3. (a) Schematic of the UV image sensor pixel. (b) Pixel layout. (c) Cross section of the pixel layout.

tunneling, as shown in Fig. 2(a). Then, as shown in Fig. 2(b), incident UV photons excite electrons to exceed the bottom of the conduction band of SiO_2 to enter the Si region. The current is approximately proportional to the intensity.

The schematic, layout and layout cross section of the sensor pixel are shown in Fig. 3. In the pixel, the gates of MOS transistors M0, M1 and M2 are interconnected to form a common poly-Si FG. The pixel consists of p-type transistors due to their lower $1/f$ noise performance. Transistor M0 is a control capacitor. Transistor M1 is used as an electron tunneling junction from node T to the FG. Transistors M2 and M3 are connected as a readout amplifier. Because the area of the FG over transistor M0 is much larger than that over transistors M1 and M2, the potential of the FG mainly depends on the number of electrons on the FG and the bias on node C. It is approximately given by

$$V_{FG} = V_C + Q_{FG}/C_{sum}, \tag{1}$$

where V_C is the voltage bias on node C, Q_{FG} is the amount of electric charge on FG, and C_{sum} is the whole capacitance of the FG.

In the pixel there are three operating modes: reset, UV radiation exposure and readout. Firstly, the pixel is reset by injecting electrons into the FG. In this step, the voltage on node

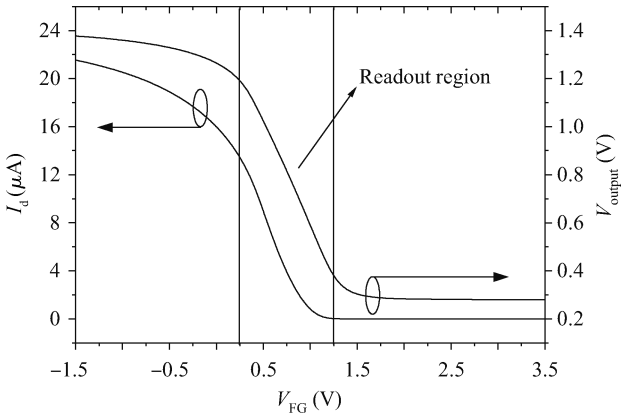

Fig. 4. Simulated results of the sensor pixel transfer characteristics.

C is high and the voltage on node T is 0. Secondly, the pixel is exposed to UV radiation for a fixed time and the electrons on the FG are erased. Thirdly, electrons on the FG are readout. A simulated result of the sensor pixel transfer characteristics is shown in Fig. 4. Figure 4 shows that V_{FG} should be biased in the linear region when the pixel is read. In this region, the output voltage is almost linear to the FG potential V_{FG}, as expressed by

$$V_{output} = \sqrt{\frac{W_2}{L_2}\frac{L_3}{W_3}}\,|V_{FG} - V_R - V_{THP}| - V_{THP}, \qquad (2)$$

where V_{output} is the output voltage of the sensor pixel, W_2 and W_3 are the widths of the M2 and M3 transistors, L_2 and L_3 are the length of M2 and M3, V_R is the voltage bias of node R, and V_{THP} is the threshold voltage of the P type transistor. Finally, we obtain the change of the number of electrons on the FG by comparing the output results before and after exposure to UV radiation. The difference between the output voltages is the readout result of the radiation intensity and it is given by

$$V_{readout} = \sqrt{\frac{W_2}{L_2}\frac{L_3}{W_3}}|\Delta Q_{FG}/C_{sum}|, \qquad (3)$$

where ΔQ_{FG} is the charge change on the FG. As a result, the intensity of incident UV radiation is detected using this UV sensor. A detailed theoretical analysis of the sensor pixel sensitivity is described in Ref. [17].

4. UV Sensor array and decoder design

A simplified schematic of the 16 × 16 sensor array circuit is displayed in Fig. 5. Similar to a sensor pixel, the sensor array also has three modes: reset, UV radiation exposure and readout. A row decoder and a column decoder serve to control the operations of the sensor array. The operating conditions are shown in Table 1. It should be noted that node C is biased to a proper voltage V_r to make two readout transistors be in saturation in read mode. The image output stage consists of traditional unit gain samplers[18].

As shown in Table 1, high voltage V_h and mediate voltage V_m are used in reset mode. For this reason, the row and column decoders should involve high voltage switches. A simple

Table 1. Operating conditions for different modes.

Node	C	T	R	EN
Reset	V_h	0	0	V_m
Exposure to UV	0	0	0	0
Read	V_r	0	V_{dd}	0

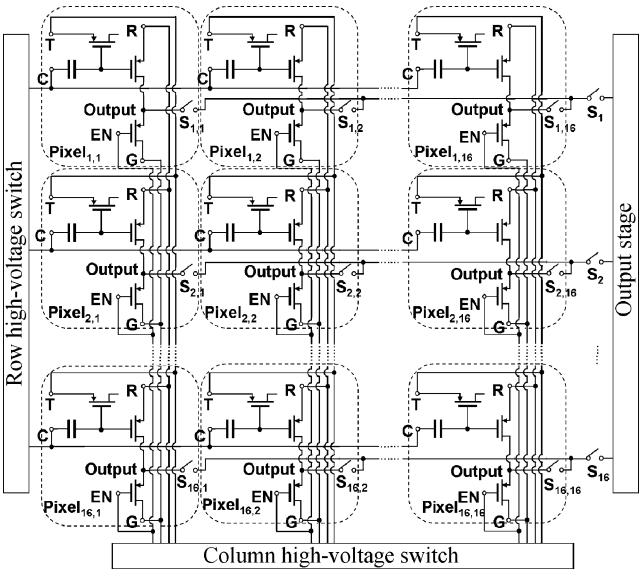

Fig. 5. Schematic of the 16 × 16 sensor array.

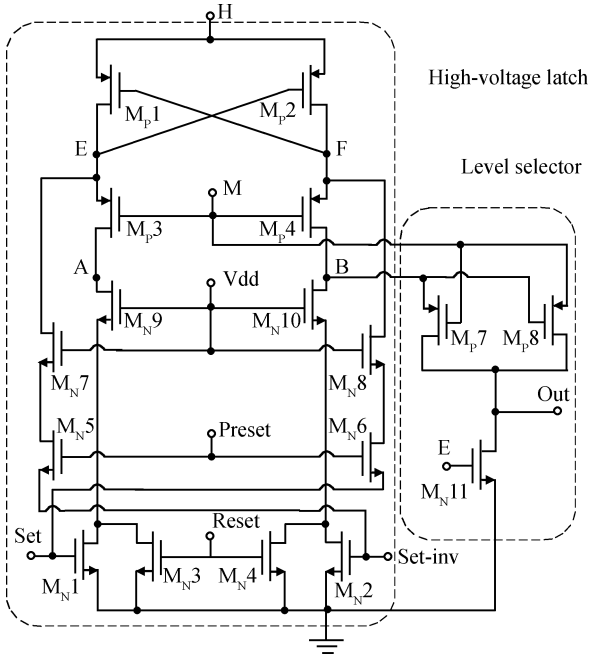

Fig. 6. A simple schematic of the high-voltage switch.

schematic of the high-voltage switch is displayed in Fig. 6. It consists of a high-voltage latch and a level selector. The clock timing waveforms of the high-voltage switch are presented in Fig. 7. In the high-voltage switch, NMOS transistors are specially designed in a standard CMOS process and more details are described in Ref. [19]. As shown in Fig. 7, the signal Set and signal Set-inv are complementary in the whole process. Firstly, the Reset signal is high and the voltage of nodes A and

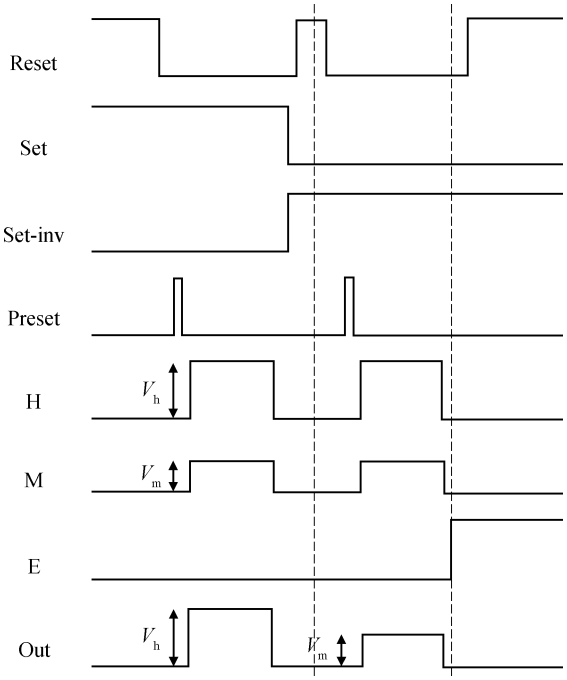

Fig. 7. Clock timing waveforms of the high-voltage switch.

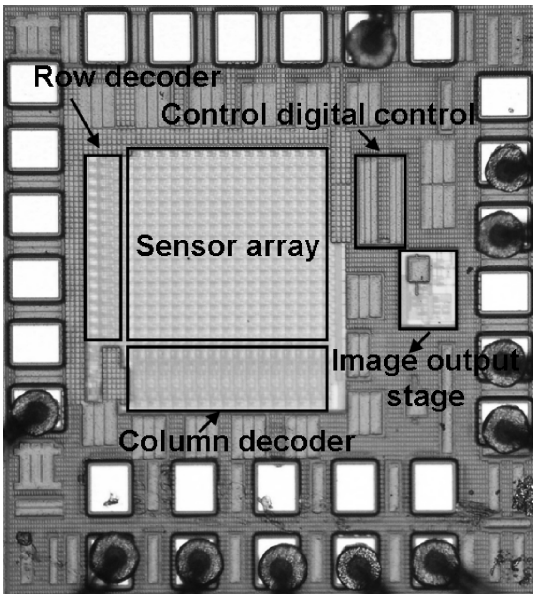

Fig. 8. Microphotograph of the UV image sensor.

B is pulled down to 0 to initiate the latch. Then the Reset signal gets low and a preset pulse is applied to make nodes E and F establish two complementary states. In the next step, high voltage V_h and intermediate voltage V_m are applied to nodes H and M, respectively. The voltages of nodes A and B are determined by the states of nodes Set and se-inv. Similarly, the voltage of node Out depends on the voltages of nodes M and B. Thus, the high-voltage switch can output three levels of voltage: high voltage V_h, intermediate voltage V_m and 0.

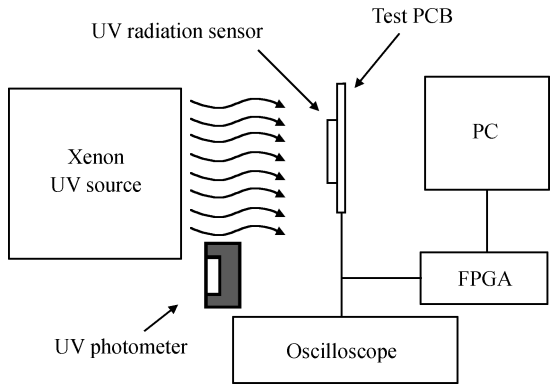

Fig. 9. Test platform for measurement of the UV sensor pixel.

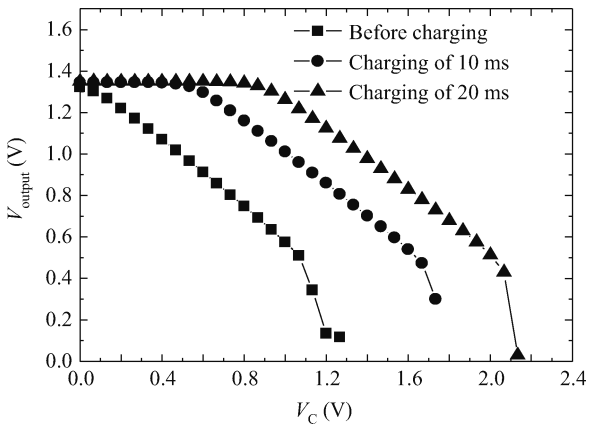

Fig. 10. Transfer characteristics of a UV sensor pixel with different charging times.

5. Implementation and measurement of the UV image sensor

A prototype UV image sensor chip with 16 × 16 pixels was fabricated in a 0.18 μm 1P6M standard CMOS process. The microphotograph of the prototype is shown in Fig. 8 and the area of whole sensor is 800 × 800 μm^2.

A test platform for measurement of the UV sensor pixel is schematically represented in Fig. 9. A Xenon lamp serves as the UV radiation source, characterized by a spectral distribution with emission values in a range of 250 to 300 nm. A photometer is placed directly before the UV radiation source to evaluate radiation intensity. In the experiment, a FPGA board controlled by a PC gives test signals to the chip and the measurement results are displayed on an oscilloscope.

Firstly, the transfer characteristics of the sensor pixel are measured. Figure 10 plots the transfer characteristics for two different pre-charge times of 10 ms and 20 ms. The shift of transfer characteristics for different pre-charging times means that different amounts of electrons are injected into the FG. When the output voltage decreases to a low enough value, the signal output stage can not operate properly and the output voltage drops suddenly. In the linear region, the sensor pixel linearity is about 99.8%. The experimental results show that the sensor pixel can operate more than 100000 times.

Secondly, we measured the UV sensitivity of the sensor pixel. First of all, the sensor pixel was pre-charged for 20 ms.

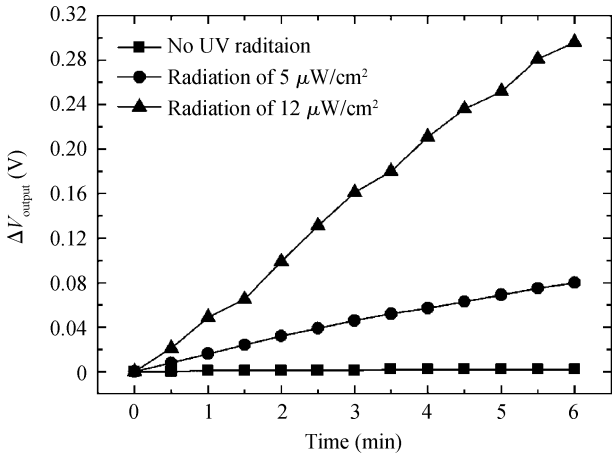

Fig. 11. Test results of sensor pixel exposed to UV radiation of different intensities.

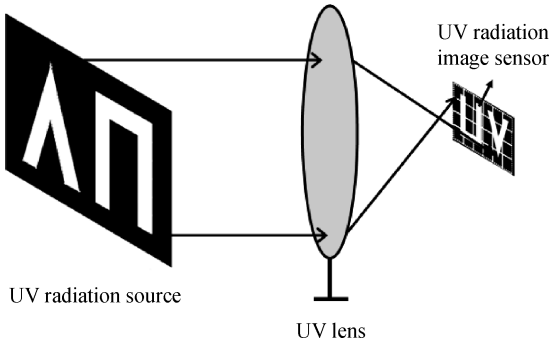

Fig. 12. Test platform for the UV image sensor measurement.

Then the sensor pixel was exposed to UV radiation with intensity of 12 μW/cm^2 and 5 μW/cm^2. During exposure, the potential change of the FG was measured in time intervals of 1 min with node C biased at 1 V. The test results are shown in Fig. 11. The figure shows that radiation with an intensity of 12 μW/cm^2 erased electrons from the FG and the output voltage decreased by 0.052 V/min. Similarly, when the sensor is exposed to UV radiation with an intensity of 5 μW/cm^2, the output voltage decreased by 0.013 V/min. Therefore, the sensor pixel sensitivity of the sensor pixel is about 0.072 V/(mJ/cm^2).

Finally, the UV image sensor was measured using the characters "UV" with UV radiation intensity of 6 μW/cm^2 in a darkroom. The test platform for this UV image sensor measurement is schematically displayed in Fig. 12. To obtain a larger-scale image, a 2-dimentional optical stage is used to adjust the 16 × 16 array into a 96 × 64 one by successively moving the UV image sensor 6 times in the row direction and 4 times in the column direction in the focal plane.

The experimental process is similar to that for the measurement of the sensor pixel. First of all, electrons on the FG of every pixel are erased and then electrons are charged into the FG. This operation is to make the number of electrons on the FG in every pixel almost the same. After that, the electrons on the image sensor are readout. Secondly, the sensor is exposed to the character image for 5 min. In this process, a different amount of electrons are erased by UV radiation with different intensities for every pixel. At the same time, the electrons on every pixel are readout again. Then, the image of the "UV" characters gets through by subtracting the first readout result from the second one. Figure 13 shows the measured image of the "UV" characters with ultraviolet radiation.

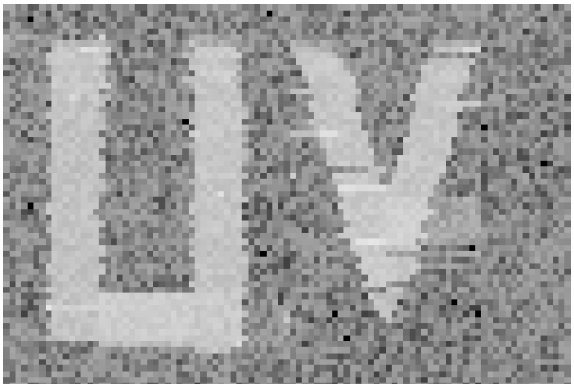

Fig. 13. Captured image of the characters "UV" with ultraviolet radiation.

Table 2. Parameters of the UV image sensor.

Parameter	Value
Technology	0.18 μm 1P6M CMOS Std.
Chip size	800 × 800 μm^2
Pixel size	17 × 17 μm^2
Number of trans./pixel	4T
Fill factor	41%
Sensitivity	0.072 V/(mJ/cm^2)
Sensor pixel linearity	99.2%
Charging times	> 100000

In conclusion, the parameters of the UV image sensor in a standard CMOS process are listed in Table 2.

6. Conclusion

In this paper, we designed a novel monolithic FG UV image sensor in a standard CMOS process. The core of the image sensor pixel was a UV-sensitive device based on a single-poly FG MOSFET. This compact design can be integrated into a SOC with signal conditioning and data processing. A 16 × 16 image sensor prototype chip was implemented in a 0.18 μm single-poly standard CMOS process. Experimental results demonstrated that this sensor pixel has sensitivity of 0.072 V/(mJ/cm^2) and the image sensor can capture a UV image. It is suitable for future smart applications.

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