A highly linear baseband G_m–C filter for WLAN application

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Abstract: A low voltage, highly linear transconductance–C (G_m–C) low-pass filter for wireless local area network (WLAN) transceiver application is proposed. This transmitter (Tx) filter adopts a 9.8 MHz 3rd-order Chebyshev low pass prototype and achieves 35 dB stop-band attenuation at 30 MHz frequency. By utilizing pseudo-differential linear-region MOS transconductors, the filter IIP_3 is measured to be as high as 9.5 dBm. Fabricated in a 0.35 μm standard CMOS technology, the proposed filter chip occupies a 0.41×0.17 mm^2 die area and consumes 3.36 mA from a 3.3-V power supply.

Key words: wireless local area network; transconductance–C low-pass filter; linearity; linear-region MOS transconductors; pseudo-differential transconductors

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1. Introduction

The rapid development of battery-operated portable systems and the ever-increasing level of circuit integration call for low power and thus low supply voltage integrated circuit topologies. One possible solution to make circuit work under low voltage is to use a pseudo-differential structure.

In this paper, a highly linear G_m–C filter using a pseudo-differential transconductor topology designed as a baseband analog front-end wireless transmitter block is shown in Fig. 1.

The transmitter is based on direct conversion architecture that can be fully integrated on chip. The proposed third-order Chebyshev low-pass filter receives the signals from the baseband I and Q digital-to analog converters (DACs). The outputs of the low-pass filters are then applied to baseband programmable gain amplifiers (PGAs). The signals are then directly up-converted to RF frequency and combined before RF VGA, then amplified by a power amplifier driver (PAD). Since low power dissipation is greatly desirable in order to prolong the standby time of the WLAN system, circuit building blocks operating under low supply voltages should be developed.

In this paper, the filter design adopts a pseudo-differential structure to achieve high linearity and low power simultaneously. Since the pseudo-differential structure has low common-mode rejection in nature, a common-mode feed-forward circuit should be adopted to cancel the input CM signal, with an additional transconductor that responds to CM signals only. This paper describes in detail the core of the proposed G_m–C filter: the transconductor cell including CMFB and CMFF circuits, the transconductance–C integrator and the automatic tuning circuits.

2. Filter architecture

The proposed transconductor cell can be divided into three parts, as shown in Fig. 2. Part A is the G_m cell, Part B is the common-mode feedback circuit and Part C is the common-mode feed-forward circuit, respectively. In this section, we will introduce all of these building blocks first. Then the integrator of the 3rd low-pass filter and the automatic tuning system of the proposed continuous-time G_m–C filters are discussed.

2.1. G_m cell

The proposed G_m cell is shown in Fig. 3, in which two assistant amplifiers force transistors M1 and M2, whose drain voltages are equal to the reference voltage V_{tune} provided by the automatic tuning circuit output. These two transistors work in the triode region and the single-end output current I_{out1} can be calculated as

$$I_{out1} = \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{th}) V_{tune}. \quad (1)$$

Similarly, I_{out2} can be derived as

$$I_{out2} = \mu_n C_{ox} \frac{W}{L} (V_{in2} - V_{th}) V_{tune}. \quad (2)$$

Then the differential transconductance can be derived from Eqs. (1) and (2) as

$$G_m = \frac{I_{out}}{V_{in}} = \mu_n C_{ox} \frac{W}{L} V_{tune} = K V_{tune}, \quad (3)$$

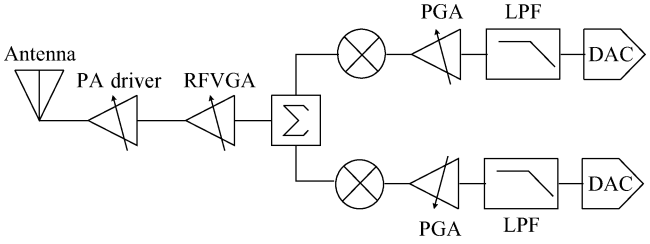

Fig. 1. Transmitter system of WLAN.

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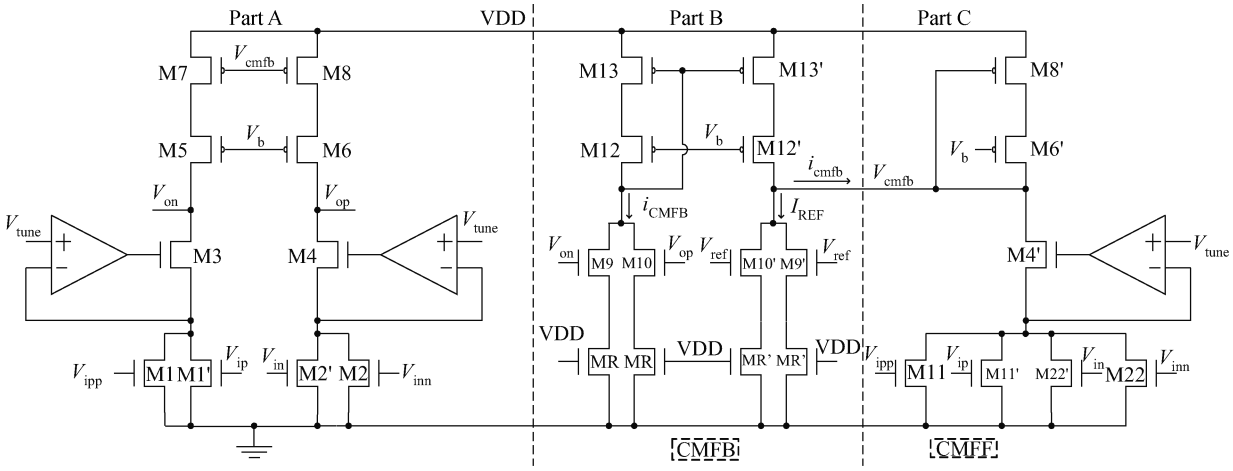

Fig. 2. The proposed G_m cell.

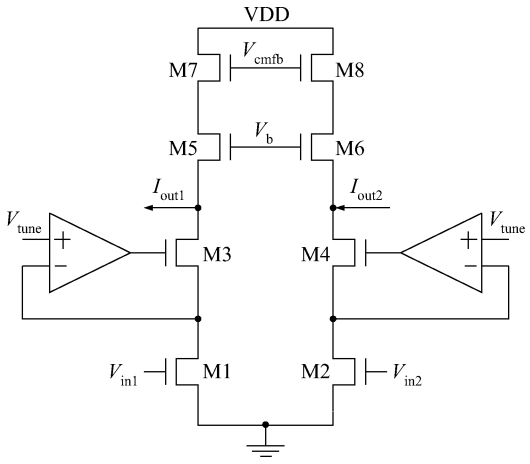

Fig. 3. Simplified schematic of the proposed G_m cell.

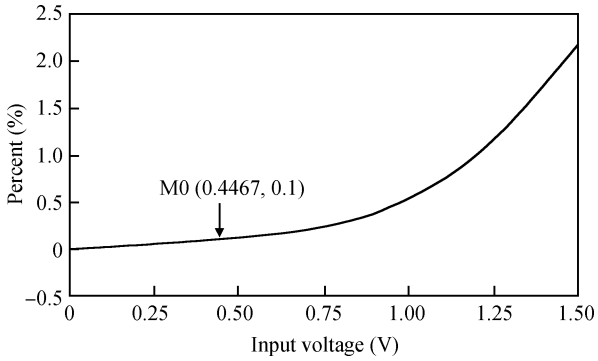

Fig. 4. Simulated THD at 100 kHz input frequency.

where $K = \mu_n C_{ox} \frac{W}{L}$ is constant.

Equation (3) shows that the transconductance has a linear relationship with the reference voltage V_{tune}. By controlling this tuning voltage V_{tune}, the filter transconductances and hence the filter corner frequencies can be changed linearly.

The same common-mode reference voltages are applied to each stage since they are directly DC coupled. As shown in Fig. 3, assuming the differential input voltages satisfy: $V_{in1} = V_{CM} + v_i$, $V_{in2} = V_{CM} - v_i$, the output voltages can be shown as follows: $V_{o1} = V_{CM} - v_o$, $V_{o2} = V_{CM} + v_o$, respectively. Where V_{CM} stands for the common-mode output voltages of the transconductors. To ensure that input transistors M1 and M2 work in the linear region, the tuning voltage should satisfy:

$$V_{tune} \leqslant V_{DD} - (V_{dsat5} + V_{dsat7}) - V_{thn}, \tag{4}$$

where V_{dsat} is the saturation voltage of an NMOS device, and V_{thn} is the threshold voltage of the NMOS transistor.

The gain of the filter is 0 dB, so the largest no distortion output signal is equal to the largest no distortion input signal in the passband, namely $v_{o,max} = v_{i,max}$. As a result, we can get

$$v_{i,max} = V_{DD} - V_{CM} - (V_{dsat5} + V_{dsat7}). \tag{5}$$

Table 1. Comparison of performance with other transconductors.

Parameter	Ref. [1]	Ref. [2]	Proposed
Process (μm)	0.18	0.5	0.35
Power supply (V)	1.8	3.3	3.3
THD (dB, Vpp)	–62, 0.7	–60, 0.39	–60, 0.89
G_m (μS)	220–880	–	100–300
Linear input range (Vpp)	1.5	1.2	2

To achieve the largest input signal swing, as well as passband linearity performances, the common-mode reference voltage is chosen to be equal to one half of the supply voltage according to Eqs. (4) and (5). By applying this optimum common-mode reference voltage, the highest input amplitude of 1 Vpp can be attained. In Fig. 4, the simulated transconductor THD as a function of a 100 kHz input signal is plotted, which demonstrates that the input voltage swing of the proposed transconductor cell for –60 dB THD is larger than 0.89 Vpp.

Table 1 compares the performances of the proposed transconductor cell with the referenced works. All of the listed transconductor cells are working in the triode region, among which the proposed transconductor has the widest linear input range to achieve high linearity.

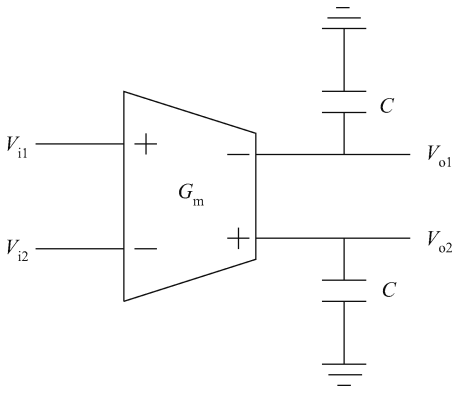

Fig. 5. Integrator cell.

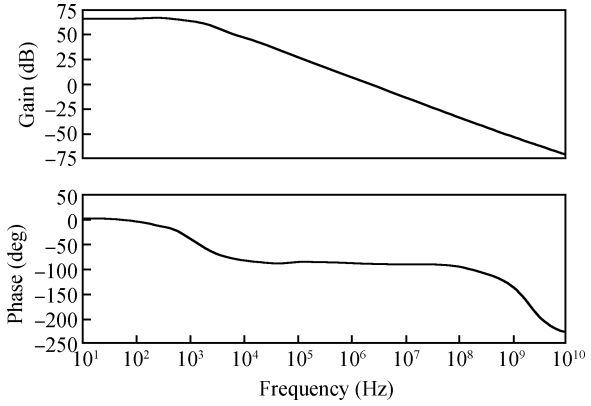

Fig. 6. Frequency response of the integrator.

2.2. Integrator

The transconductor–capacitor integrator is shown in Fig. 5. Its transfer function can be expressed as

$$H(s) = -\frac{A_{DC}}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)} = -\frac{G_m r_o}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)}, \tag{6}$$

where ω_1 stands for the dominant pole and ω_2 is the non-dominant pole. G_m is the transconductance and the output impedance $r_o = (g_{m3}r_{o1}r_{o3}) // (g_{m5}r_{o5}r_{o7})$. Equation (7) shows the relationship between ω_1 and the unity-gain frequency ω_0:

$$\omega_1 = \frac{\omega_0}{A_{DC}} = \frac{1}{r_o C}, \tag{7}$$

where $\omega_0 = \frac{G_m}{C}$.

The finite DC gain of the transconductor can introduce phase lead at the unity-gain frequency, which will result in filter Q and passband gain degradation. In addition, the non-dominant poles formed by the parasitic capacitances of the internal nodes introduces excess phase shift and causes Q enhancement and endangers the stability of the G_m–C filter. Since the Q enhancement may result in filter oscillation, the phase lag of the integrator must be designed to be small enough to guarantee stability.

In this paper, the proposed transconductor makes use of a cascode structure with the DC gain of the transconductor being more than 1000—enough to render the integrator phase lead negligible.

The transistor sizes of the transconductor cell must be carefully chosen in order to keep the parasitic capacitances as small as possible, not only for minimizing the phase lag but also because they are unpredictable and nonlinear, which can degrade the capacitance-matching accuracy.

The simulated frequency response of the proposed integrator is shown in Fig. 6. The DC gain of the proposed transconductor is 66 dB, which is sufficient to prove that the phase lead caused by the integrator finite gain is small enough. The frequency of the non-dominant pole is situated at larger than 10 GHz, making the phase lag negligible. The simulated phase lag of the proposed integrator is only 0.3° and can guard the proposed 3rd order Chebyshev filter from oscillation.

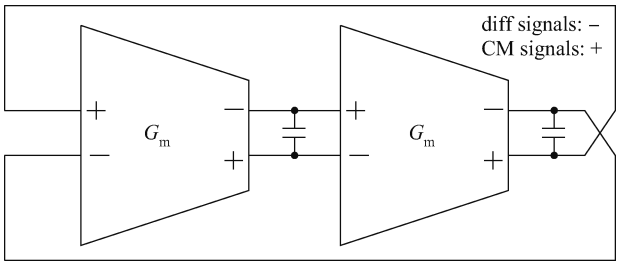

Fig. 7. Two integrators feedback loop.

2.3. Common-mode control circuit

When the power supply voltage becomes increasingly lower for power dissipation considerations, pseudo-differential structures are more frequently used to gain more signal swings.

Since a pseudo-differential structure has the same transconductance for both a differential and common-mode signal, circuits based on such structures require careful control of their common-mode behaviors[2, 3]. For example, as shown in Fig. 7, a cross-couple is not effective for a common-mode signal and a common-mode positive feedback loop exists. Meanwhile, this common-mode positive loop may have a voltage gain larger than unity, which will cause instability of the filter common-mode loop. As a consequence, to ensure stability it is necessary to develop a solution that is able to reject the common-mode signal in order to reduce the gain of the positive common-mode feedback loop. One possible way of rejecting the common-mode input signal is based on cancellation of the common-mode transconductance by an additional feed forward transconductance[4], as is shown in Fig. 8.

In Fig. 8, the principle of decreasing the common-mode loop gain by canceling the common-mode transconductance is illustrated by adding a parallel transconductor G_{CMFF} whose common-mode transconductance is equal in magnitude to that of the original one G_m and the differential transconductance is equal to zero. Then the common-mode transconductance could be cancelled to the first order while the differential mode signal remains intact.

The common-mode rejecting circuit that implements the principle in Fig. 8 is shown in Fig. 2. This circuit is made up of two parts: part C is an adaptive bias circuit and a common-mode feed forward (CMFF) circuit to achieve common-mode

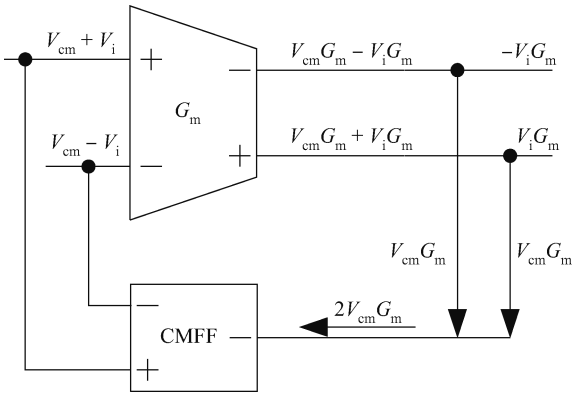

Fig. 8. Principle of feed forward CM cancellation.

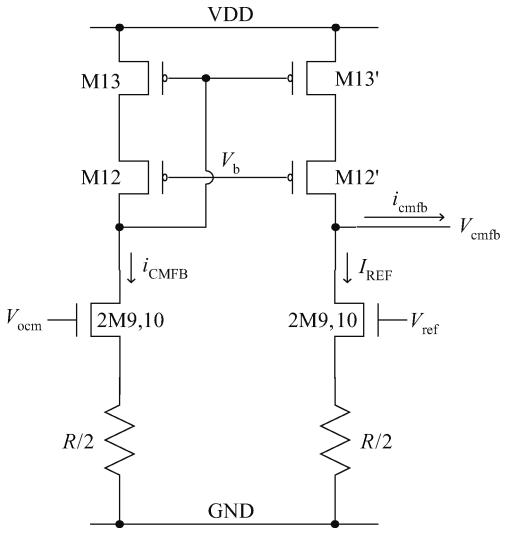

Fig. 9. CMFB equivalent circuit.

signal cancellation and to lower the common-mode loop gain; part B is a common-mode feedback (CMFB) circuit to define the common-mode voltages of the proposed transconductors[5]. A simplified open loop equivalent circuit for the CMFB is shown in Fig. 9. This circuit compares the output common voltage with the common-mode reference voltage V_{ref} and converts the voltage difference into the CMFB correction current.

$$i_{cmfb} = i_{CMFB} - I_{REF} \approx \frac{2g_{m9,10}}{1+g_{m9,10}R}v_{ocm}, \tag{8}$$

where R is the drain–source resistance of the transistor MR working in linear region, and v_{ocm} is the output common-mode error voltage.

A simplified equivalent circuit for the CMFF is shown in Fig. 10. In the CMFF circuit, the CMFF bias is a replica of the input transistor branch, except that the dimensions of input transistors M2 and M2' are one half of the original transconductor's input transistors (M1 and M2 in Fig. 3). Transistors M2 and M2' in Fig. 10 are connected to the inputs of the transconductor and driven by the tuning voltage, which is used to replicate the current and to cancel the common-mode input signals.

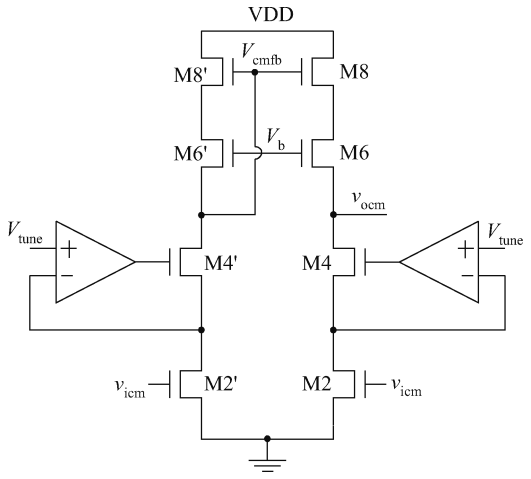

Fig. 10. CMFF equivalent circuit.

2.4. Filter circuit

The circuit topology of the proposed 3rd order Chebyshev low-pass filter is shown in Fig. 11. The integrating capacitance can be split into two parts: one C_{com} as the common-mode compensation capacitance connecting between the output nodes and the common-mode feedback voltage V_{cmfb} as shown in Fig. 11. The other part C_{int}, connecting the positive and negative output nodes, represents the integrator capacitor banks. The cut-off frequency of the filter can be changed by changing the control words of these capacitance banks for WLAN b/g/n. Furthermore, to lower the power dissipation and to minimize the die size, transconductors connected to the same output nodes share the same load capacitors as well as the same common-mode feedback circuits.

2.5. Automatic tuning system

Accurate frequency response is demanded in order to achieve sufficient stop-band attenuation over power, voltage, temperature (PVT) and process variations. Without a frequency tuning mechanism, the cut-off frequency of an integrated filter generally can vary by more than $\pm 50\%$. So an automatic tuning system is indispensable.

A PLL based frequency-tuning system consisting of a phase comparator, a voltage controlled oscillator and a low-pass filter[6] is adopted in this paper, as shown in Fig. 12. The phase comparator compares the frequency of the signal coming out from the voltage controlled oscillator with that of the reference signal. Then the result of the comparator is sensed to the slave filter through a low-pass filter. The oscillation frequency of the voltage control oscillator is

$$\omega = \frac{1}{\sqrt{\dfrac{C_1C_2}{2G_mG_m}}}. \tag{9}$$

When this frequency is locked at the reference frequency, the center frequency of the slave filter is also locked at the reference frequency by using the same tuning voltage V_{tune}.

The negative resistor is used to tune the amplitude of the second-order harmonic oscillator since harmonic distortion

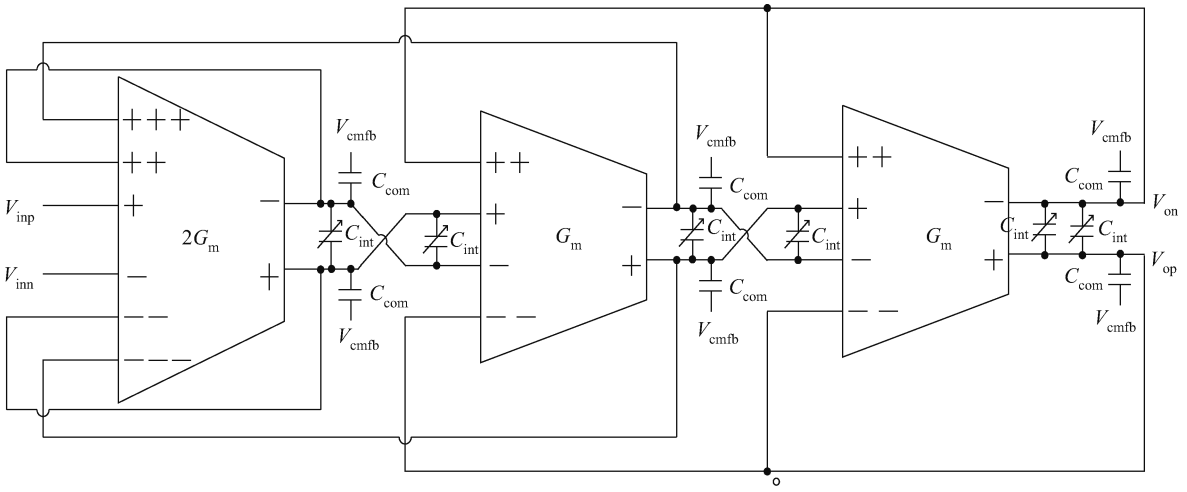

Fig. 11. 3rd order Chebyshev low-pass filter.

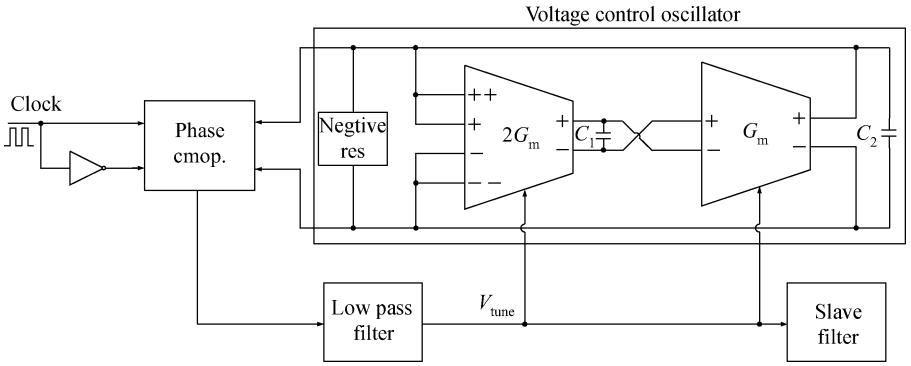

Fig. 12. Frequency-tuning system of the proposed filter.

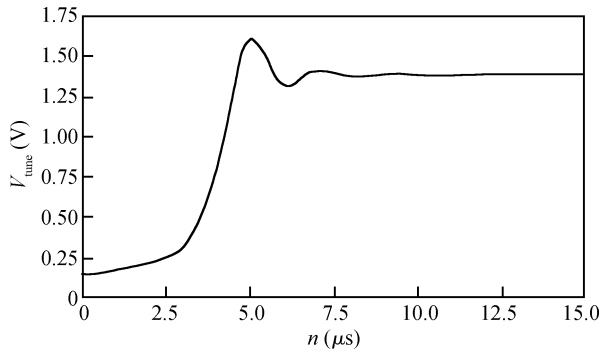

Fig. 13. Simulation result of the tune system.

and nonlinearities in the transconductors would shift the effective oscillation frequency, thus introducing a tuning error.

The main problem in this architecture is the implementation of the voltage controlled oscillator that is well matched to the filter to be tuned. So for good matching properties between the slave filter and the oscillator, the latter was built around a specific two-integrator loop that has been implemented using the same unit transconductance elements and with approximately the same parasitic-to-functional capacitor ratio and layout disposition. The capacitors use a voltage control oscillator and the slave filter has the same material capacitors.

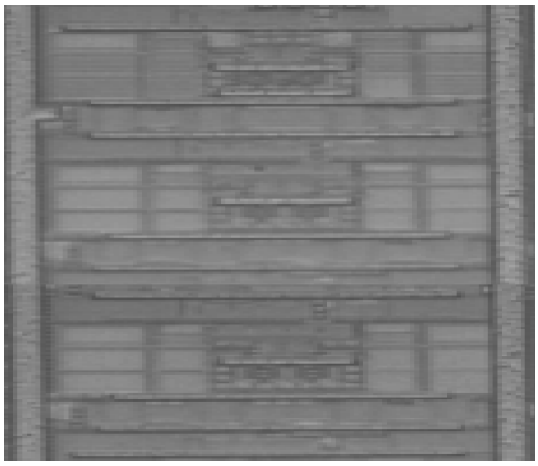

Fig. 14. Die photograph of the proposed filter.

The simulation result of the tuning system is shown in Fig. 13 and the tuning voltage is locked at 1.378 V.

3. Experimental results

Fabricated in a 0.35 μm standard CMOS technology, the propose filter occupies 0.41 $\times$ 0.17 mm^2 active area. Its die photograph is shown in Fig. 14.

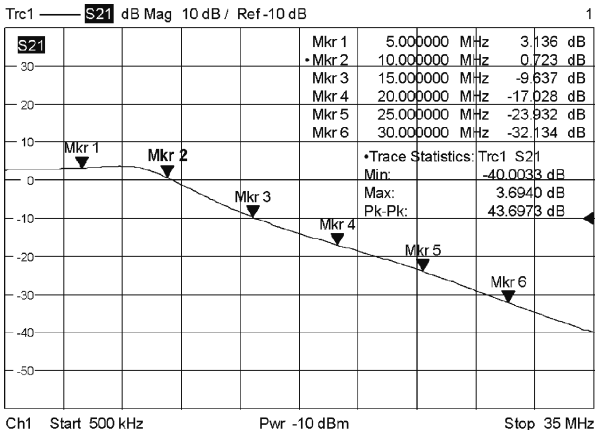

Fig. 15. Frequency response of the filter.

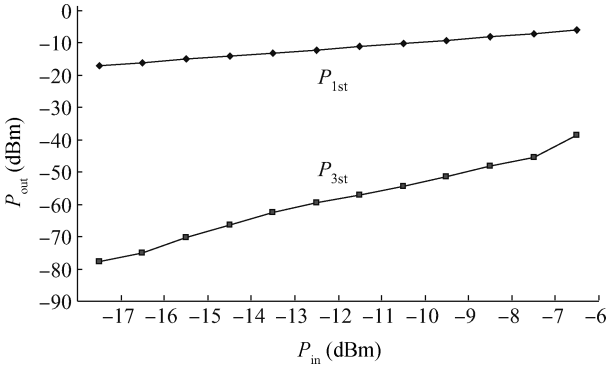

Fig. 16. Input IIP_3 plot of the filter.

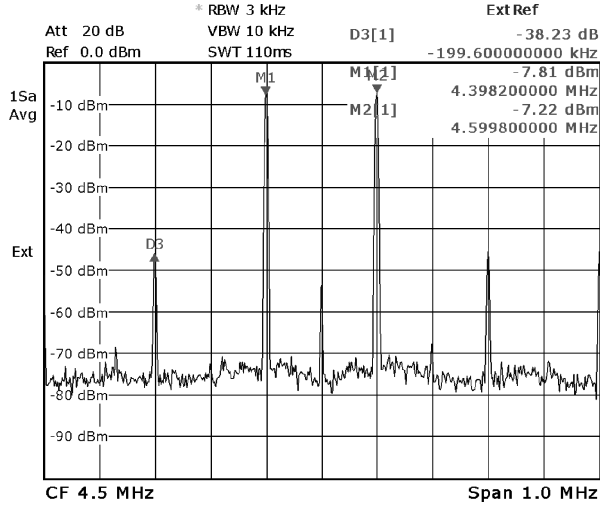

Fig. 17. Filter's P_{IIP3} at 4.4 MHz and 4.6 MHz.

The proposed G_m–C filter operates with a 3.3 V voltage supply and consumes 3.36 mA. The measured frequency response of the filter is shown in Fig. 15, where the measured cut-off frequency is 9.8 MHz when the tuning voltage V_{tune} is locked to 1.36 V. The stop-band attenuation of the 3rd Chebyshev low-pass filter is measured to be over 35 dB at 30 MHz.

During the linearity test of the proposed G_m–C filter, a test buffer of 3.5 dB gain and 19 dBm IIP3 is added to drive the spectrum analyzer. The input IIP3 plot of the filter is shown in Fig. 16. The filter's P_{IIP3} for input test two-tone at 4.4 MHz and 4.6 MHz are shown in Fig. 17. Since the power divider has 3 dB attenuation and the buffer's gain is 3 dB, the P_{IIP3} of the filter can be calculated as

$$P_{\mathrm{IIP3,1}} = -10\lg\left(10^{-0.9} - 10^{-1.9}\right) = 9.5\,\mathrm{dBm}. \quad (10)$$

The overall experimental results of the proposed filter are summarized in Table 2.

Table 2. Summary of the experimental results.

Parameter @ 25 ℃	Experimental result
Technology	TSMC 0.35 μm
Filter prototype	3rd Chebyshev
Supply	3.3 V
Power drain	3.36 mA × 3.3 V
Passband gain	–0.36 dB
Cut-off frequency	9.8 MHz (V_{tune} = 1.36 V)
Stop-band attenuation	$3f_c$ > 35 dB
P_{IIP3}	9.5 dBm
Area	0.41 × 0.17 mm^2

4. Conclusion

This paper proposes a continuous time filter with an on-chip automatic frequency tuning circuit for use in a wireless radio frequency transmitter chip. To meet the WLAN transmitter system specifications, the proposed filter adopts a 9.8 MHz 3rd-order Chebyshev low pass prototype and achieves 35 dB stop-band attenuation at 30 MHz frequency. By utilizing pseudo-differential linear-region MOS transconductors, the filter IIP_3 is measured to be as high as 9.5 dBm. Fabricated in a 0.35 μm standard CMOS technology, the proposed filter chip occupies a 0.41 × 0.17 mm^2 die area and consumes 3.36 mA from a 3.3-V power supply.

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