An improved single-loop sigma–delta modulator for GSM applications*

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Abstract: Traditional feedforward structures suffer from performance constraints caused by the complex adder before quantizer. This paper presents an improved 4th-order 1-bit sigma–delta modulator which has a simple adder and delayed input feedforward to relax timing constraints and implement low-distortion. The modulator was fabricated in a 0.35 μm CMOS process, and it achieved 92.8 dB SNDR and 101 dB DR with a signal bandwidth of 100 kHz dissipating 8.6 mW power from a 3.3-V supply. The performance satisfies the requirements of a GSM system.

Key words: sigma–delta modulator; low-distortion; CDS; switched-capacitor circuit; delayed input feedforward
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1. Introduction

The global system for mobile communications (GSM), which originated from groupe spécial mobile developed by CEPT, has become the most popular standard for mobile communication all over the world, and analog-to-digital converters (ADCs) are one of the key modules in a GSM system. As used for GSM standard, 80–90 dB high dynamic range (DR) and 100 kHz bandwidth are required[1]. Based on the above specifications, sigma–delta ADCs are no doubt the most appropriate structures among all kinds of ADCs because of their inherent tradeoff between high resolution and bandwidth along with low power. A sigma–delta ADC is made up of an anti-alias filter, a sigma–delta modulator and a decimator, among them, the modulator determines its performance, so this paper focuses on researching the modulator.

The effective number of bits (ENOB) required for an ideal Nyquist-rate ADC to achieve the same resolution as an ideal sigma-delta ADC could be defined as[2]:

$$\mathrm{ENOB_{bits}} = \log_2 \frac{(2^B - 1)(2L + 1)^{1/2} R^{L+1/2}}{\pi^L}, \quad (1)$$

where L, R and B denote the modulator order, the oversampling ratio and the number of bits in the quantizer, respectively. According to Eq. (1), increasing L, R or B are all strategies to improve the ENOB. However, a simple high-order gives rise to stability problems, a large oversampling ratio is impractical for wideband applications, and then, to reduce the linearity requirements of a multibit feedback DAC, dynamic element matching (DEM) techniques are generally needed but they suffer from both complexity and the occurrence of unwanted spectral tones. Considering the requirements of resolution, bandwidth and low circuit complexity, a 4th order, 1-bit modulator with $R = 128$ has enough design margins for GSM applications.

As for the topologies, cascaded architectures have displayed advantages in high-resolution and wideband applications, but more stringent matching and integrator leakage requirements consume more power and die area. Meanwhile, continuous-time implementations are appropriate due to their high speed, but clock jitter, excess loop delay and a large time constant shift restrict their available resolution. For the purpose of satisfying the GSM high-resolution and near wideband requirements, a single-loop single-bit discrete-time topology should be a highly power-efficient choice because of its reduced building block sensitivity, low circuit complexity and high performance. In this paper, an improved high-order single-loop sigma–delta modulator has been fabricated in a 0.35-μm CMOS technology. The integrated modulator achieves a 15-bit resolution over a signal bandwidth of 100 kHz. The prototype operates from a 3.3-V supply with a 25.6 MHz sampling rate and dissipates 8.6 mW of total power.

2. Proposed modulator architecture

To design a single-loop high-order stable sigma–delta modulator, an aggressive noise transfer function (NTF) that does not destabilize the modulator is essential for high resolution. In addition, taking circuit level design into consideration, a unity-gain signal transfer function (STF) has the great advantage of lowering the modulator sensitivity to circuit nonidealities[3, 4]. Figure 1 shows the linear model of a single-

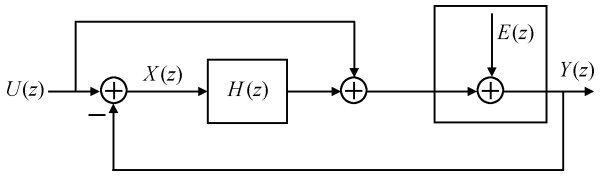

Fig. 1. Linear model of a single-loop feedforward sigma–delta modulator with an ideal feedback DAC.

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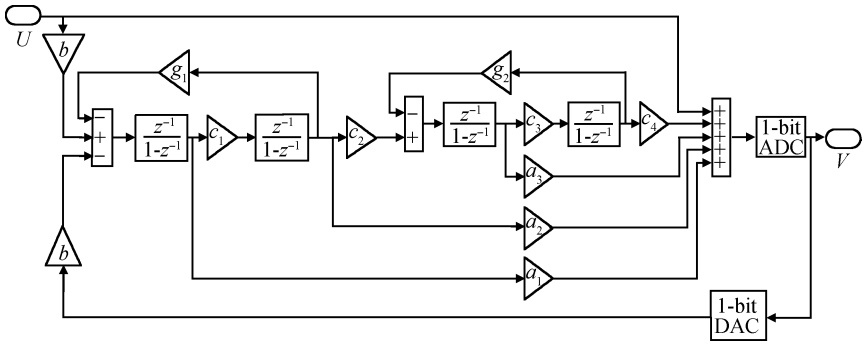

Fig. 2. Block diagram of the traditional 4th-order 1-bit CIFF sigma–delta modulator.

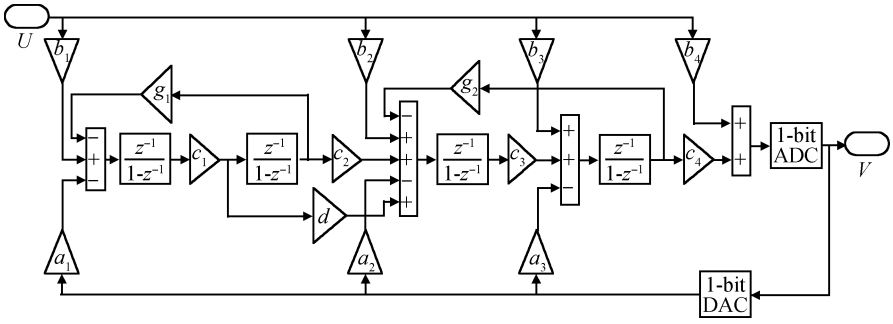

Fig. 3. Block diagram of a proposed 4th-order 1-bit unity-STF sigma–delta modulator.

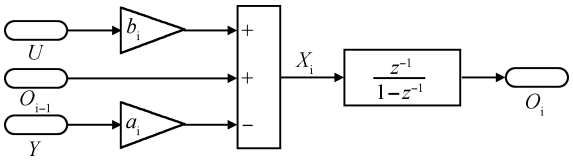

Fig. 4. Block diagram of the *i* th integrator with distributed feedback and feedforward input paths.

loop feedforward low-distortion sigma-delta modulator, where $H(z)$ is the loop filter, $U(z)$ and $E(z)$ are modulator's input signal and quantization error, respectively. The output can be shown as

$$Y(z) = \mathrm{STF}(z) \cdot U(z) + \mathrm{NTF}(z) \cdot E(z). \tag{2}$$

Since $\mathrm{STF}(z) = 1$, the error signal at the input of $H(z)$ can be represented as

$$X(z) = U(z) - Y(z) = -\mathrm{NTF}(z) \cdot E(z), \tag{3}$$

where $\mathrm{NTF}(z) = \frac{1}{1+H(z)}$.

As can be seen from Eq. (3), ideally, no input signal but only shaped quantization noise is processed by the loop filter so that the total harmonic distortion is suppressed. Consequently, integrators' signal swings inside the loop filter are reduced and more power efficient operational transconductance amplifiers (OTAs) can be designed.

The most universal structure used as a unity-STF sigma–delta modulator is the so-called cascade of integrators feedforward form (CIFF)[5] as displayed in Fig. 2. However, there are obvious drawbacks in this structure. Although the feedback DAC timing constraint is greatly relaxed by using 1-bit DAC, the additional signal summation implemented by active or passive adder is still required at the quantizer input. As shown in Fig. 2, for a 4th-order modulator, five paths are needed to be summed before the quantizer. As for the active adder, it means an extra power-hungry OTA is required. For the passive one, the parasites caused by a mass of extra capacitors and switches for the summation import signal attenuation lead to a reduced step of the quantizer threshold voltage and increased power dissipation[6]. Moreover, in a high-speed modulator, the additional long processing time of the signal summation operation would greatly alter the STF and NTF, resulting in a decrease in performance.

In order to conquer the drawbacks of traditional feedforward topology, the key is to simplify the adder before quantizer, i.e. to reduce the number of the input branches of the adder. For this, a capacitive input feedforward (CIF) structure[7] and an improved feedforward structure[8] were reported, but both of them need a power-hungry and impractical delay-free integrator as the last stage. Other structure proposed in Ref. [6] completely eliminates the adder before quantizer using SGF transformation, however, two input delay paths imported result in difficulties to implement and unity-STF is also changed. Thus, as shown in Fig. 3, an improved structure using hybrid distributed feedback and distributed feedforward input paths along with local resonator feedback control topology has been proposed in this paper. In Fig. 3, the number of the adder's input paths has been reduced from five to two. Feedforward path d has been inserted to reduce the 1st integrator's output swing so that the requirements of its components can be relaxed. In addition, the feedback and feedforward branches of the 2nd integrator have been replaced by path d leading to a saving of the number switches and capacitors used. Also, be-

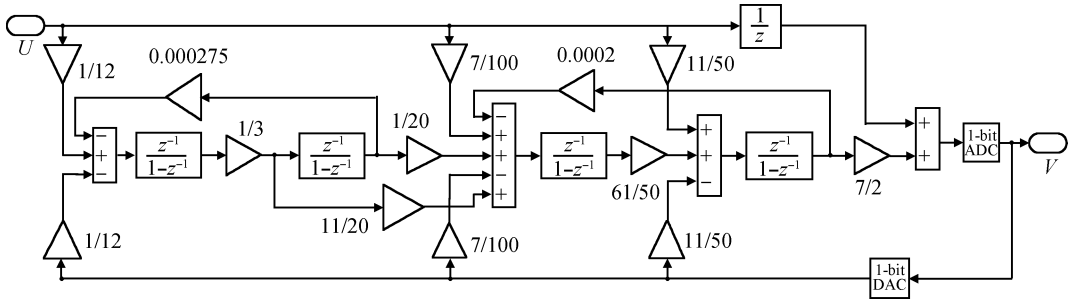

Fig. 5. Block diagram of the final proposed 4th-order 1-bit sigma–delta modulator.

cause of the 1-bit feedback realized by simple switch-capacitor branches, the a_2 and a_3 feedback paths will not burden the circuit complexity and time constraint.

The STF of the proposed modulator could be obtained by signal flow graph (SGF) and be shown as

$$\begin{aligned}\mathrm{STF}(z) &= \frac{N(z)}{D(z)} \\ &= \frac{N_4z^{-4}+N_3z^{-3}+N_2z^{-2}+N_1z^{-1}+N_0}{D_4z^{-4}+D_3z^{-3}+D_2z^{-2}+D_1z^{-1}+D_0},\end{aligned} \tag{4}$$

where

$$\begin{aligned}N_4 &= a_1b_4(1+c_1g_1+c_3g_2+c_1c_3g_1g_2) \\ &\quad + a_1c_4(b_2c_3-b_3-c_1db_1c_3-b_3c_1g_1 \\ &\quad + b_1c_1c_2c_3+b_2c_1c_3g_1),\end{aligned}$$

$$\begin{aligned}N_3 &= -a_1b_4(4+2c_1g_1+2c_3g_2) \\ &\quad + a_1c_4(3b_3-2b_2c_3+c_1db_1c_3+b_3c_1g_1),\end{aligned}$$

$$N_2 = a_1b_4(6+c_1g_1+c_3g_2)+a_1c_4(b_2c_3-3b_3),$$

$$N_1 = -4a_1b_4+a_1c_4b_3,$$

$$N_0 = a_1b_4,$$

$$\begin{aligned}D_4 &= a_1(1+c_1g_1+c_3g_2+c_1c_3g_1g_2) \\ &\quad + a_1c_4(a_2c_3-a_3-a_1c_1dc_3-a_3c_1g_1 \\ &\quad + a_1c_1c_2c_3+a_2c_1c_3g_1),\end{aligned}$$

$$\begin{aligned}D_3 &= -a_1(4+2c_1g_1+2c_3g_2) \\ &\quad + a_1c_4(3a_3-2a_2c_3+c_1da_1c_3+a_3c_1g_1),\end{aligned}$$

$$D_2 = a_1(6+c_1g_1+c_3g_2)+a_1c_4(a_2c_3-3a_3),$$

$$D_1 = -4a_1+a_1c_4a_3,$$

$$D_0 = a_1.$$

After comparing N_i with D_i $(i=0,\ldots,4)$, we can see that, when $a_i=b_i$ $(i=1,2,3)$ and $b_4=1$, the STF is exactly 1. Moreover, once the above conditions are satisfied, the input signal $X_i(z)$ to the ith integrator with distributed feedback and feedforward input paths, shown in Fig. 4, can be calculated using Eq. (3) as

$$\begin{aligned}X_i(z) &= O_{i-1}(z)+b_iU(z)-a_iY(z) \\ &= O_{i-1}(z)-a_i\mathrm{NTF}(z)E(z).\end{aligned} \tag{5}$$

Thus, the modulator's input $U(z)$ is completely removed from the input of the integrator. This conclusion could be used for the proposed structure shown in Fig. 3. The 1st, 3rd and 4th integrator all can be analyzed using Eq. (5) so that $U(z)$ is not present in the three integrators. Then, since the 1st integrator's output, which is the only input path of the 2nd one, does not have $U(z)$, there is also no $U(z)$ to be injected into the 2nd integrator. As for the two feedback branches g_1 and g_2, since their inputs (which are the output of the 2nd and 4th integrator respectively) do not include $U(z)$, they also will not introduce it to the loop filter. A detailed calculation for the inputs of all the integrators using SGF has also confirmed the above conclusion. Consequently, like the traditional CIFF form, the proposed modulator displayed in Fig. 3 also has characteristics of unity-STF and low-distortion.

Although the structure proposed in Fig. 3 maintains the advantages associated with traditional feedforward low-distortion sigma–delta modulators, very high speed circuit components have to be employed in the input feedforward and modulator feedback paths in order that the delay from the input through the overall modulator feedback path is zero, otherwise, the input signal can not be entirely removed from the loop filter. As a result, the overall power dissipation will increase.

For the purpose of relaxing the time constraints mentioned above, a full-cycle delay has been inducted in the b_4 path, i.e., a single sampling clock delay is introduced into the input feedforward path of Fig. 1, so that an extra half a sampling period could be obtained to perform summation, quantization and feedback operation[9]. Then, the NTF is unchanged and STF becomes

$$\mathrm{STF}(z) = \frac{z^{-1}+H(z)}{1+H(z)}. \tag{6}$$

In case of Lth noise shaping of the quantization error provided, then

$$\mathrm{STF}(z) = 1-(1-z^{-1})^{L+1}, \tag{7}$$

and

$$X(z) = (1-z^{-1})^{L+1}\cdot U(z)-\mathrm{NTF}(z)\cdot E(z). \tag{8}$$

Since $(L+1)$th-order difference shapes $U(z)$, the input component imported by the full-cycle delay can be ignored and the in-band STF is nearly flat owing to the oversampling, thus low-distortion can be hold.

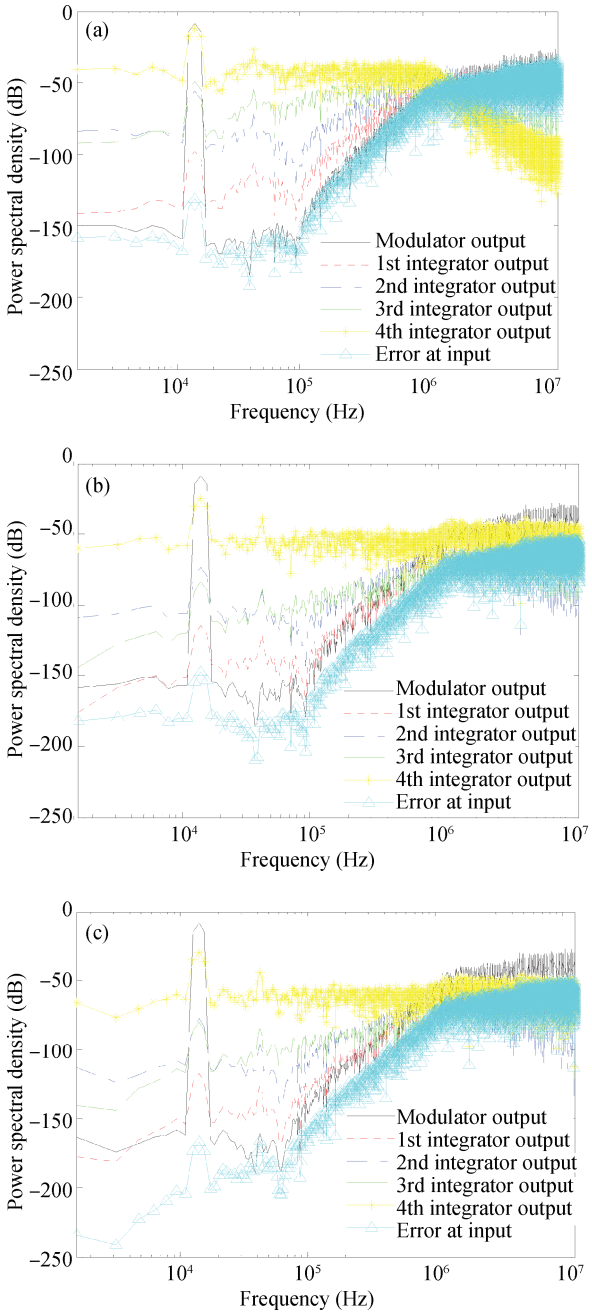

Fig. 6. Simulated output spectra of the 4th-order 1-bit sigma–delta modulators. (a) CIFF modualtor shown as Fig. 2. (b) Unity-STF modulator shown as Fig. 3. (c) Proposed modulator shown as Fig. 5.

The final structure with coefficients has been presented in Fig. 5. The coefficients were initialized by the well-known 'delsig' toolbox[10] with an inverse Chebyshev NTF whose maximum out-of-band gain is 1.5 for stability[5]. Then, equivalent transformations based on SGF and the scaling of internal nodes' signal swings were performed. Finally, all the coefficients, except for the two too small ones g_1 and g_2, were processed by rational approximations in order for switched capacitor circuit implementation.

The NTF of Fig. 5 can be calculated as

$$\mathrm{NTF}(z) = \frac{z^4 - 4z^3 + 6.0003z^2 - 4.0007z + 1.0003}{z^4 - 3.23z^3 + 3.9892z^2 - 2.2232z + 0.4699}. \quad (9)$$

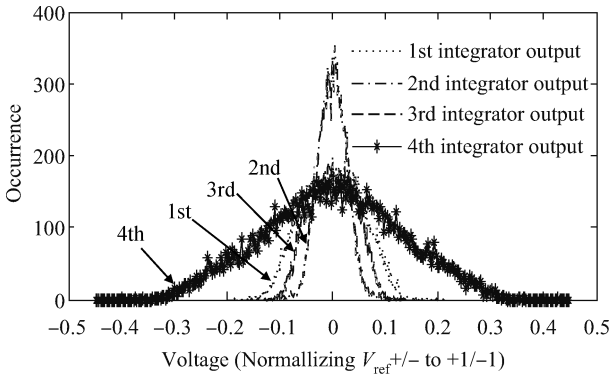

Fig. 7. Integrators' output swings of the proposed modulator as Fig. 5.

Owing to single-bit quantization, the modified Lee's approximate criterion[5] could be used to estimate stability. Using Eq. (9), we obtain

$$|\mathrm{NTF}(-1)| = 1.4664 < 1.5. \quad (10)$$

Since $|\mathrm{NTF}(-1)|$ is usually equal or close to the peak gain of $|\mathrm{NTF}(z)|$[5], from Eq. (10), we know that Lee's Rule is satisfied and modulator may operate stably.

Figure 6 displays the ideal spectra of each integrator output, error signal at the input of the loop filter and the overall modulator output for the structures shown in Figs. 2, 3 and 5, respectively, using 11.23 kHz and –3.8 dBFS sine wave input with 16 k samples. We can see that, even if the components of the loop filter are all ideal, the topologies shown in Figs. 2 and 3 still exhibit harmonic distortion. The reason is that the linear model of the modulator used for the above analysis could not respond to the extremely nonlinear quantizer block. When a nonlinear quantizer transfer function (QTF) is introduced, the input components of the modulator will appear in the loop filter and an input signal whose third harmonic lies at the passband edge leads to the most distortion[11]. Even so, as shown in Figs. 6(a) and 6(b), the input components emerging in the internal nodes are still very small, thus the low-distortion property is present. In addition, comparing Fig. 6(c) with Figs. 6(a) and 6(b), the delay imported in the quantizer feedforward path has little influence on the distortion suppression, thus the proposed structure also exhibits good low-distortion performance. Ideally, all the three modulators should present more than 19-bit resolution.

The histogram of integrators' output swings of the final proposed structure can be found in Fig. 7. The output swings of the first three integrators can be suppressed to less than 20% of the reference voltage. Although the output swing is more than double at the 4th integrator, the requirement of the last OTA can be relaxed in other circuit specifications because of the loop's noise shaping.

3. Circuit design

The proposed sigma–delta modulator shown in Fig. 5 has been realized by a fully-differential switched-capacitor circuit displayed in Fig. 8. The modulator is controlled by two phase, non-overlapping clocks: Φ_1 and Φ_2 for the sampling and integrating phase, respectively, and delayed clocks (Φ_{1d} and Φ_{2d})

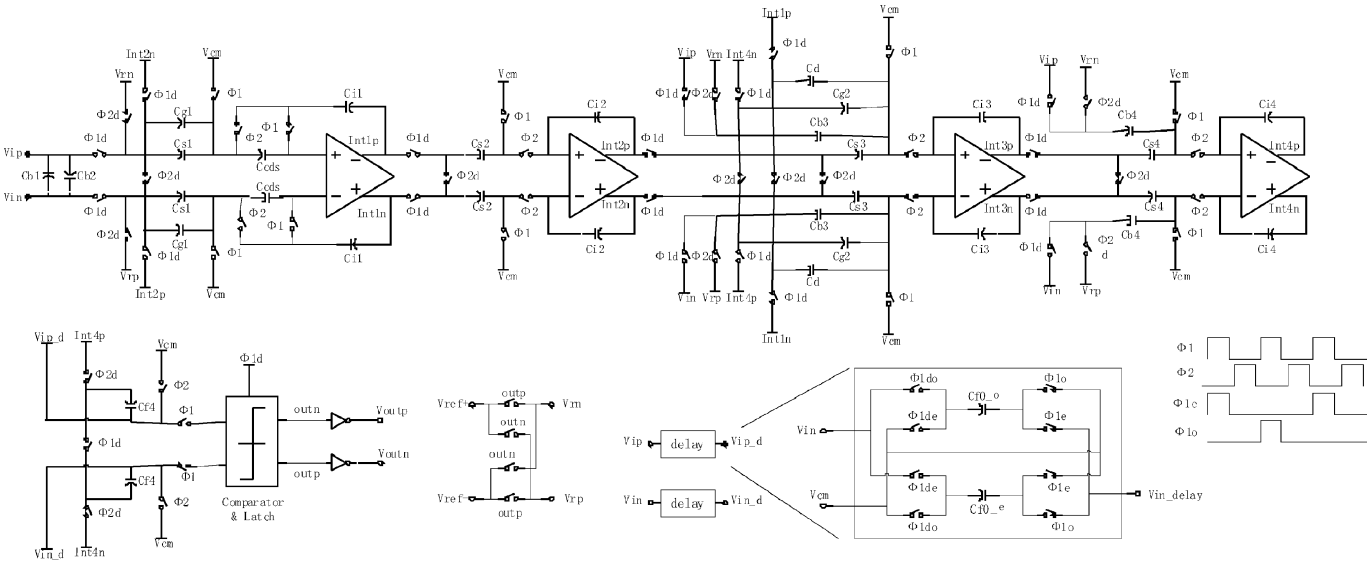

Fig. 8. Schematic of the proposed switched-capacitor sigma–delta modulator.

are used to reduce the effects of charge injection. The input and output common-mode voltage is set to $V_{DD}/2$. Then, the feedback reference voltages V_{ref+} and V_{ref-} are chosen as the single power supply rails V_{DD} (3.3 V) and ground. Then, the key building blocks are explained as follows.

3.1. Integrators

Since the 1st integrator dominates the performance of the overall modulator, high specification circuit components are required and, in addition, the correlated double sampling (CDS) technique, which is a particular case of autozero (AZ) technique based on sampling, is used to reduce the effect of the low-frequency noise, offset and finite DC-gain of OTAs. As shown in Fig. 8, the hold capacitor, C_{cds}, is used to store OTA's noise and offset. In general[12], C_{cds} is set to be C_i, and for a CDS integrator, the baseband component at low frequency of the input-referred noise spectrum is approximately:

$$S(\omega) \approx \left(\frac{\omega}{2f_s} + \frac{2C_p}{C_{cds}}\right)^2 \frac{\omega_0}{|\omega|}, \quad \frac{\omega}{f_s} \ll 1, \tag{11}$$

where C_p is the input parasitic capacitor, f_s is sampling frequency, and ω_0 is the flicker noise corner frequency. Hence, increasing C_i could minimize the flicker noise, moreover, also could enhance the settling speed during integration phase by small signal analysis[12].

Next, considering KT/C noise requirement of a fully differential switched-capacitor circuit, the sampling capacitor needs to satisfy[2]:

$$C_s \geqslant \frac{2kT \cdot \mathrm{SNR}}{(\mathrm{OL} \cdot V_{ref})^2 R}, \tag{12}$$

where OL is the overload level and SNR is the required signal-to-noise ratio. Using the parameters of this paper to Eq. (12), it is seen that a 0.153 pF sampling capacitor is enough for 16-bit resolution.

In view of the aforementioned, the OTAs' load capacity, the realization of resonators' small feedback coefficients, which were implemented by connecting larger capacitors available in series, and the design margin of real circuits, the final integrating capacitors of every integrator have been summarized in Table 1. In addition, sharing sampling capacitors and redundant switches techniques are used to save power and chip area.

Table 1. Integrating capacitors for each stage. Unit: pF.

Parameter	C_{i1}	C_{i2}	C_{i3}	C_{i4}
Value	12	6	10	5

Table 2. 1st OTA's performance (12 pF load capacitor).

Parameter	DC gain (dB)	GBW (MHz)	PM (degree)	SR (V/μs)	Output swing (V)
Value	50.4	114.4	65.1	75.3	$\pm$ 3.12

3.2. OTAs

The integrators have each been implemented using the two-stage OTA with a dynamic common mode feedback loop (CMFB), which is based on a switched-capacitor circuit and consumes no static current to sense the output common mode voltage and generate control voltage to balance OTA's differential outputs as shown in Fig. 9(a). The output and input common mode voltage were both set to be $V_{DD}/2$.

Table 2 shows the basic performance parameters of the OTA used in the first integrator, obtained from Fig. 9(b), with a 12 pF load capacitor. A behavior simulation presented over 17 bit resolution with this specification. Since the noise caused by the non-idealities of the latter integrator can be shaped by the preceding ones and smaller load capacitors have to be driven in the following stages, these OTAs can be implemented by smaller current consumption.

3.3. Clock generator

To generate the control phases for the input delay block, a clock generator has been proposed in Fig. 10. First, the period

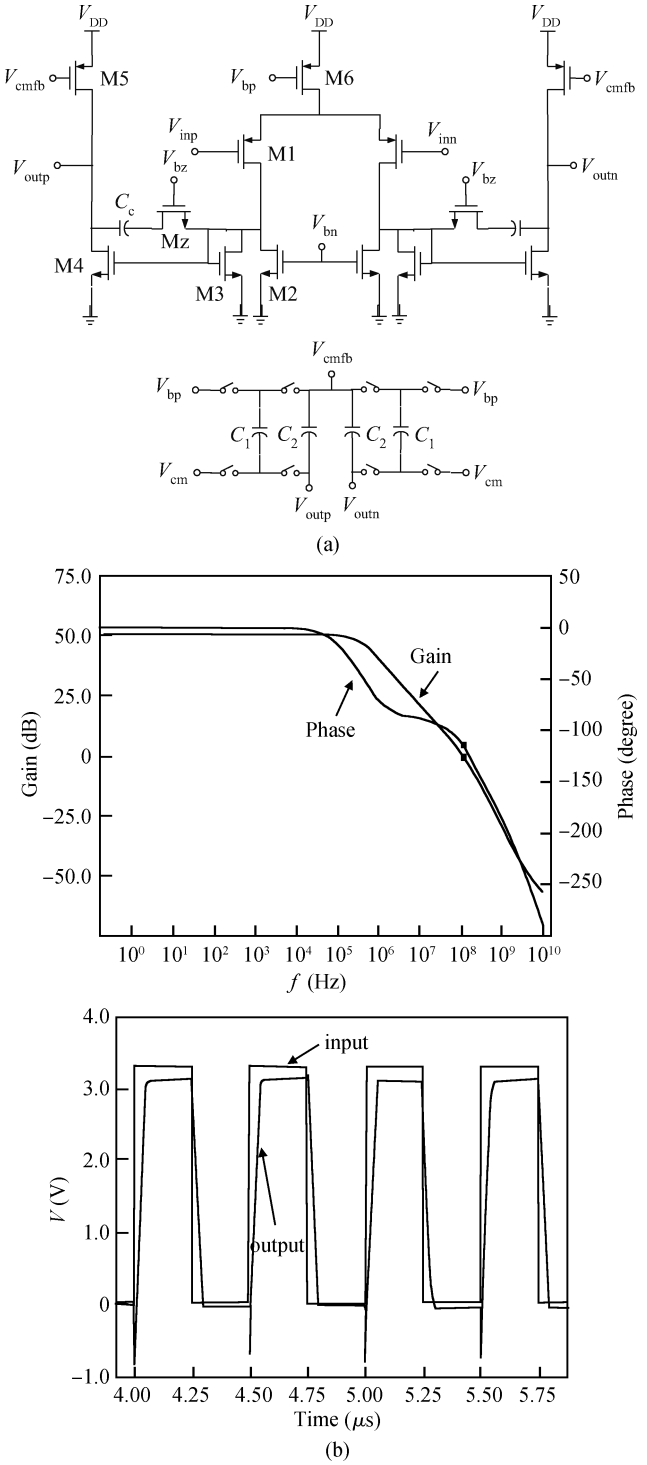

Fig. 9. (a) Schematic of the OTA with switched-capacitor CMFB. (b) Its frequency response (up) and transient simulation wave (down).

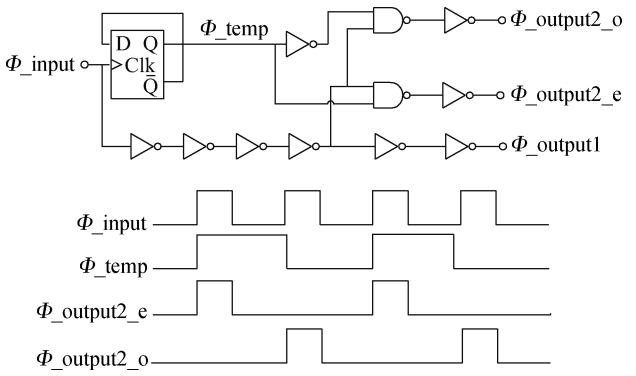

Fig. 10. Schematic and timing diagram of the clock generator for the input delay block.

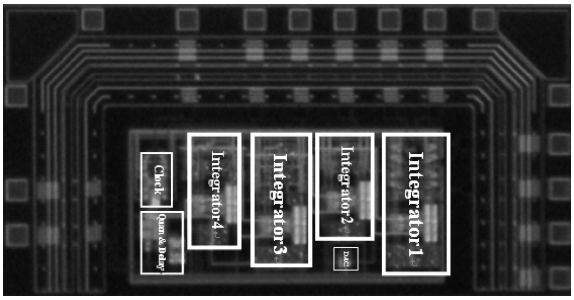

Fig. 11. Chip microphotograph of the proposed modulator.

Table 3. Modulator performance summary.

Parameter	Value
Supply voltage	3.3 V
Technology	Chartered 0.35 μm 2P4M CMOS
Sampling frequency	25.6 MHz
Oversampling ratio	128
Signal bandwidth	100 kHz
Peak SNR	100.2 dB
Peak SNDR	92.8 dB
Dynamic range	101 dB
ENOB	15.12 bits
Power consumption	8.6 mW
Core Area	1.2 × 0.6 mm^2
FOM	1.206 pJ/conversion-step

of the input clock $\Phi_{\_input}$ is doubled by a D flip-flop to generate $\Phi_{\_temp}$. Then, an and operation is performed between $\Phi_{\_temp}$ and $\Phi_{\_input}$, so $\Phi_{\_output2\_e}$ can be obtained. The same process could be used to produce $\Phi_{\_output2\_o}$ except an invert operation of $\Phi_{\_temp}$. The inverters employed in the $\Phi_{\_output1}$ path are used to generate delay for signal synchronization. As a result, $\Phi_{\_output2\_e}$ and $\Phi_{\_output2\_o}$ will only be efficient during every $\Phi_{\_output1}$ period. Simulations approved its efficiency for mid-frequency applications. Other two-phase non-overlapping clocks as shown in Fig. 8 were generated by a traditional clock generator as Ref. [2]. Consequently, there were 16 clock signals required in all to provide non-delayed, delayed, invert non-delayed, invert delayed clocks for the transmission gate switches and 8 clock control signals for the switches used for the input feedforward delay blocks.

3.4. Input delay and 1-bit feedback DAC

The two blocks were both realized by switched-capacitor circuits, as shown in Fig. 8. As for the input feedforward delay circuit[9], in the phase of Φ_{1o}, the input signal is sampled onto C_{f0_o}, and, in addition, the delayed input signal (which has been sampled in the previous cycle of Φ_1 and held on C_{f0_e}) will be quantized. Thus, input delay can be realized. The 1-bit DAC whose switches are controlled by the modulator's differential output signals is used to provide negative feedbacks with the

Table 4. Performance comparison.

Paper	Structure	Technology/V_{DD} (V)	BW (kHz)	SNDR (dB)/DR (dB)	Power (mW)	FOM (pJ/conv)
Dessouky, 2001[13]	SC	0.35 μm CMOS/1	25	85/88	0.95	1.307
Keskin, 2002[14]	SC	0.35 μm CMOS/1	50	70.4/74	5.6	20.723
Lee, 2003[15]	SC MASH	0.35 μm CMOS/1.8	500	85.7/87	150	9.544
Yang, 2003[16]	SC Multibit	0.35 μm CMOS/5	20	105/114	55	9.454
Ahn, 2005[17]	SC Switched RC	0.35 μm CMOS/0.6	20	81/82	1	2.731
Chae, 2009[18]	SC Class-C	0.35 μm CMOS/1.2	8	63/76	0.0056	0.303
This work	SC	0.35 μm CMOS/3.3	100	92.8/101	8.6	1.206

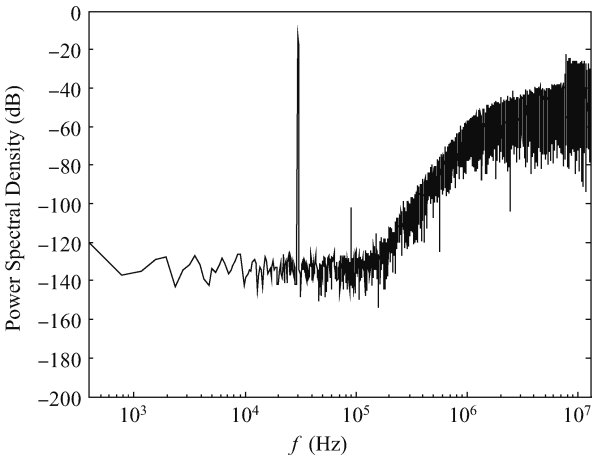

Fig. 12. Output power spectrum with 65k samples of the modulator.

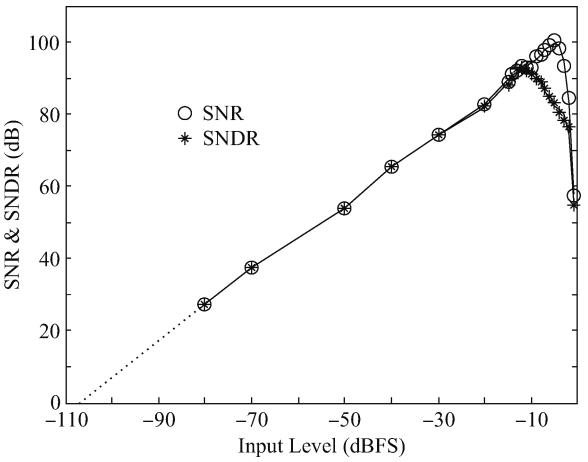

Fig. 13. SNR and SNDR versus input amplitude of the modulator.

value of V_{ref+} or V_{ref-}.

3.5. Other building blocks

The 1-bit quantizer was implemented by a traditional dynamic comparator followed by a latch[5]. All switches are realized by transmission gates and driven by a pair of invert clock signals. In addition, large switches have to be used in the large signal input positions and the 1st integrator to suppress switch non-ideality.

4. Experiment results

The proposed modulator was implemented in a 0.35 μm 2P4M CMOS technology and the die photo of the fabricated chip is displayed in Fig. 11. The test bench was set up using an Agilent 93000 SOC test system and the output waves present the correct function. The output of the modulator was sent to MATLAB for calculating performance parameters which were summarized in Table 3. Figure 12, where modulator's output voltage was normalized to the modulator's reference voltage, shows the modulator's output power spectrum of a 30.08 kHz, which was used to include the most significant 3rd harmonic distortion in the bandwidth, sinusoidal input signal with -8 dB to full scale magnitude, and Figure 13 is the plot of SNR and SNDR versus relative input amplitude (dBFS) using 30.08 kHz input signal. We can see that harmonic distortions appear when the input amplitude becomes higher. The figure-of-merit of sigma–delta modulator is defined as[18]:

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2 \cdot \mathrm{BW} \cdot 2^{(\mathrm{SNDR}-1.76)/6.02}}. \quad (13)$$

Table 4 shows performance comparison of several efficient designs based on a 0.35 μm CMOS process and this work presents superior performance among them.

5. Conclusion and future work

Using distributed feedback and distributed feedforward along with internal feedforward path, a unity-STF structure can be obtained without the complicated adder before quantizer. Then, by means of an additional delayed input feedforward branch, the modulator's timing constraints are further relaxed. A 4th-order 1-bit sigma–delta modulator is implemented based on the above idea. Compared to the other sigma–delta modulators with the same technology level, our design presents a good FOM, thus both power and performance are well optimized.

The future work is to perform a further study on how to reduce the harmonic distortions that appear when a large amplitude signal is added.

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