A low power CMOS 3.3 Gbps continuous-time adaptive equalizer for serial link*

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Abstract: This paper describes using a high-speed continuous-time analog adaptive equalizer as the front-end of a receiver for a high-speed serial interface, which is compliant with many serial communication specifications such as USB2.0, PCI-E2.0 and Rapid IO. The low and high frequency loops are merged to decrease the effect of delay between the two paths, in addition, the infinite input impedance facilitates the cascade stages in order to improve the high frequency boosting gain. The implemented circuit architecture could facilitate the wide frequency range from 1 to 3.3 Gbps with different length FR4-PCB traces, which brings as much as 25 dB loss. The replica control circuits are injected to provide a convenient way to regulate common-mode voltage for full differential operation. In addition, AC coupling is adopted to suppress the common input from the forward stage. A prototype chip was fabricated in 0.18-μm 1P6M mixed-signal CMOS technology. The actual area is 0.6×0.57 mm^2 and the analog equalizer operates up to 3.3 Gbps over FR4-PCB trace with 25 dB loss. The overall power dissipation is approximately 23.4 mW.

Key words: continuous-time equalizer; common-mode voltage; replica control circuits; FR4-PCB
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1. Introduction

As transmission speed increases, the channel loss at high frequency is becoming more and more severe. This will cause ISI (inter symbol interference) and restrict the transmission rate[1]. There have been many reported methods to overcome the limitation. The most popular method is to induct pre-emphasis in the output of the transmitter[2−4]. Another method is utilizing an equalizer in the receiver to compensate channel loss. Receiver equalization can be categorized into two methods: discrete-time equalization and continuous-time equalization. In the digital domain, equalization relies on the recovered clock, which is not the case for the CDR (clock data recovery) in the receiver. In Ref. [5], an open loop equalizer filter is proposed and the unstable low frequency gain produced is due to the increased bandwidth. Moreover, some scholars reported negative resistor feed back[6] and g_m-matched diode-connected transistor[7] to fix the gain, however, these approaches could not provide a good performance as they are mismatch to the high frequency boosting path. In addition, the pre-emphasis and equalization are combined to equalize the channel loss[8]. A robust equalization could fulfill different communication specifications adaptively over a wide frequency scale. A continuous-time adaptive cable equalizer using an enhanced low-frequency gain control method is proposed[10] to compensate the loss of channel at 3.5 Gbps, but it consumes a great deal of power for the specified transfer data rate.

Based on above reasons, a continuous-time adaptive analog equalizer can be selected as our target, which is often used in CDR for high-speed serial interfaces. The high frequency control loop and low frequency control loop are merged to compensate the flat loss and frequency-dependent loss, respectively.

This paper presents the limitation of the low-pass channel with flat loss and frequency-dependent loss, and illustrates the circuit implementation

2. Limitation of low-pass channel characteristic

A simple schematic of serialization and de-serialization for serial link is illustrated in Fig. 1. The transmitter converts the parallel data into serial data with the synchronized clock generated from PLL. Then the pre-emphasis driver of the transmitter is inserted to equalize the channel's loss. The receiver recovers the clock from received data and then retimes the date synchronized by the recovered clock. However, the essential issue is that the eye diagram of the received signal is closed to some extent, which may lead to inaccurate processing of the receiver and therefore, increases the BER (bit error ratio) of the overall system. Therefore, an equalizer is necessary for the receiver of lined transfer system to a reach specified BER.

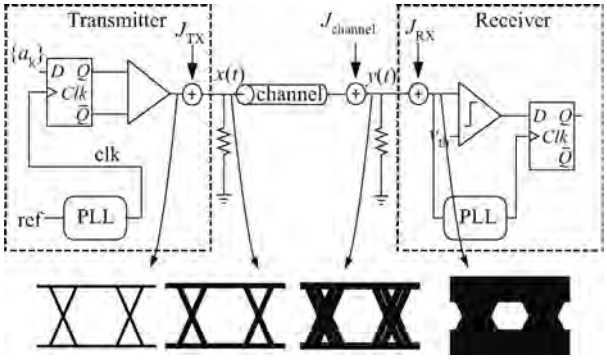

Fig. 1. Schematic of Serdes architecture.

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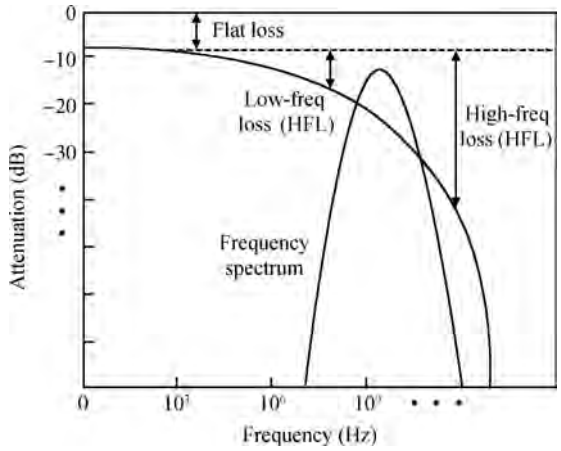

Fig. 2. Attenuation characteristic of the low-pass channel.

Figure 2 shows the attenuation characteristic of a low-pass channel[10−12]. When a signal with a well-defined quality transfers in the channel, the flat loss keeps constant for all of the signal frequency. This results from the system attenuation from the transmitter to the receiver, which is unrelated to frequency. However, the channel will give rise to different loss for different signal frequency gradients. Compared with low-frequency gradients, high-frequency gradients suffer from great loss, which is due to the low-pass characteristic of the channel. If G_{TX} represents the transmitter gain of signal, G_{CH} refers to gain of the channel and G_{RX} is the gain of the analog equalizer in the receiver front-end, the transfer function can be presented as:

$$H(s) = 20 \lg G_{\mathrm{TX}}(s) G_{\mathrm{CH}}(s) G_{\mathrm{RX}}(s). \tag{1}$$

More often, the pre-emphasis is included in the output driver of transmitter, which will advance the high frequency gradients to some extent, but the compensation will either under- or over-estimate the actual channel's characteristic, so it can be seen as a blind equalization in the transmitter-end. A more straightforward and efficient way to remedy the loss is by embedding an equalizer filter in the front-end of the receiver. Compared with the attenuation characteristic of the low-pass channel, the actual channel will present more complex performance. So, an adaptive equalizer is indispensable with respect to different transfer data rates or channels.

In order to compensate the losses, which contain flat loss and frequency dependent loss, we should design a circuit whose response should have some gain to compensate flat loss. In addition, the high-frequency should have large gain to expiate the frequency dependent of the channel, in simple terms, it is a high-pass filter.

Figure 3 shows the block diagram of a conventional equalizer. The received signal from the channel goes through two separate paths: the gain path and high-frequency boosting path. The output signal is the addition of the two paths. Although it can implement the basic function of the equalizer, it has some deficits in the realized application. Firstly, the factor α and β are often manually adjusted in order to adapt the different signal or different channel. This will result in the overestimate or underestimate of the channel loss. Secondly, the bandwidth of the HP (high pass) filter is fixed, so it will lead to a limitation of

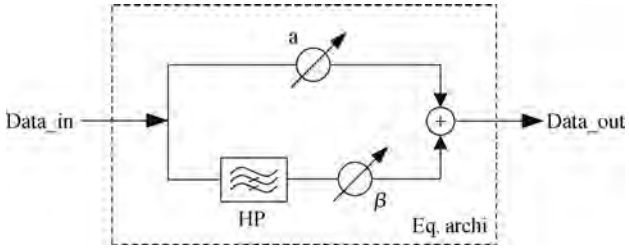

Fig. 3. Block diagram of a conventional equalizer.

signal speed. We should implement an equalizer that can cover a wide frequency for different communication specifications.

3. Circuit design

The implemented analog equalizer topology was adopted in the serial link receiver. As is shown in Fig. 4, a comparator compares the amplitude of signal between its input and output, the low-pass and high-pass filters extract the edge information from the input and output of the comparator, then the rectifier converts the edge change into energy. The energy differences are amplified by an error amplifier and capacitors are added to filter the voltage ripple. As a result, the two voltage signals are applied to regulate the low and high frequency gain of the equalizer cell.

3.1. Adaptive equalizer filter topology

The topology operates as a conventional high-pass filter with capacitor and resistor as source negative-feedback type structure, as is shown in Fig. 5.

The overall transfer function is as follows:

$$H(s) = \frac{-g_{\mathrm{m1,2}} R_{\mathrm{L}} (1 + sR_0C)}{1 + \dfrac{1}{2} g_{\mathrm{m1}} R_0 + sR_0C}. \tag{2}$$

So the pole is $f_{\mathrm{p}} = \frac{1}{2\pi R_0 C}$ and the zero is $f_{\mathrm{z}} = (1 + \frac{1}{2} g_{\mathrm{m1,2}} R_0) \frac{1}{2\pi R_0 C}$.

It is obvious that the zero frequency is larger than pole frequency, so it will perform as a high-pass filter. From the formula above, we can obtain that the low frequency gain can be adjusted by capacitors embedded in the point P1 and P2. The MOS varactor is introduced to provide alterable capacitance controlled by voltage bctrl, as shown in Fig. 6. Another controllable component is transistor M3, which can be regarded as a resistor dominated by voltage gctrl. So, low frequency gain can be regulated by adjusting the voltage gctrl applied to transistor M3 while High frequency boosting can be enhanced by rectifying the voltage bctrl. In order to temper the varactor and to control the MOS transistor-type resistor to a large degree, a rail-to-rail voltage gctrl and bctrl must be generated for full-swing operation. This issue will be highlighted in the implementation of error amplifiers.

3.2. Comparator topology

Figure 7(a) shows a diagram of the comparators, which are realized by cascading three comparator units. The cascading stages could obtain much gain and bandwidth in order to

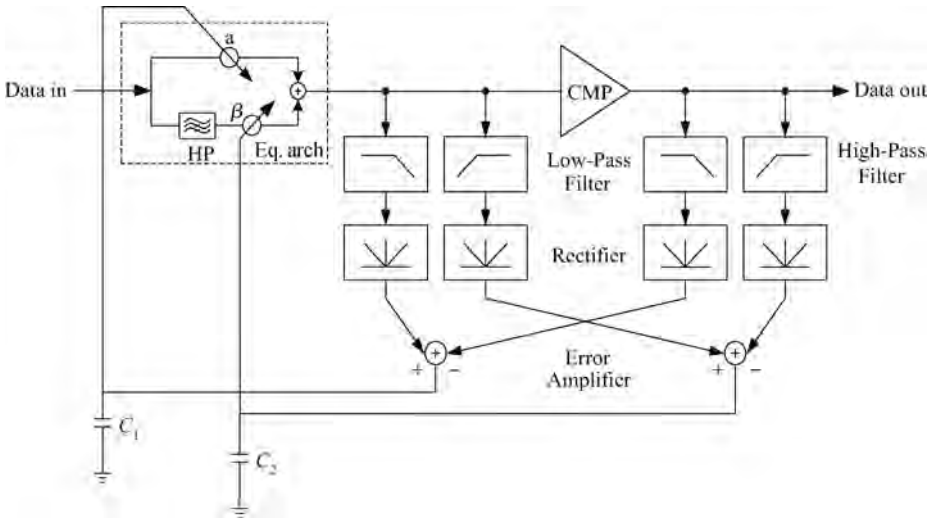

Fig. 4. Overall architecture.

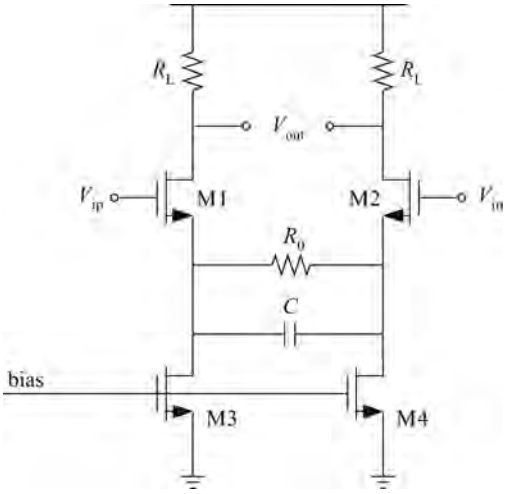

Fig. 5. Conventional equalizer.

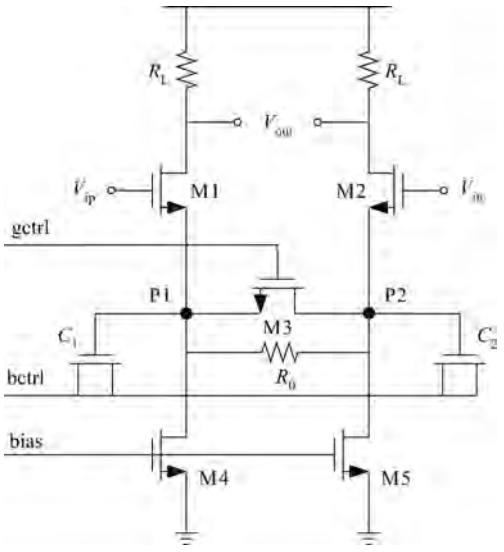

Fig. 6. Topology of the implemented analog equalizer.

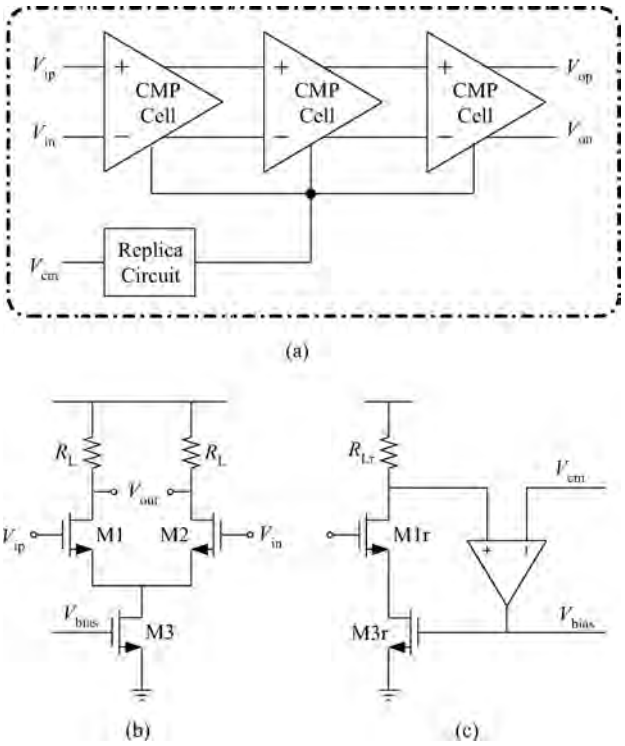

Fig. 7. Topology of comparator. (a) Cascaded comparators. (b) Comparator cell. (c) Replica circuit.

transfer signal with gigaherz spectrum, which operates as CML (current mode logic) buffer. Meanwhile, since the dimension of transistors M1r, M3r and resistors R_{Lr} in the replica cell are the same as that in comparator cell M1, M3, R_L, the output common-mode voltage is determined by the replica circuit.

3.3. Low-pass filter and high-pass filter

The same ac coupling principle is adopted in the design of low-pass and high-pass filters because different common-mode voltages will be applied to the filters. Figure 8(a) shows the topology of the high-pass filter and Figure 8(b) shows the

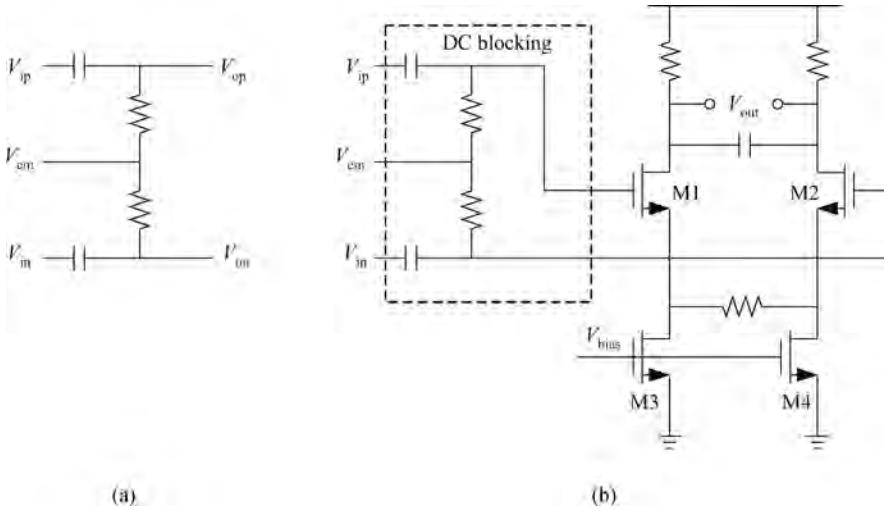

Fig. 8. (a) High-pass filter. (b) Active low-pass filter.

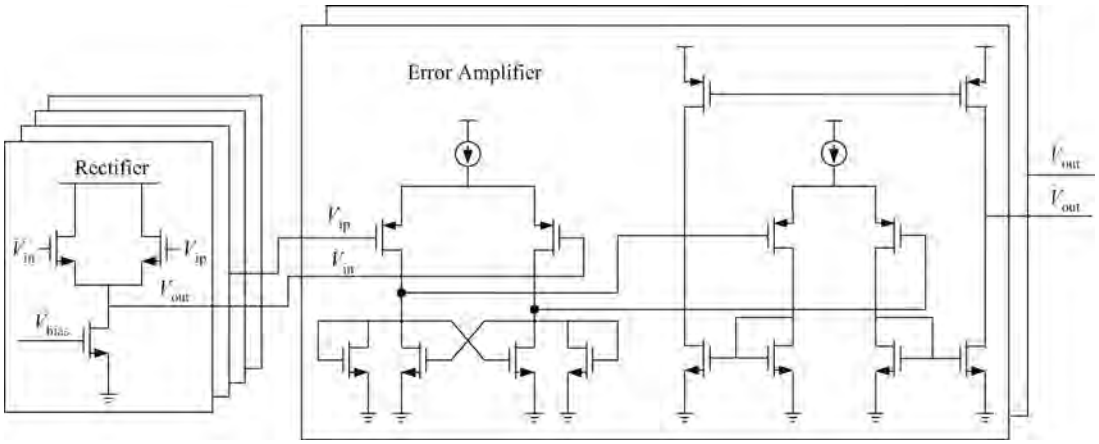

Fig. 9. Topologies of the rectifier and the error amplifier.

low-pass filter. The critical point that degrades the performance is distortion in the low-pass filter, so an active low-pass topology is developed: the differential pair with source degradation resistor and load capacitor. The bias voltages are generated through the replica circuit presented above. In addition, because a conventional active low-pass filter has no dc blocking to eliminate the influence of common-mode voltage, an efficient DC blocking cell is embedded to give an predefined common-mode voltage in port V_{cm}.

3.4. Rectifier and error amplifier

Figure 9 shows the rectifier and error amplifier. The rectifier circuit plays an important role in converting a negative waveform into a positive one, which will facilitate the access of the error amplifier. In order to ensure that the control voltage has rail-to-rail voltage swings, two stages are adopted to amplify the difference of energy from the low-pass and high-pass filters.

3.5. Simulation results

Simulation results of the channel characteristic, which include magnitude and phase information corresponding to frequency, are shown in Fig. 10. The attenuation of channel is 31 dB at 1.65 GHz. Figure 11(a) presents the attenuation effect of the channel with a data rate 3.3 Gbps, which is shown in terms of a closed eye diagram. When the attenuated signal passes through the adaptive equalizer, the simulated eye is open with an eye height of 800 mV and a peak-to-peak jitter of 46 ps, as shown in Fig. 11(b).

Table 1. Measurement summary.

Parameter	Value
Data rate	1–3.3 Gbps
Supply voltage	1.8 V
Current consumption	13 mA (at 3.3 Gbps)
Chip area	0.6×0.57 mm^2 (including pads)
Technology	0.18 μm CMOS

4. Measurement setup and results

Figure 12 shows a photomicrograph of the prototype chip of the continuous-time adaptive equalizer. The output driver buffer is contained to detect the signal's eye diagram after equalization. The chip was fabricated in 0.18-μm six-metal mix signal CMOS process. The actual area of the chip is $0.6 \times$

Table 2. Comparison of the implemented architecture.

Item	Supply	Process (μm)	Data rate (Gbps)	Area (mm^2)	Jitter (ps)	Power (mW)
JSSC[13]	1.8	0.18	3.125	0.72	86	144
JSSC[10]	1.8	0.18	3.5	0.35	120	80
This work	1.8	0.18	3.5	0.342	69.46	23.4

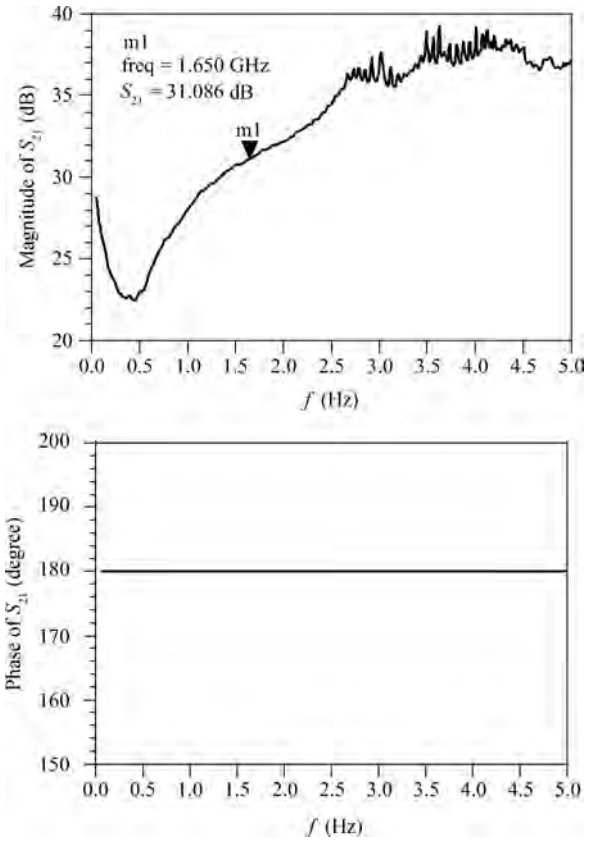

Fig. 10. Simulation results of channel characteristic.

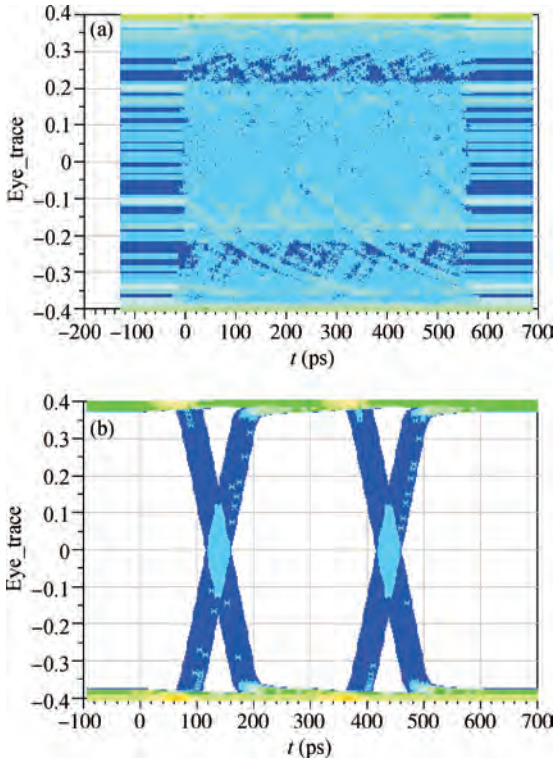

Fig. 11. Simulation result of overall topology (a) before equalizer and (b) after equalizer.

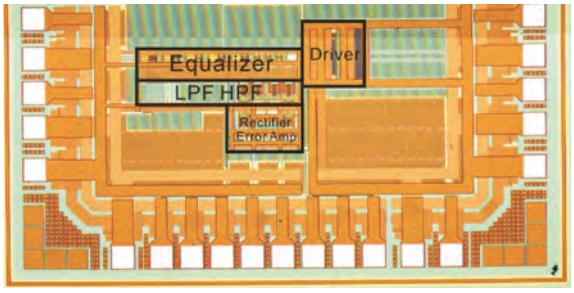

Fig. 12. Photomicrograph of prototype chip.

0.57 mm^2 and the power dissipation is 23.4 mW with a 1.8 V supply voltage.

4.1. Channel measurement

In order to emulate the different loss of channel, PCB traces with different lengths are designed for the channel model. An Agilent N5071C vector network analyzer is used to measure the channel's S parameters for different PCB traces, as shown in Fig. 13.

An Agilent 81134A pulse generator sends ($2^{31}-1$) PRBS (pseudorandom bit sequence) to the chip as the input data through the actual PCB traces, the outputs of the chip connect to an Agilent DSA 91304A digital signal analyzer with bandwidth 13 GHz and sample rate 40 G/s. The pulse generator creates ($2^{31}-1$) PRBS with frequency ranging from 1 to 3.3 Gbps. Figures 14–18 show the eye diagram of the output of channel 2 with different transfer data rates. Table 1 gives measurement result overview of the overall adaptive equalizer and Table 2 is the comparison of implemented architectures from the published literatures, which shows that the implemented topology in this paper illustrates optimized performance in data transmission with date rate 3.3 Gbps.

5. Conclusions

A low power 3.3 Gbps CMOS analog equalizer for serial link was implemented based on conventional architecture. The equalizer topology can merge low-frequency and high-frequency paths together, eliminating the effect of a parasitic capacitor. The merged paths can collaborate with each other to adjust the low-frequency gain and high-boosting level. The implemented chip can operate up to 3.3 Gbps through different PCB traces with different losses at data rates ranging from 1 to 3.3 Gbps.

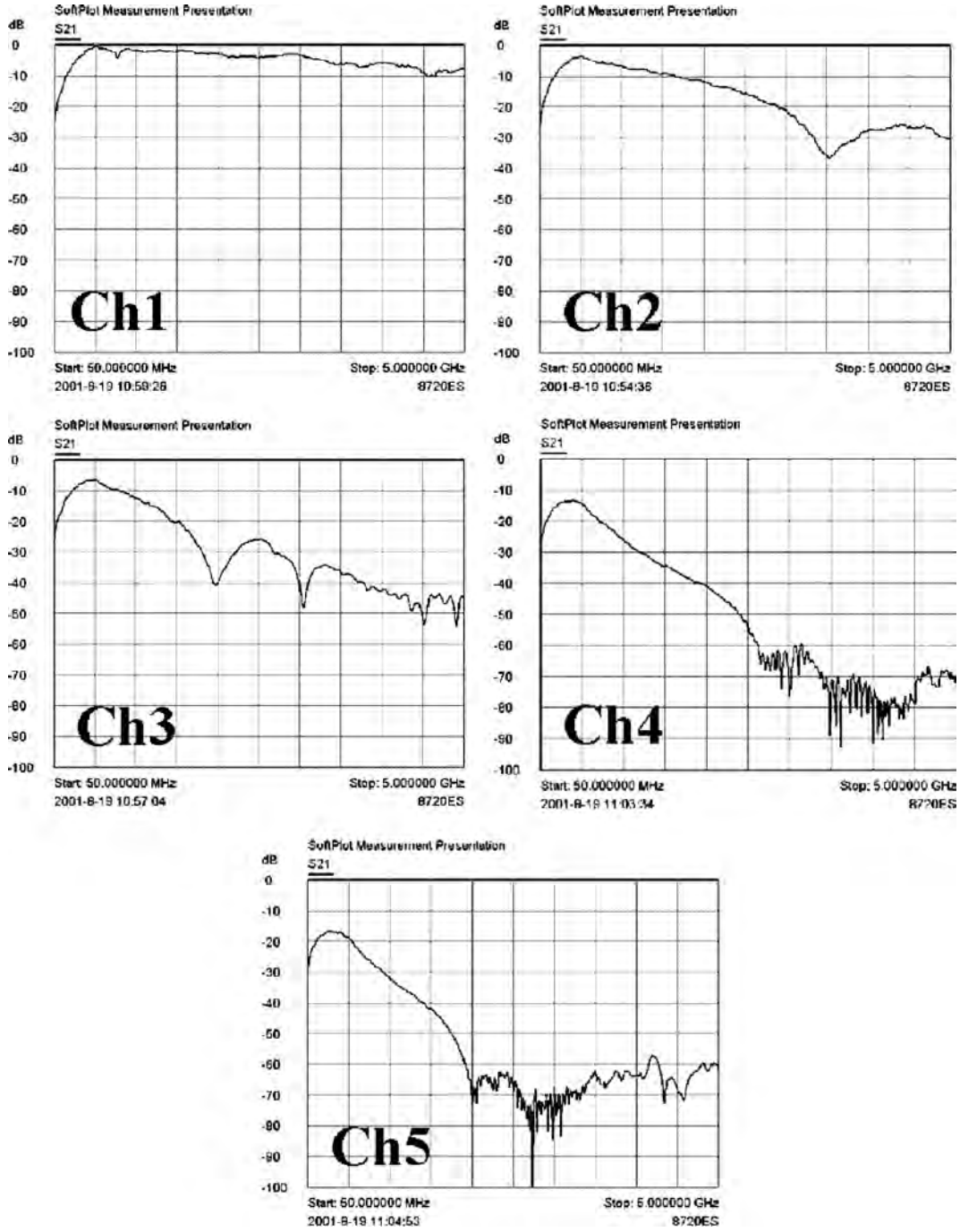

Fig. 13. Measurement of the *S* parameter of channel loss.

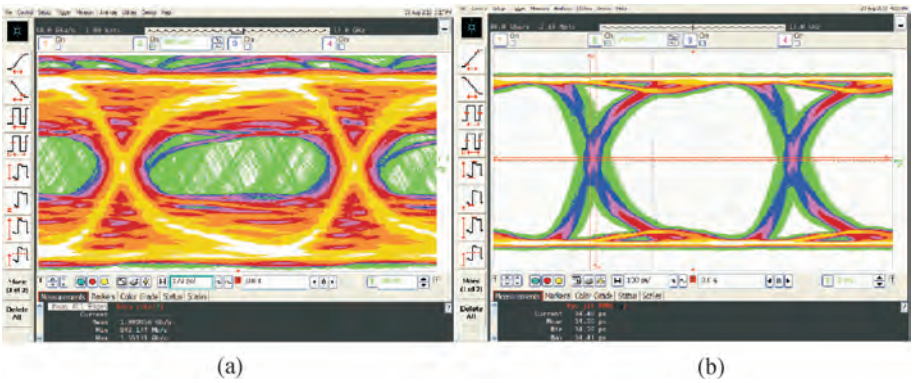

Fig. 14. Equalizer results for a 1 Gbps data rate. (a) Before equalization. (b) After equalization.

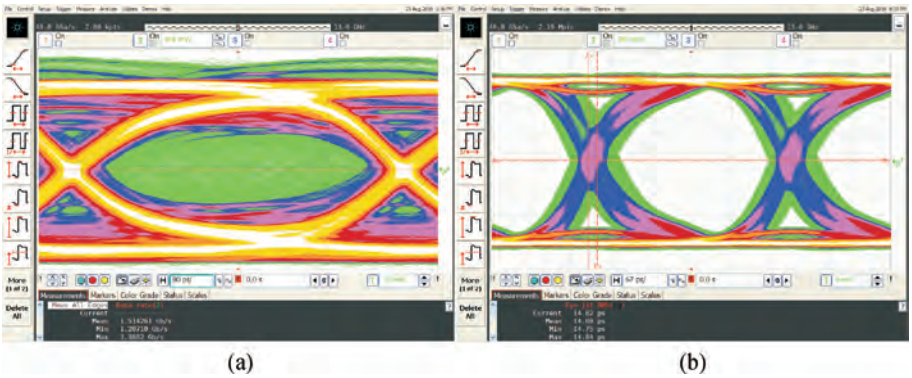

Fig. 15. Equalizer results for a 1.5 Gbps data rate. (a) Before equalization. (b) After equalization.

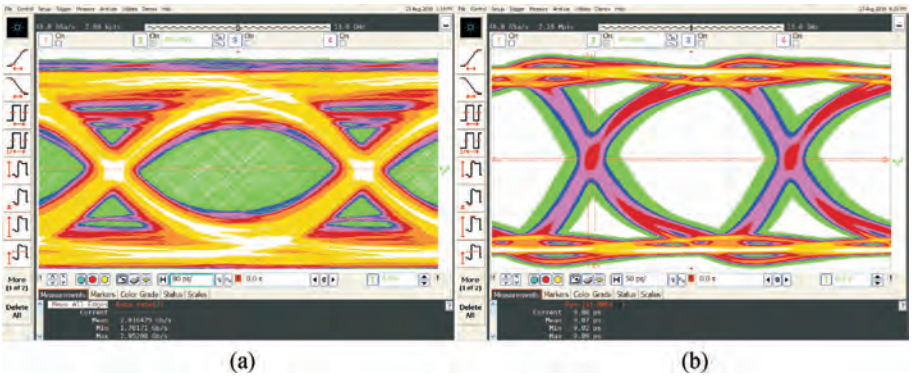

Fig. 16. Equalizer results for a 2 Gbps data rate. (a) Before equalization. (b) After equalization.

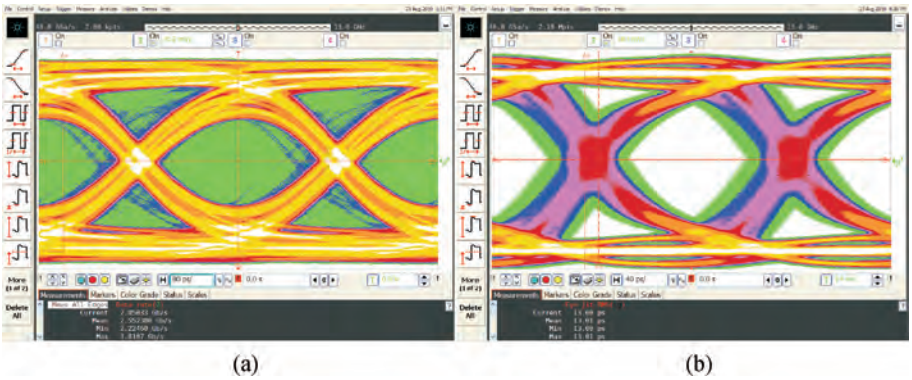

Fig. 17. Equalizer results for a 2.5 Gbps data rate. (a) Before equalization. (b) After equalization.

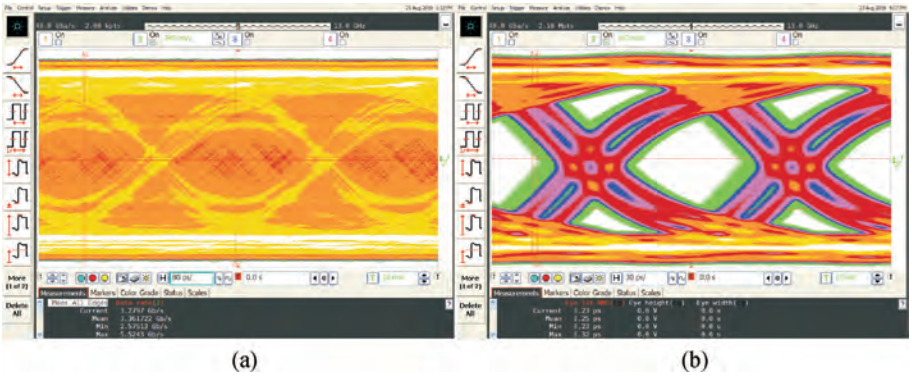

Fig. 18. Equalizer results for a 3.3 Gbps data rate. (a) Before equalization. (b) After equalization.

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References

[1] Liu C Y, Caroselli J. Comparison of signaling and equalization schemes in high speed SerDes. 2007

[2] Fiedler A, Mactaggart R, Welch J, et al. A 1.0625 Gb/s transceiver with 2x-oversampling and transmit signal pre-emphasis. IEEE Int Solid-State Circuits Conf Dig Tech Papers, 1997: 238

[3] Farjad-Rad R, Yang C K, Horowitz M, et al. A 0.4-μm CMOS 10 Gb/s 4-PAM pre-emphasis serial transmitter. IEEE J Solid-State Circuits, 1999, 34: 580

[4] Farjad-Rad R, Ng H T, Lee M J E. 0.622–8.0 Gbps 150 mW serial IO macrocell with fully flexible preemphasis and equalization. Symposium on VLSI Circuits Digest of Technical Papers, 2003: 63

[5] Kudoh Y, Fukaishi M, Mizuno M. A 0.13-μm CMOS 5 Gb/s 10 meter 18AWG cable transceiver with no-feedback-loop continuous-time post-equalizer. IEEE J Solid-State Circuits, 2003, 38: 741

[6] Babanezhad J N. A 3.3 V analog adaptive line-equalizer for fast Ethernet data connection. IEEE Custom Integrated Circuit Conf, 1998: 343

[7] Harman G P, Martin K W, McLaren A. Continuous-time adaptive-analog coaxial cable equalizer in 0.5 μm CMOS. Proc Symp Circuits and Systems, 1997: 97

[8] Higashi H, Maski S, Kibune M. A 5–6.4 Gb/s 12-channel transceiver with pre-emphasis and equalization. IEEE J Solid-State Circuits, 2005, 40(4): 978

[9] Gondi S, Razavi B. Equalization and clock and data recovery techniques for 10 Gbps CMOS serial-link receivers. IEEE J Solid-State Circuits, 2007, 42(9): 1999

[10] Choi J S, Hwang M S, Jeong D K. A 0.18-μm CMOS 3.5-Gb/s continuous-time adaptive cable equalizer using enhanced low-frequency gain control method. IEEE J Solid-State Circuits, 2004, 39(3): 419

[11] Cao Zhigang, Qian Yasheng. Modern principle of communication. Beijing: Tsinghua University Press, 2008

[12] Razavi B. Design of analog CMOS integrated circuits. Beijing: Tsinghua University Press, 2005

[13] Kao T S C, Musa F A, Carusone A C. A 5-Gbit/s CMOS optical receiver with integrated spatially modulated light detector and equalization. IEEE Trans Circuits Syst I, 2010, 57(11): 2844