$Pb(Zr_{0.52}Ti_{0.48})O_3$ memory capacitor on Si with a polycrystalline silicon/SiO_2 stacked buffer layer*

Cai Daolin(蔡道林)[1,†], Li Ping(李平)[2], Zhai Yahong(翟亚红)[2], Song Zhitang(宋志棠)[1], and Chen Houpeng(陈后鹏)[1]

[1]State Key Laboratory of Functional Materials for Informatics, Laboratory of Nanotechnology, Shanghai Institute of Microsystems and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
[2]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

Abstract: $Pb(Zr_{0.52}Ti_{0.48})O_3$ (PZT) thin films have been deposited on a p-type Si substrate separated by a polycrystalline silicon/SiO_2 stacked buffer layer. The X-ray diffraction peaks of the PZT thin films prepared on the polycrystalline silicon annealed at different temperatures were measured. In addition, the polarization of the Pt/PZT/polycrystalline silicon capacitor has been investigated. The memory capacitor of the metal/ferroelectric/polycrystalline silicon/SiO_2/semiconductor structure annealed at 650 ℃ exhibits a clockwise capacitance–voltage hysteresis loop due to the ferroelectric polarization of the PZT thin film. The memory window increases with increasing the area coupling ratio between the SiO_2 capacitor and the PZT capacitor.

Key words: capacitor; thin film; memory
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1. Introduction

Ferroelectric thin film is a promising material for nonvolatile memory applications[1,2]. In particular, the ferroelectric field effect transistor (FFET), as a nonvolatile memory, is promising for the future because FFETs have a single device structure, low power consumption, nonvolatile data storage and nondestructive readout operation characteristics[3−6]. FFETs can pave the way for the high-density integration of nonvolatile ferroelectric random access memory (FRAM). However, it is difficult to prepare ferroelectric thin films with good characteristics directly on silicon substrate because of the interface reactions between the ferroelectric thin film and the silicon substrate[7]. A ferroelectric FET with a metal/ferroelectric/insulator/silicon (MFIS) structure is proposed in order to avoid interface reactions[8−10]. When a metal is additionally inserted between the ferroelectric layer and the insulator layer, a metal/ferroelectric/metal/insulator/silicon (MFMIS) structure can be obtained[11−13].

In our previous work, an FFET structure using a polycrystalline silicon (poly-Si)/SiO_2 stacked layer as a buffer layer has been proposed and the current–voltage characteristics of the FFET with this metal/PZT/poly-Si/SiO_2/Si (MFPIS) structure have been reported[14]. Electrical properties of MFPIS capacitors such as the memory window need to be better understood. So MFPIS structure memory capacitors have been fabricated. In this paper, the crystalline phases of the $Pb(Zr_{0.52}Ti_{0.48})O_3$ (PZT) thin films on polycrystalline silicon annealed at different temperatures are identified. The memory window of the MFPIS capacitors is investigated by the capacitance–voltage (C–V) method. The memory window as a function of the area coupling ratio between the SiO_2 capacitor and the PZT capacitor is discussed.

2. Experiment

To fabricate the MFPIS capacitors, a p-type Si wafer with (100) orientation was used as the starting substrate. A SiO_2 layer was thermally grown on Si substrate. A poly-Si layer was fabricated by the liquid phase chemical vapor deposition method. Then the phosphorus ions were implanted to dope the poly-Si. PZT thin films were deposited by radio frequency magnetron sputtering at room temperature. The PZT target was $Pb_{1.1}(Zr_{0.52}Ti_{0.48})O_3$. The excess of Pb was to compensate for volatile PbO. The PZT thin films were etched by a wet process. The Pt electrode was sputtered and patterned by a lift-off process. Then the PZT thin films were rapidly thermal annealed at 500–650 ℃ for 40 s in an argon and oxygen mixed gas atmosphere in order to obtain a good crystal orientation. The volume ratio of argon and oxygen in the mixed gas atmosphere was 10 : 3. The thicknesses of Pt, PZT, poly-Si, and SiO_2 were 100, 200, 200 and 20 nm, respectively. The aluminum electrode was sputtered. Post metallization annealing was performed at 250 ℃ in an N_2 ambient for 30 min.

The crystalline phase of the PZT thin films was identified by X-ray diffraction (XRD). The C–V characteristics were measured with an Agilent 4284A precision LCR meter.

3. Results and discussion

Figure 1 shows the XRD patterns of the PZT thin films formed by the process described above. The crystallization behavior of the PZT films was sensitively influenced by the an-

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† Corresponding author. Email: caidl@mail.sim.ac.cn
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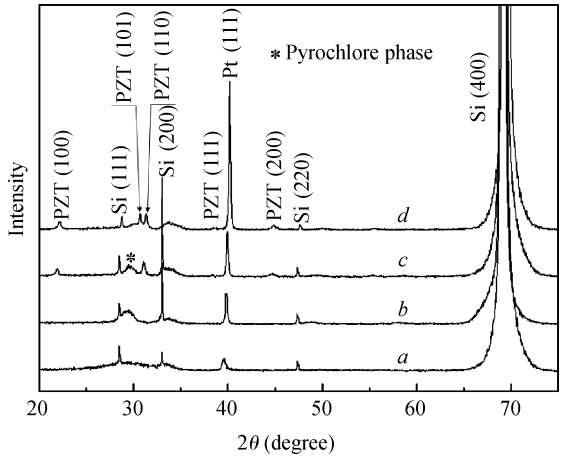

Fig. 1. XRD patterns of the PZT thin films on poly-Si/SiO_2/Si annealed at various temperatures. (*a*) As deposited. (*b*) 500 ℃. (*c*) 600 ℃. (*d*) 650 ℃.

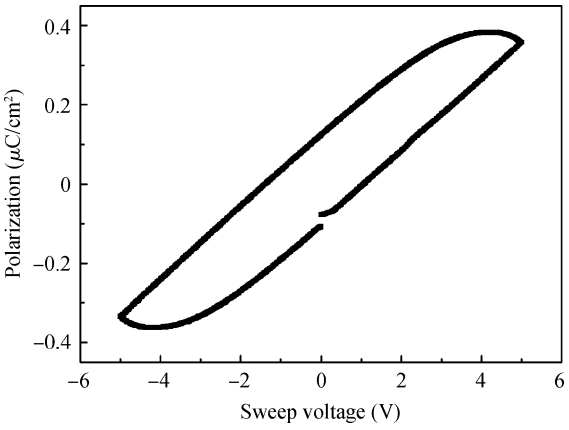

Fig. 2. $P-V$ hysteresis loop of the Pt/PZT/poly-Si capacitor. PZT thin film was annealed at 650 ℃.

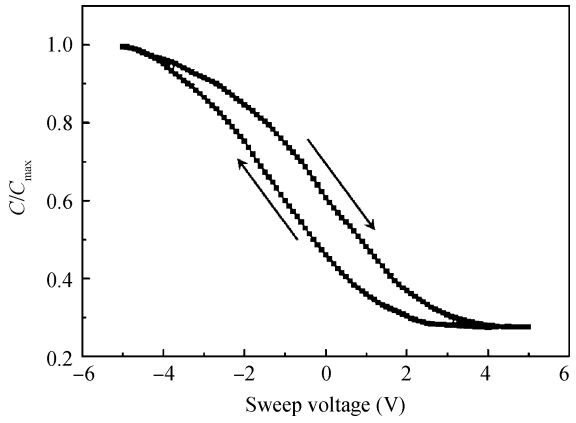

Fig. 3. $C-V$ characteristics of the MFPIS memory capacitor. PZT thin film was annealed at 650 ℃.

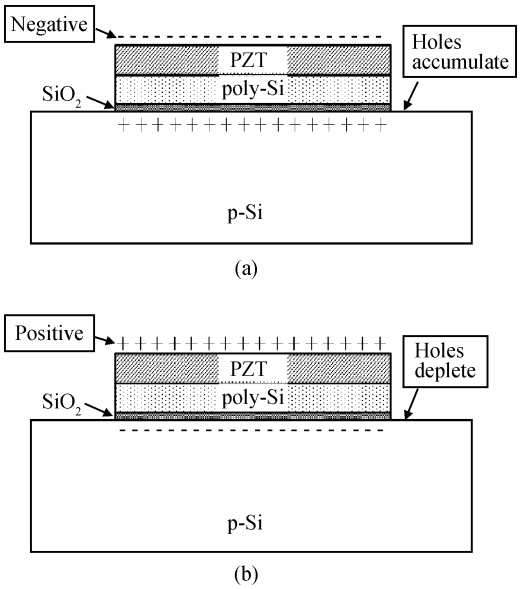

Fig. 4. Schematic diagram of a simplified model for the MFPIS memory capacitor under different bias conditions. Si surface is (a) in accumulation and (b) in inversion.

nealing temperatures. As-deposited PZT film and the PZT film annealed at 500 ℃ exhibit the pyrochlore phase. As the annealing temperature is increased to 600 ℃, the PZT film exhibits (100), (110), (111), (200) diffraction peaks and the pyrochlore phase. With further an increase of annealing temperature to 650 ℃, the pyrochlore phase disappears and a (101) diffraction peak appears. At 650 ℃ annealing temperature, the PZT thin film exhibits (100), (101), (110), (111) and (200) diffraction peaks, but the peak intensity is weak.

Figure 2 shows the polarization–voltage ($P-V$) hysteresis loop of the Pt/PZT/poly-Si capacitor, indicating a non-saturating $P-V$ behavior with a small remnant polarization (~ 0.15 μC/cm^2). This is because that the insufficient crystalline occurs when the PZT thin films are deposited on the poly-Si layer. The small polarization is consistent with the weak peak intensity shown in Fig. 1.

Figure 3 shows the $C-V$ characteristics of the MFPIS memory capacitor. The sweep voltage changed from negative to positive and then back, and the frequency and the voltage of the measuring signal were 1 MHz and 50 mV, respectively. As traced by arrows, the clockwise hysteresis loop is clearly observed, indicating that the memory effect is due to the ferroelectric polarization of the PZT thin film.

When a negative voltage is applied to the top electrode of the MFPIS capacitor, the PZT layer becomes polarized and the holes will accumulate at the silicon surface due to the polarization of the PZT layer, as shown in Fig. 4(a). When the sweep voltage sweeps from negative to positive voltage, an additional positive voltage is needed to convert the silicon surface from accumulation to inversion. Thus, the $C-V$ curve is shifted toward the right.

When a positive voltage is applied to the top electrode of the capacitor, the PZT layer becomes polarized. As shown in Fig. 4(b), the holes will be depleted and an extra number electron will be induced to inversion at the silicon surface. When the sweep voltage sweeps from positive to negative voltage, an additional negative voltage is needed to convert the silicon surface from inversion to accumulation. Thus, the $C-V$ curve is shifted toward the left. Hence, there will be a clockwise $C-V$ hysteresis window. This is due to the polarization effect

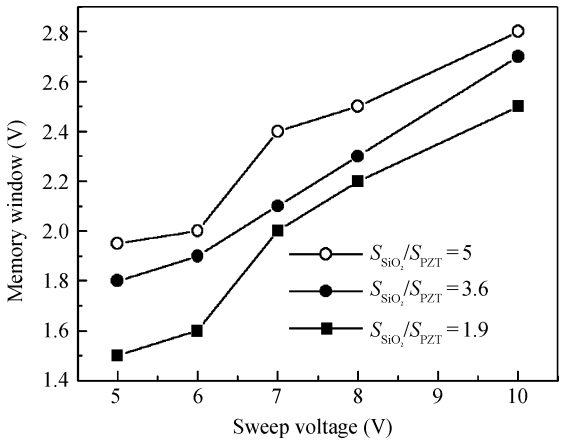

Fig. 5. Memory windows of the MFPIS memory capacitors with different coupling ratios. PZT thin film was annealed at 650 ℃.

of the PZT thin film. The shifted direction is consistent with the counterclockwise current–voltage loops of the MFPIS FFET in our previous work[14].

The memory window is an important memory parameter. The memory window is defined as the voltage shift when the sweep voltage is swept from accumulation to inversion and back[15]. The memory window as a function of the sweep voltage derived from the C–V curves has been measured. Figure 5 shows the memory windows measured from the C–V characteristics of the MFPIS memory capacitors with the sweep voltage range of 5–10 V. The MFPIS memory capacitors exhibit the progressively increasing C–V memory window with increasing the sweep voltage because the ferroelectric polarization increases as the sweep voltage increases. The memory windows with different area coupling ratios between the SiO_2 capacitor and the PZT capacitor are shown in Fig. 5. The memory window increases with increasing the coupling ratio. In order to further explain this, the electrical field on PZT (E_{PZT}) has been calculated by the following equations[2, 14, 16]:

$$E_{PZT} = V_g \Big/ \left(d_{PZT} + \frac{\varepsilon_{PZT} S_{PZT}}{\varepsilon_{SiO_2} S_{SiO_2}} d_{SiO_2} \right), \qquad (1)$$

where d_{PZT} and d_{SiO_2} are the thicknesses of PZT and SiO_2 respectively. S_{PZT} and S_{SiO_2} are the areas of PZT and SiO_2 corresponding to the areas of the ferroelectric capacitor and the metal–oxide–semiconductor capacitor, respectively. It is noted that E_{PZT} increases with increasing the coupling ratio. So the memory window increases with increasing the coupling ratio. In our case, $d_{PZT} = 200$ nm, and $d_{SiO_2} = 20$ nm, even $S_{SiO_2}/S_{PZT} = 1.9$. Considering the dielectric constants of PZT ($\varepsilon_{PZT} = 500$)[2] and SiO_2 ($\varepsilon_{SiO_2} = 3.9$)[17], we get E_{PZT} as 32.3 kV/cm at 5 V sweep voltage, which is sufficient for ferroelectric domain switching to occur in PZT[16].

In fact, the polarization of 0.15 μC/cm^2 shown in Fig. 2 is large enough to swing the silicon surface potential from depletion to inversion. This is also consistent with the theoretical prediction[18] which suggests that the remnant polarization, once it exceeds certain minimal value (e.g., of order 0.1 μC/cm^2), has a minor impact on the memory window. The device performance could be improved by further optimizing the thicknesses and areas of PZT and SiO_2.

4. Conclusion

In conclusion, a metal/PZT/poly-Si/SiO_2/Si structure memory capacitor has been fabricated by depositing a PZT ferroelectric layer on a poly-Si/SiO_2 stacked buffer layer by radio frequency magnetron sputtering. A remnant polarization that is enough to swing the silicon surface is obtained from the Pt/PZT/poly-Si capacitor. The clockwise hysteresis loop in the C–V characteristics demonstrates that this MFPIS structure capacitor can realize a memory function due to the ferroelectric polarization of the PZT thin film. This is consistent with the counterclockwise current–voltage loops of the MFPIS FFET. The memory window increases with increasing the area coupling ratios between the capacitor of SiO_2 and PZT.

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