

# Analytical model for the dispersion of sub-threshold current in organic thin-film transistors

Chen Yingping(陈映平)<sup>1</sup>, Shang Liwei(商立伟)<sup>1</sup>, Ji Zhuoyu(姬濯宇)<sup>1</sup>, Wang Hong(王宏)<sup>1,2</sup>, Han Maixing(韩买兴)<sup>1</sup>, Liu Xin(刘欣)<sup>1</sup>, and Liu Ming(刘明)<sup>1,†</sup>

<sup>1</sup>Laboratory of Nano-Fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

<sup>2</sup>Institute of Microelectronics, School of Physical Science and Technology, Lanzhou University, Lanzhou 730000, China

**Abstract:** This paper proposes an equivalent circuit model to analyze the reason for the dispersion of sub-threshold current (also known as zero-current point dispersion) in organic thin-film transistors. Based on the level 61 amorphous silicon thin-film transistor model in star-HSPICE, the results from our equivalent circuit model simulation reveal that zero-current point dispersion can be attributed to two factors: large contact resistance and small gate resistance. Furthermore, it is found that decreasing the contact resistance and increasing the gate resistance can efficiently reduce the dispersion. If the contact resistance can be controlled to 0  $\Omega$ , all the zero-current points can gather together at the base point. A large gate resistance is good for constraining the dispersion of the zero-current points and gate leakage. The variances of the zero-current points are 0.0057 and nearly 0 when the gate resistances are 17 M $\Omega$  and 276 M $\Omega$ , respectively.

**Key words:** OTFT; sub-threshold current; level 61 RPI a-Si TFT model; equivalent circuit model; HSPICE

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## 1. Introduction

Recently, organic thin-film transistors (OTFTs) have attracted much attention due to their potential application in large displays, sensors, electronic bar codes, etc<sup>[1]</sup>. According to the device physics, there is no drain–source current when the source–drain bias is equal to zero in the transistors, which means that, theoretically, all the output characteristic curves of OTFTs should gather together at the origin point. However, a number of reported experiment results have demonstrated that the output characteristic curves under different gate–source voltages ( $V_{GS}$ ) have non-zero intercepts with the horizontal axis<sup>[2–14]</sup>. This phenomenon is called sub-threshold or zero-current point dispersion. Although there have been many reported experiments on the observation of zero-current point dispersion and suggestions for experimental methods to reduce it<sup>[2–14]</sup>, details of the intrinsic reasons behind it is lacking because it is difficult to control device parameters precisely in order to find out what is more dominant in OTFTs. In this work, an equivalent circuit model is proposed for analyzing the reasons for zero-current point dispersion. According to the results, the zero-current points converge to the origin point with the source/drain contact resistance decreasing and the gate resistance increasing.

## 2. Model setup

### 2.1. Level 61 model and parameter extracting procedure

The Level 61 RPI a-Si TFT model in star-HSPICE (level 61 model)<sup>[15]</sup>, which corresponds to the AIM-Spice level-15 model<sup>[16]</sup>, was used because it is usually applied for OTFT

characterization and organic circuit simulation<sup>[17–20]</sup>. The level 61 model is based on the assumption that the drain current  $I_{DS}$  is composed of two contributions, expressed as

$$I_{DS} = I_{leakage} + I_{ab}. \quad (1)$$

$I_{ab}$  is the current due to the accumulation of carriers while  $I_{leakage}$  represents the current due to the intrinsic conductivity of the organic semiconductor and can be calculated using this formula:

$$I_{leakage} = \text{SIMGMA0} \times V_{DS}, \quad (2)$$

where SIMGMA0 is the minimum leakage current parameter.

A parameter extraction process called the integral function method is introduced in Refs. [21–23] where neglecting the  $I_{leakage}$  and the drain current is expressed as

$$I_{DS} \approx I_{ab} = \frac{K/V_{AA}^\gamma}{1 + R(K/V_{AA}^\gamma)(V_{GS} - V_T)^{1+\gamma}} \times \frac{(V_{GS} - V_T)^{1+\gamma} V_{DS}(1 + \lambda V_{DS})}{[1 + (V_{DS}/V_{DSsat})^m]^{1/m}}, \quad (3)$$

where  $K = WC_i\mu_0/L$ ;  $W$  is channel width and  $L$  is channel length;  $C_i$  is gate capacitance;  $\mu_0$  is band mobility;  $V_T$  is threshold voltage;  $R$  is the source/drain contact resistance;  $m$  is sharpness of the knee region and  $\lambda$  is channel length modulation;  $\gamma$  and  $V_{AA}$  are empirical parameters.

Ignoring resistance  $R$ , the current in the linear region (for a small drain voltage) is simplified from Eq. (3) as

$$I_{DSlin} = \frac{K}{V_{AA}^\gamma} (V_{GS} - V_T)^{1+\gamma} V_{DS}. \quad (4)$$

† Corresponding author. Email: liuming@ime.ac.cn

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If the resistance  $R$  is taken into account, Equation (3) changes as

$$I_{DSlin} = \frac{K/V_{AA}^\gamma}{1 + R(K/V_{AA}^\gamma)(V_{GS} - V_T)^{1+\gamma}} (V_{GS} - V_T)^{1+\gamma} V_{DS}. \quad (5)$$

The saturation voltage is defined through the saturation modulation parameter  $\alpha_S$ :

$$V_{DSsat} = \alpha_S (V_{GS} - V_T). \quad (6)$$

The saturation current is approximated as

$$I_{DSsat} = \frac{K}{V_{AA}^\gamma} \alpha_S (V_{GS} - V_T)^{2+\gamma}. \quad (7)$$

For the parameters, extracting a integral function  $H(V_{GS})$  is defined as

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(x) dx}{I_{DS}(V_{GS})}. \quad (8)$$

After performing the integration and dividing by  $I_{DS}$  the following expression is obtained:

$$H(V_{GS}) = \frac{1}{2 + \gamma} (V_{GS} - V_T). \quad (9)$$

Then  $V_T$  is obtained from the intercept and  $\gamma$  from the slope of the linear region of Eq. (9).

Using Eq. (4) the expression  $I_{DS}^{1/(1+\gamma)}$  versus  $V_{GS}$  is obtained, which is  $I_{DSlin}^{1/1+\gamma} = \left(\frac{K}{V_{AA}^\gamma} V_{DS}\right)^{1/1+\gamma} (V_{GS} - V_T)$ . After calculating the slope  $S_1$  of the expression  $I_{DSlin}^{1/1+\gamma}$  versus  $V_{GS}$ , the value of  $V_{AA}$  can be extracted from

$$V_{AA} = \left(\frac{K V_{DS}}{S_1^{1+\gamma}}\right)^{1/\gamma}. \quad (10)$$

Using Eq. (5), the source/drain contact resistance  $R$  can be extracted.

For extracting  $\alpha_S$ , the expression  $I_{DS}^{1/(2+\gamma)}$  versus  $V_{GS} - V_T$  is obtained from Eq. (7) and its slope  $S_S$  is calculated. Then  $\alpha_S$  can be extracted as

$$\alpha_S = \frac{S_S^{2+\gamma} V_{AA}^\gamma}{K}. \quad (11)$$

The next step is extracting  $m$ , which defines the sharpness of the knee region of transition between linear and saturation regions. It is given as follows:

$$m = \lg 2 / \lg \left[ \frac{K}{V_{AA}^\gamma} \frac{\alpha_S (V_{GS} - V_T)^{2+\gamma}}{I_{DSsat} V_{DSsat}} \right]. \quad (12)$$

The last parameter  $\lambda$  can be obtained from Eq. (3) after all the above parameters are extracted.

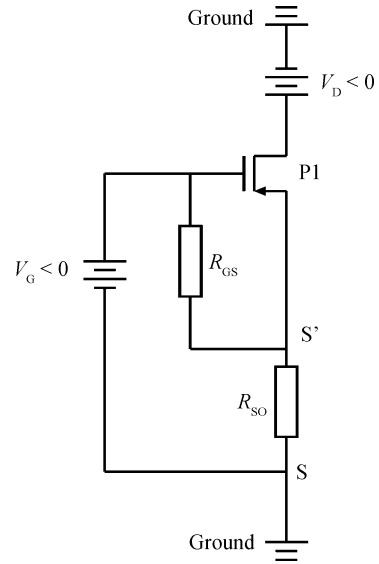


Fig. 1. Equivalent circuit model for simulating the zero-current point dispersion of an OTFT.

## 2.2. Equivalent circuit model

From the model introduced in Section 2.1 it is obvious that there would be no drain current at  $V_{DS} = 0$ . So in order to analyze the sub-threshold currents some modulations are added to the simulation circuit based on a single device. Figure 1 shows a total equivalent circuit model.

The transistor P1 in Fig. 1 is a p-type OTFT modeled by the level 61 model. The resistor  $R_{SO}$  represents the organic source metal contact resistance (also known as source contact resistance) of P1. Considering the highly symmetrical structure of an OTFT, the source contact resistance and the drain contact resistance are thought to be equal<sup>[20]</sup>. Therefore,  $R_{SO}$  equals half of the source/drain contact resistance  $R$  extracted by the integral function method<sup>[21–23]</sup> while setting the source contact resistance included in the level 61 model to be zero. Connecting the source contact resistance  $R_{SO}$  outside the transistor P1 separates the source of P1 and the metal source electrode, which enables the gate resistance to be connected between the gate and the source of the transistor. The drain contact resistance included in the level 61 model is determined to be half of  $R$  as well as  $R_{SO}$ . S in Fig. 1 represents the source electrode of P1 while S' represents the source of P1.

$R_{GS}$  represents the gate resistance. Theoretically,  $R_{GS}$  should be infinite and there should be no gate current. Unfortunately, OTFT gate leakage always exists in experimental tests, which suggests that  $R_{GS}$  is limited. Some gate currents exist flowing from the source to the gate. The current circle consists of the source S', the gate and the source electrode S. So the gate current flows from S to the gate, passing through  $R_{SO}$  and  $R_{GS}$ . Then the voltage of S' ( $V_{S'}$ ) is a minus value because of voltage drop in  $R_{SO}$  when S connects to the ground. It is said that the source and the drain of P1 are reversed when  $V_D$  is not negative enough ( $V_D > V_{S'}$ ). Therefore, there are some currents flowing from the reversed source (the origin drain) to the reversed drain S' (the origin source), which form the positive currents in the sub-threshold region. These positive currents are not eliminated until  $V_D$  is at least as negative as  $V_{S'}$ .

Table 1. Parameters extracted using the integral function method with experimental data.

Parameter	$\alpha_S$	$\gamma$	$\lambda$	$m$	$V_{AA}$	$V_T$	$R$
Value	1.29	0.155	-0.125	0.772	12.37 V	0.597 V	$5.52 \times 10^6 \Omega$

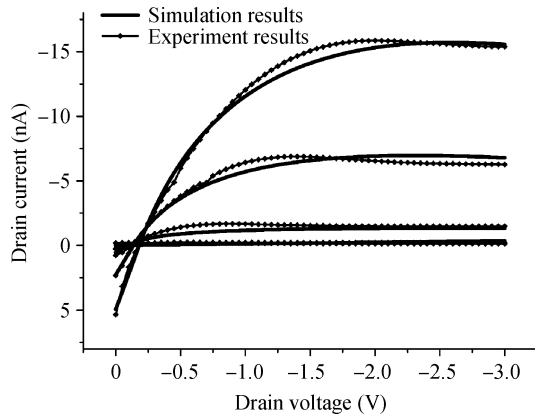


Fig. 2. Experimental data compared with simulation results: output characteristic at  $V_g = -2.0, -1.5, -1.0, -0.5$  and  $0$  V, respectively.

According to the analysis above the currents at the point  $S'$  agree with the Kirchhoff current law:  $I_S = I_G + I_D$ , where  $I_S$  represents the source current flowing from  $S$  to  $S'$ ,  $I_G$  the gate current from  $S'$  to gate and  $I_D$  the drain current from drain to  $S'$ . Applying the Kirchhoff current law at the point  $S'$  when  $V_{DS} = 0$ , we can get the relationship between  $R_{GS}$  and  $R_{SO}$ .

### 3. Simulation results and discussion

#### 3.1. Simulation results

The parameters extracted in this work are based on the device with a single annealed  $ZrO_2$  layer as gate dielectric in Ref. [4]. The device's channel width and channel length are  $W = 500 \mu m$  and  $L = 60 \mu m$ , respectively. The relative dielectric constant of  $ZrO_2$  is 22 and the dielectric layer is 150-nm-thick. According to Ref. [4], the band mobility is  $\mu_0 = 0.02 \text{ cm}^2/(\text{V}\cdot\text{s})$ , but this value was extracted using the expression  $I_D = WC_i\mu_0(V_{GS} - V_T)^2/2L$ . Compared with Eq. (7), there is difference with a coefficient of 1/2 between them. Therefore, the value of  $\mu_0$  should be settled to  $0.04 \text{ cm}^2/(\text{V}\cdot\text{s})$  when extracting the device model parameters. All of the parameters are obtained using the extraction procedure described in Section 2.1. The values of each extracted parameter are listed in Table 1. In this work both  $R_{SO}$  in Fig.1 and the drain contact resistance in level 61 model are determined by half of the parameter  $R$ , which has been extracted in Table 1. The source contact resistance in the level 61 model is set to be zero. After calculations with the Kirchhoff current law at point  $S'$  based on the experimental results,  $R_{GS} = 10R_{SO} = 27.6 \text{ M}\Omega$ .

Using the extracted parameters the simulation is completed in a CADENCE environment with the HSPICED simulator. In Fig. 2 the experimental results are compared with the simulation results. They fit well with each other, validating the proposed equivalent circuit model for simulating the general characteristics of OTFTs.

In order to quantify the dispersion of zero-current points, a novel parameter, the variance (VAR) of the zero-current points,

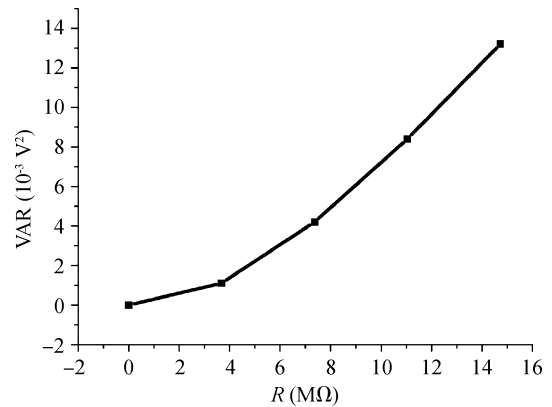


Fig. 3. Curve of VAR against  $R$  calculated from the simulation results.

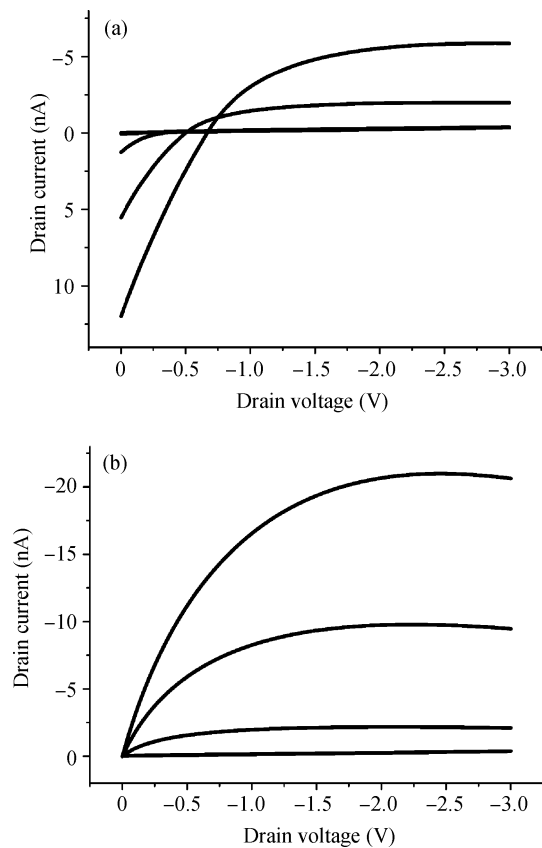


Fig. 4. Simulation output characteristics at various  $R$ . (a)  $R = 14.72 \text{ M}\Omega$ . (b)  $R = 0 \text{ M}\Omega$ .

which describes the degree of their dispersion from each other, is induced. VAR is calculated by

$$\text{VAR} = \sum (V_{0i} - V_E)^2/n, \tag{13}$$

where  $V_{0i}$  is the  $i$ th zero-current point voltage,  $V_E$  is the average value of all the zero-current point voltages, defined as  $V_E = \sum V_{0i}/n$ , and  $n$  is the number of gate biases. According to the experimental data in Ref. [4], VAR is calculated to be

0.0041 V<sup>2</sup> at  $R_{GS} = 27.6 \text{ M}\Omega$  and  $R_{SO} = 2.76 \text{ M}\Omega$ .

### 3.2. Influence of the contact resistance on the zero-current point dispersion

The ideal value of the contact resistance is 0 when there is no zero-current point dispersion. So to discuss the influence of the contact resistance on the zero-current point dispersion, the first value of  $R_{SO} = 0.5R = 0$  is selected. The value of  $R_{SO} = 0.5R = 14.8 \text{ M}\Omega$  is as 5 times that of the experimental contact resistance value shown in Table 1 and it is big enough to observe the trend of the zero-current points' dispersion along with the contact resistance increasing. Five values of the source contact resistance are selected from 0 to 14.8 M $\Omega$  at a linear step 3.7 M $\Omega$  for simulation.  $R_{GS}$  is kept a constant 27.6 M $\Omega$ . Figure 3 shows the curve of VAR against  $R_{SO}$  calculated from the simulation results. It is found that VAR decreases with decreasing  $R_{SO}$ . The zero-current point dispersion changing with  $R_{SO}$  can be seen from Fig. 4 more directly. It shows that zero-current point dispersion can be constrained by decreasing the source/drain contact resistance  $R_{SO}$ . However, the absolute value of the gate leakage increases with  $R_{SO}$  decreasing at the same gate voltage. This is because the total resistance from S to the gate decreases. All of factors suggest that zero-current point dispersion is caused not only by the gate leakage but also the source/drain contact resistance. In fact, the voltage of the source S' is calculated by  $V_{S'} = I_{gate} R_{SO}$ . Although  $I_{gate}$  increases,  $R_{SO}$  decreasing leads smaller  $V_{S'}$ . Therefore, it needed a less negative drain voltage to eliminate the drain and source reverse at a certain gate voltage.

In order to reduce the contact resistance, a modification of the organic-metal interface is used. Modifying the organic-metal interface to reduce the contact resistance improves OTFT performance<sup>[24–27]</sup>. Zero-current point dispersion can be improved obviously by inserting a transition metal oxide layer between the Al source/drain electrodes and the active layer (pentacene)<sup>[27]</sup>. This is because the presence of a MoO<sub>3</sub> layer at the organic/Al interface significantly reduces contact resistance by aligning the highest occupied molecular orbital (HOMO) of pentacene with the valence band of MoO<sub>3</sub><sup>[27]</sup>.

### 3.3. Influence of the gate resistance $R_{GS}$ on the zero-current point dispersion

Keeping the contact resistance  $R_{SO} = 0.5R = 2.76 \text{ M}\Omega$  and changing the value of  $R_{GS}$ , the simulation results show the influence of  $R_{GS}$  on the zero-current point dispersion. A large value of  $R_{GS} = 276 \text{ M}\Omega$ , 10 times that of the experimental gate resistance value shown in Table 1, was selected.  $R_{GS} = 276 \text{ M}\Omega$  is almost an ideal situation where the gate resistance is infinity. Another gate resistance as small as  $R_{GS} = 17 \text{ M}\Omega$  is selected to observe the zero-current point dispersion case at a small gate resistance. Five values of  $R_{GS}$  are chosen between  $R_{GS} = 17 \text{ M}\Omega$  and  $276 \text{ M}\Omega$  with the latter one being 2 times that of the former one, between every two neighbor values. Figure 5 shows the curve of VAR against  $R_{GS}$  according to the simulation results. From Fig. 5, it is found that with  $R_{GS}$  increasing VAR decreases. This can be seen more directly from Fig. 6. With increasing  $R_{GS}$  the gate leakage decreases at the same gate voltage. According to the level 61 model, the drain-source current is dependent only on the gate voltage

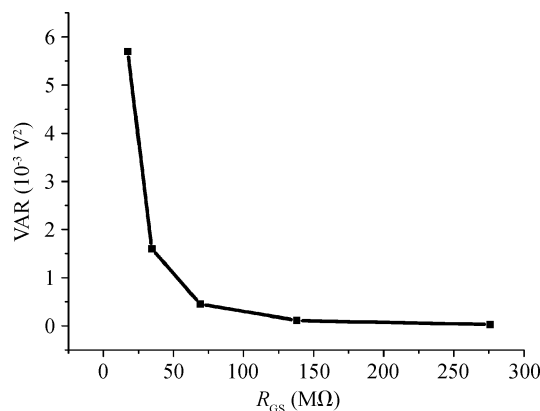


Fig. 5. Curve of VAR against  $R_{GS}$  calculated from the simulation results.

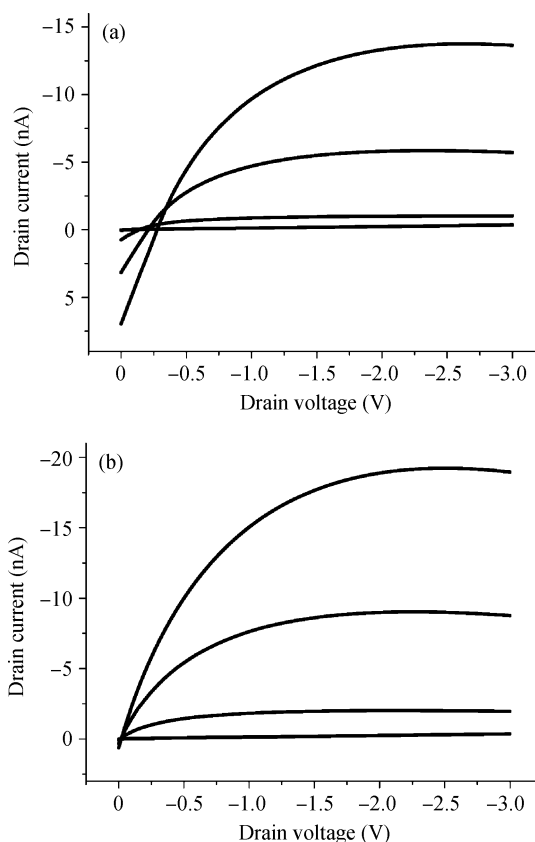


Fig. 6. Simulation output characteristics at various  $R_{GS}$ . (a)  $R_{GS} = 17.25 \text{ M}\Omega$ . (b)  $R_{GS} = 276 \text{ M}\Omega$ .

and the drain-source voltage, and independent of the gate resistance. Therefore, the drain-source current is constant when  $R_{GS}$  changes at the same gate voltage and drain-source voltage, which means that the total current flowing through  $R_{SO}$  decreases when the gate leakage decreases. So the voltage drop between S and S' decreases according to the Ohm law. This suggests that the drain voltage  $V_D$  needed to eliminate the reverse source is less negative, causing the zero-current points to gather together closer to the origin.

Physically, the gate resistance  $R_{GS}$  comprises the insulator bulk resistance and the series resistance in the insulator-active layer interface. Its value relates to the insulator resistive, the

overlap area between the insulator and the active layer, and the interface situation. In order to improve the carrier injection from the insulator-active layer interface it is used to modulate the interface and reduce the series resistance.

Therefore, in order to increase  $R_{GS}$  the general methods include applying a high resistive material as an insulator layer and increasing the insulator thickness. In Ref. [4] the zero-current points of a device with a double layer PMMA/ZrO<sub>2</sub> as the insulator are much better than that of a device with an annealed ZrO<sub>2</sub> as the insulator<sup>[4]</sup>. Similar results are also reported in Refs. [13, 14]. The thickness of the polymer also influences the zero-current points. According to Fig. 3 in Ref. [14], the zero-current point dispersion becomes better and better with the PMMA thickness changing from 15 to 250 nm.

Another method used to constrain the zero-current point dispersion by increasing  $R_{GS}$  is patterning the device's channel<sup>[5]</sup>. In Ref. [5] Song *et al.* applied a non-destructive, high-throughput and high-resolution lithographic patterning method to fabricate poly(3-hexylthiophene) (P3HT)-based OTFTs. Compared with OTFTs whose channels are not patterned, the zero-current point dispersion is improved largely.

#### 4. Conclusion

An equivalent circuit model based on the level-61 model in HSPICE has been applied to simulate the zero-current point dispersion successfully. Through the model we found that zero-current point dispersion is greatly influenced by both source/drain contact resistance and gate resistance. Increasing the gate resistance and decreasing the source/drain contact resistance causes the zero-current points to converge at the origin. The validation of the proposed model is verified by experimental results.

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