An ultra high-speed 8-bit timing interleave folding & interpolating analog-to-digital converter with digital foreground calibration technology

Zhang Zhengping(张正平)[1,†], Wang Yonglu(王永禄)[2], Huang Xingfa(黄兴发)[2], Shen Xiaofeng(沈晓峰)[2], Zhu Can(朱璨)[2], Zhang Lei(张磊)[1], Yu Jinshan(余金山)[2], and Zhang Ruitao(张瑞涛)[2]

[1]No.24 Research Institute, China Electronics Technology Group Corporation, Chongqing 400060, China
[2]Science and Technology on Analog Integrated Circuit Laboratory, Chongqing 400060, China

Abstract: A 2-Gsample/s 8-b analog-to-digital converter in 0.35 μm BiCMOS process technology is presented. The ADC uses the unique folding and interpolating algorithm and dual-channel timing interleave multiplexing technology to achieve a sampling rate of 2 GSPS. Digital calibration technology is used for the offset and gain corrections of the S/H circuit, the offset correction of preamplifier, and the gain and clock phase corrections between channels. As a result of testing, the ADC achieves 7.32 ENOB at an analog input of 484 MHz and 7.1 ENOB at Nyquist input after the chip is self-corrected.

Key words: ultra high-speed; interpolation algorithm; folding; analog-to-digital converter
DOI: 10.1088/1674-4926/32/9/095010 **EEACC:** 2570

1. Introduction

With the rapid expansion of broadband digital communication over the past two decades, analog-to-digital converters (ADCs), as one of the most important building blocks for the analog front-end, have attracted much attention. Ultra high-speed and wide-band ADCs apply to receiver fields, such as satellite, radar/ECM, digital oscilloscopes and direct RF down conversion, and communication systems[1]. The most straightforward technique to convert an analog signal into an 8-b digital output code is used in the so-called full parallel or flash ADC. Although full flash type architecture is known to be the most popular, the hardware complexity is proportional to 2^n (n is the resolution bits)[2, 3]. The two-step structure reduces the number of comparators drastically. A coarse decision is converted back into an analog value using a digital-to-analog converter (DAC) and is subtracted from the originally applied input signal. The residual signal is then converted into digital levels using a flash ADC. The extra block DAC is hard to design for the intended sampling frequencies. A pipeline structure adopts closed-loop amplifiers to achieve high resolution, but closed-loop amplifiers limit the conversion speed of the ADC. In order to overcome the drawbacks of the flash ADC a two-step ADC and pipeline ADC, a folding and an interpolation ADC (F&I ADC) is proposed. The F&I ADC has the advantage of a small number of comparators and a small chip area, while the operating speed is almost the same as that of the flash type. Another advantage is that the F&I ADC does not have residual amplifiers and adopts an open-loop structure, so the ADC's conversion speed is higher than that of a two-step ADC and a pipeline ADC. However, folding architecture is very susceptible to device mismatch even in bipolar technologies, but the mismatch can be mitigated by digital foreground calibration. The calibration technique has been proved to be efficient for pipeline ADC, F&I ADC in performance improvement[4, 5].

This paper presents an ultra high-speed wide bandwidth F&I ADC. It has 8-bit resolution and the sampling rate is 2 GSPS. The ADC utilizes time-interleaving technology and 2 single-channel ADCs with a sampling rate of 1 GSPS are combined into the ADC with a sampling rate of 2 GSPS. The ADC utilizes digital calibration to achieve high performance.

2. F&I ADC architecture

The system block diagram of the proposed ultra high-speed F&I ADC is presented in Fig. 1. It consists mainly of INPUT MUX, S/H circuit, clock circuit, reference circuit, A-to-D conversion circuit and calibration logic. System inputting sampling clock clk is 2 GHz, and channel I's sampling clock and channel Q's sampling clock are $\div$ 2 fractional frequency of system clock clk. The system sampling timing diagram is shown in Fig. 2. Input sinusoidal signals are sampled by 1 GHz clki and clkq, and the sampled nodes 1, 3 and 5 and the sampled nodes 2 and 4, respectively, will be obtained. Putting all the sampled nodes together at the output terminal is equivalent to sampling sinusoidal signals of 2 GHz clk[6]. To achieve good performance at 2 GSPS, the ADC utilizes digital calibration logic to mitigate gain error, mismatch error and clock phase error between channels I and Q.

2.1. Architecture of one channel

A block diagram of one channel F&I ADC is shown in Fig. 3. After being processed by input MUX, the analog input signals enter a high-performance sample/hold unit, and the holding signals of the S/H output are compared with the voltage across reference tap and are pre-amplified. The pre-amplified signals are preprocessed analogously and 12 effective signals are obtained. Meanwhile, the 3-times folding of the amplified signals are done for the first time, then 4-times interpolation

† Corresponding author. Email: lovezzpan@126.com
Received 15 March 2011, revised manuscript received 19 April 2011

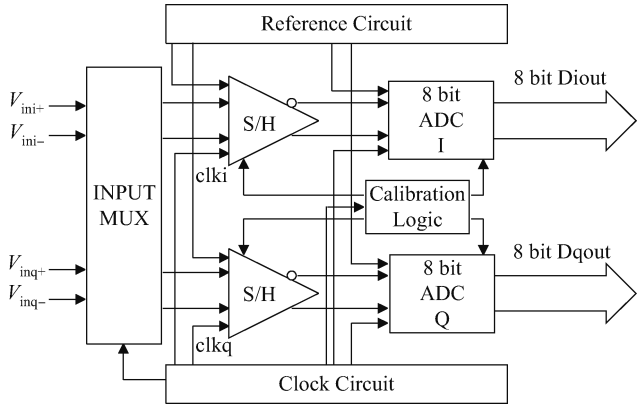

Fig. 1. Architecture of the ADC.

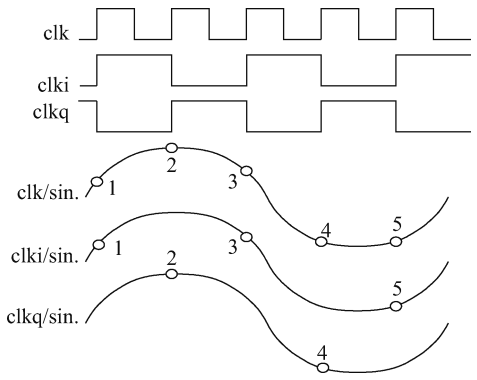

Fig. 2. System sampling timing diagram.

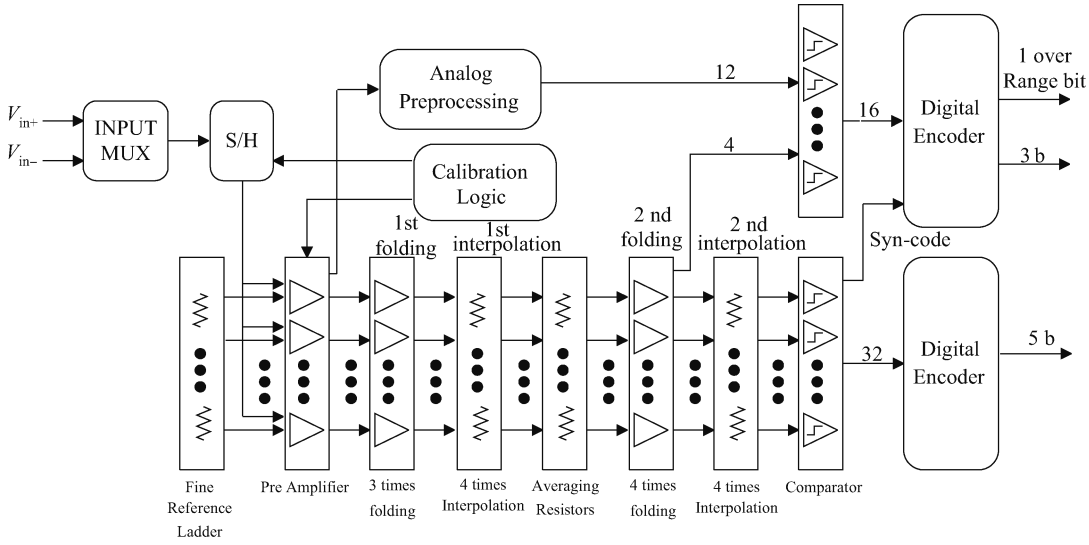

Fig. 3. Architecture of one channel ADC.

is made, and the resistances of interpolated signals are averaged. The second 4-times folding of the averaged signals is conducted and 4 effective signals selected the from folding signals and 12 signals pre-processed comprise MSB signals, which enter a comparator for comparison and 8 effective signals are obtained. Again, a 4-times interpolation of the second folding signals is made, the signals enter comparator, 32 comparison signals and 1 synchronous signal are obtained, finally 32 signals are encoded and low 5-bit digital codes are obtained. In a coarse quantizer, 16 coarse quantization signals and 1 synchronous signal are encoded, and high 3-bit codes and 1 out range bit code are obtained.

2.2. S/H circuit

Sample/hold circuit implements the function of conversion of analog signals into spread signals, and is one of the key units in an A/D converter. Its dynamic performance determines the dynamic performance of ADC for the whole system. As the sampling rate of the circuit in this study is as high as 1 GSPS, the S/H circuit uses open-loop architecture. As shown in Fig. 4, the S/H circuit consists of the S/H stage (SHa) and the amplification and driving stage (SHb). The SHa pair is a pseudo-differential circuit and is converted into a true differential circuit in the SHb to enhance its anti-interference capability. In order to eliminate the effect produced possibly by the input current, a PMOS transistor instead of a bipolar transistor is used as an input transistor. In an open-loop circuit, errors in both gain and offset are especially prominent and are removed by a D/A control technique. An 8-bit inverse R–$2R$ network D/A control circuit is added to the base of output transistors Q17 and Q18, whose schematic is shown in Fig. 5. The architecture of the D/A circuit is unique and is different from that of a conventional D/A circuit, thus saving layout area greatly.

The digital code D1, as a maximum weighted code, controls S1. If D1 is "1", then the right switch will be on; but if D1 is "0", then the left switch will be on. Similarly, D2 controls S2, D3 controls S3, …, D8 controls S8. The current controlling R_5, I_{out}, can be expressed as

$$I_{\text{out}} = \left(\frac{\text{D1}}{2} + \frac{\text{D2}}{4} + \ldots + \frac{\text{D8}}{256}\right) I_{\text{ref}}. \tag{1}$$

The offset voltage adjustable to S/H circuit is $R_5 I_{\text{out}}$ ($R_7 = R_5$), and accuracy in adjustment is 1/8 LSB of output amplitude for S/H circuit.

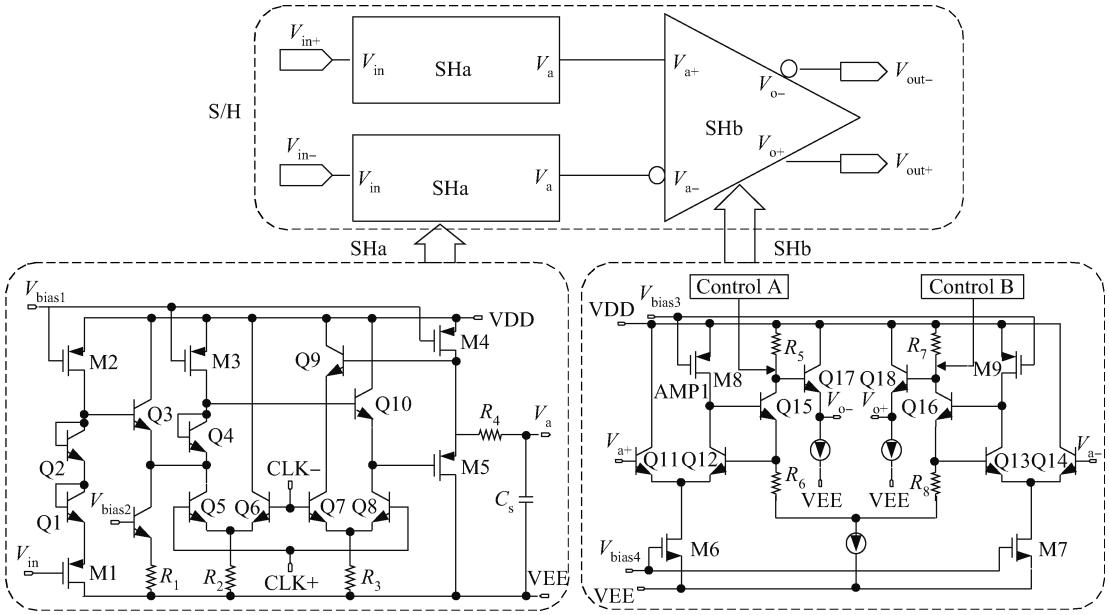

Fig. 4. S/H circuit.

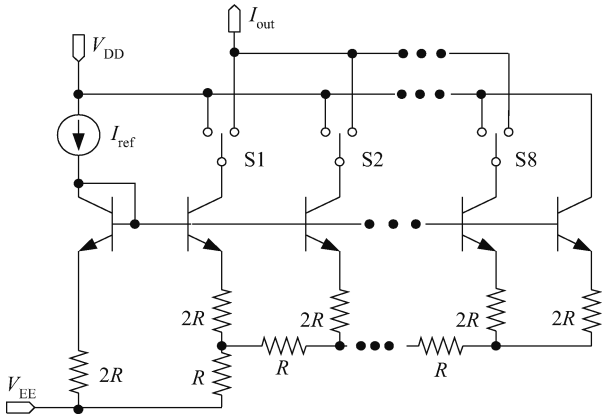

Fig. 5. 8-bit inverse R–$2R$ D/A control circuit.

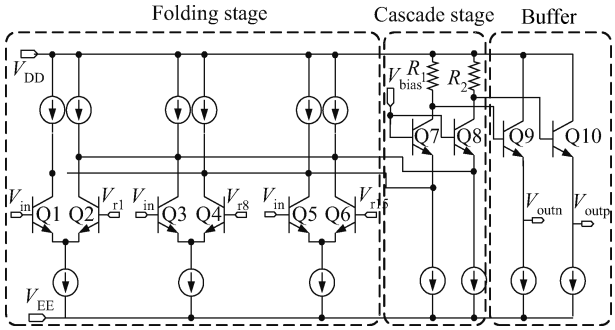

Fig. 6. Folding by 3 circuits.

If the voltage gain of SHa is a_1, if the gain of the amplifier unit consisting of Q11, Q12, M6 and M8 is a_2, if the ratio of adjustable resistors R_5 to R_6 (i.e. R_5/R_6) is a_3, and if the gain of output transistors Q17 and Q18 is a_4, then the gain of the S/H circuit can be expressed as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = a_1 a_2 a_3 a_4 = M. \tag{2}$$

The S/H circuit is designed to achieve an input-to-output voltage gain of 2. Due to mismatch of transistors, current source, etc., there tends to be an error in gain, and there would be a resulting error when the S/H circuit is compared with the reference voltage. Therefore, the current flowing through the reference resistor string in Fig. 2 is adjusted in order to equate the amplitude of maximum reference voltage to the amplitude of output difference for S/H circuit. The 8-bit R–$2R$ network D/A control circuit is used to adjust the current, with the adjustable resolution of 1/8 LSB. The theory of this approach is the same as that of offset elimination technology.

2.3. Folding and interpolating circuit

The output signal amplified by preamplifiers is folded by 3 reference voltages using 3 differential pairs, as shown in Fig. 6. The frequency of the folding signal is equal to the product of input frequency and folding degree, which is 3 in this case, thus it is required that bandwidth of folder should be 4 GHz.

Although adding the cascade stage following the folding stage consumes extra power, the power is actually negligible since it is shared between three amplifier differential pairs. The cascade stage circuit brings two advantages: one is to amplify the folding signals, and the other is to reduce load capacitance at the folding nodes. Thus, the following Eq. (3) can be obtained.

$$f_{3\text{dB}} = \frac{1}{2\pi R(FC_{\text{folding-amp}} + C_{\text{load}})}, \tag{3}$$

where F $(=3)$ is folding factor. Lowering C_{load} can increase the bandwidth of the folder. The buffer circuit is added after the cascade stage. This not only obtains low output source impedance at the output nodes, but also increases the capability of driving the folder or comparator in the following stage.

Interpolation allows the generation of intermediate voltages, so that the voltages will not need to be compared to

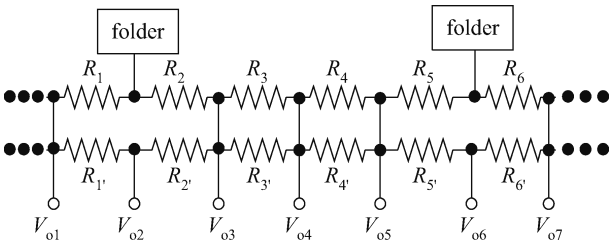

Fig. 7. Interpolation by 4 and averaging circuit.

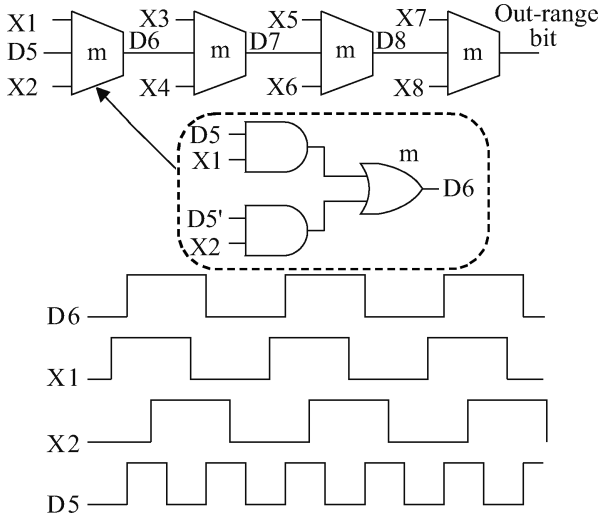

Fig. 8. High 3-bit encoding logic.

255 distinct reference voltages at the front-end of a flash-like converter. Each input to reference voltage comparison at the front-end would require its own amplifier, consuming an unacceptable amount of power and area. The two interpolation stages (the preceding and following interpolation stages) use 4-times interpolation, as shown in Fig. 7. As the subsequent circuit of the final pre-amplifier pair implements calibration, the technology of device matching must be taken into special consideration. After a 4-times interpolation of folding signals is made, the interpolation signals are averaged by resistors R'_1, $R'_2, \ldots R'_6 \ldots$ in order to make zero-crossings shift towards their ideal positions, thus improving INL and DNL.

Considering noise and bandwidth, the equivalent resistor string of the resistor string should satisfy the equation below:

$$V_{\text{noise}} = \sqrt{4kTR_{\text{eq}}\text{Bandwidth}} < \frac{1}{3}\times\frac{1}{2}\,\text{LSB} = \frac{1}{3}\times\frac{V_{\text{FS}}}{2\times 2^{\text{ENOB}}}. \tag{4}$$

A signal bandwidth of 1.5 GHz and signal amplitude of 500 mV are needed, and the maximum equivalent resistance of corresponding resistor string is 4.4 kΩ.

2.4. Encoding LOGIC

The folding algorithm in the circuit is unique. The high 3 bits are not a coding form of temperature code, but are a progressive reduction coding of low bit code to high bit code (i.e. the 5th bit to the 8th bit). For the convenience of analysis, the input is a ramp signal. The 5th code D5 is used as both a digital output and a connecting and synchronous code between the 5th bit and the high 3 bits[7]. For reasons of differential relation, X1, X2, …, X7 and X8 are 8 in 16 high-bit signals in Fig. 2, the encoding logic of the 6th code D6 is shown in Fig. 8, which can be expressed as Eq. (5). Similarly, the maximum 2 bits D7 and D8 as well as the out range bit can be obtained.

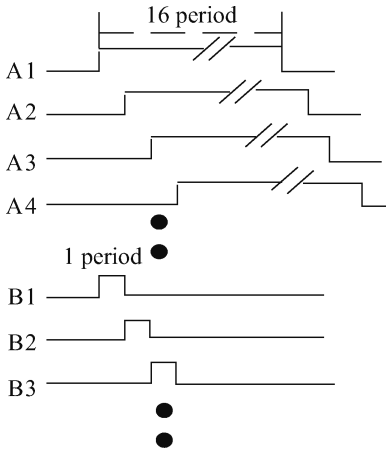

Fig. 9. Low 5-bit encoding logic.

$$\text{D6} = \text{D5}\times\text{X1} + \text{D5}'\times\text{X2}. \tag{5}$$

Figure 9 shows the low 5 bit encoding logic 32 LSB signals are compared and latched, and 16 cyclic signals A1, A2, …, A16 are obtained. The data rate is 62.5 MHz; that is, 1 period is 1 GHz. Through cyclic successive xor operation, B1, B2, …, B16 are obtained, the low 5-bit digital codes are:

$$\text{D1} = \text{B1} + \text{B3} + \cdots + \text{B13} + \text{B15},$$
$$\text{D2} = \text{B1} + \text{B2} + \text{B5} + \text{B6} + \cdots + \text{B15} + \text{B16},$$
$$\text{D3} = \text{B1} + \text{B2} + \text{B3} + \text{B4} + \text{B9} + \text{B10} + \text{B11} + \text{B12},$$
$$\text{D4} = \text{B1} + \text{B2} + \text{B3} + \text{B4} + \text{B5} + \text{B6} + \text{B7} + \text{B8},$$
$$\text{D5} = \text{A1}.$$

2.5. Two channel ADC

If the performance of one channel ADC with 1 GSPS sampling rate is excellent, the results of conversion, in which an equivalent sampling rate of 2 GSPS is achieved by two-channel alternate sampling technology, may be very bad. The reason for this is that there is offset error and clock phase error between channels. The calibration technology of the offset error between channels is similar to that of gain error in a single channel, and also calibration of output for the S/H circuit. During the calibration, the dual-channel ADC uses one sampling clock to sample and convert the analog input, to compare the output of S/H circuit and to enhance voltage to compensate for the S/H circuit with the small output voltage. The principle of compensation is similar to the one of one channel gain compensation, and the same inverse R–$2R$ network D/A control circuit is used as well. The principle of dual-channel gain error calibration is as follows. Controlled by input MUX, the gain error and offset error of one channel itself is first calibrated, and digital calibration codes are latched; offset error between channels are then calibrated, the calibration circuit still uses those in Figs. 4 and 5, and the equal digital calibration codes are simultaneously put at differential terminals of a single channel;

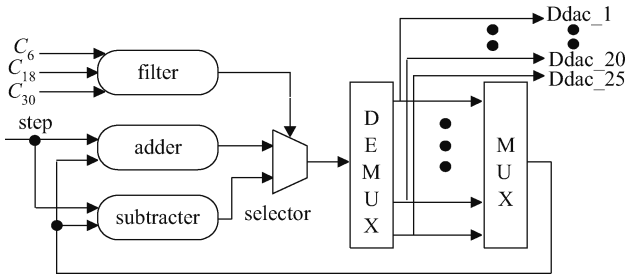

Fig. 10. Functional block diagram of digital correction for preamplifiers.

Table 1. Relation between pre-amplifier with calibration feedback signal.

i	y
2, 5, 8, 11, 14, 17, 20, 23	6
3, 6, 9, 12, 15, 18, 21, 24	18
1, 4, 7, 10, 13, 16, 19, 22, 25	30

finally, the digital calibration codes and latch codes calibrated previously are added, thus the ultimate correction codes are obtained.

Dual-channel ADC alternate sampling realizes an equivalent sampling rate of 2 GSPS, and correctly controls the duty cycle of the sampling clock of 50% using DCS technology. The sampling interval between channels, however, may not be 1/2 of the sampling clock period due to an error. Therefore, a sampling clock calibration circuit is designed. As it is inconvenient for the clock calibration circuit to use self-calibration technology, external manual calibration is made by SPI. The 8-bit D/A converter is used to control the transmission gate current to set the delay, and the sampling clock of channel Q is manually calibrated with channel I fixed until measured performances have been optimized and the digital codes are latched.

2.6. Digital calibration technique

Calibration logic consists of the manual calibration of the sampling clock and the self-calibration of gain error, offset error, the preamplifier's offset error of a single channel and gain error between two channels. The sequence of calibration is as follows. First, gain error and offset error of a single channel S/H circuit are calibrated; then, gain error between two channels is calibrated; finally, offset errors of preamplifiers of all channels are calibrated.

Figure 10 shows functional block diagram of the digital calibration of offset error for preamplifiers and the calibration flow is plotted in Fig. 11. In Fig. 11, V_{cal_i} is the i-th calibration reference voltage ($i = 1, 2, 3, \ldots, 25$), d_{DAC_i} is the i-th DAC control code (starting from 100000), step is the step length for change in d_{DAC_i}, and C_y is the output of the y-th comparator. The correspondence between y and i is listed in Table 1. The calibration period is controlled by a counter.

Every time a round of calibration is made, 1 is added to counter. When the reading of counter is 21, all calibration clocks will be off, the calibration period will be over, and the circuit will enter a normal operational mode. In 20 rounds of calibration, the step (step length for change in d_{DAC_i}) diminishes gradually. In each round of calibration, the analog input is disconnected, a calibration voltage is applied to the input of the S/H circuit, then relevant comparator output C_y is filtered. If output of filter is 1, then the step will be subtracted from d_{DAC_i}; otherwise if the filter output is 0, then the step will be added to d_{DAC_i}. After that, the next reference voltage is applied to the input of the S/H circuit, the next preamplifier is calibrated, the above process is repeated until 25 preamplifiers have been calibrated once each. Finally, the code value of d_{DAC_i} is latched and is added to normal operational circuit[8].

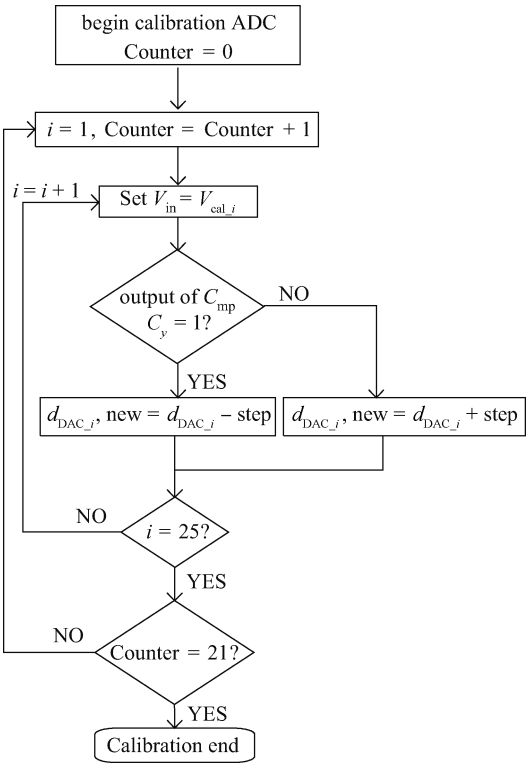

Fig. 11. Calibration flow.

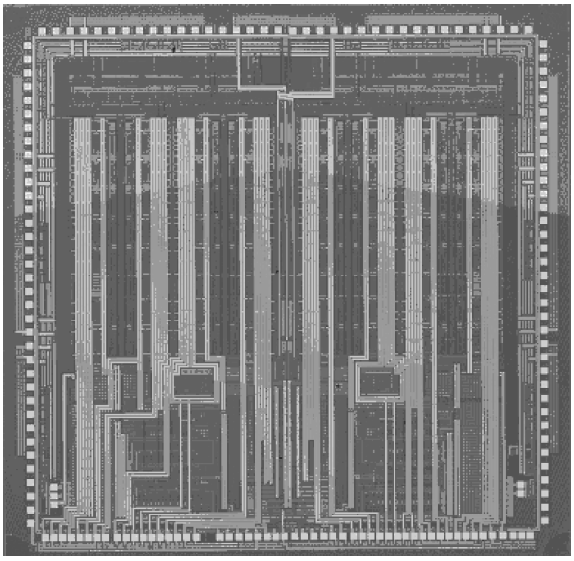

Fig. 12. Microphotograph of the ADC.

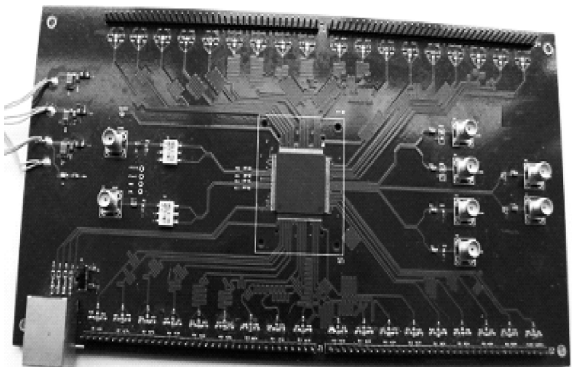

Fig. 13. Evaluation board for the ADC.

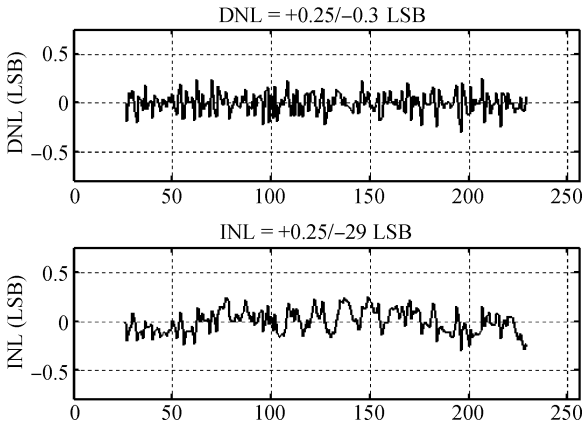

Fig. 14. DNL and INL at $F_{in} = 484$ MHz, $F_s = 2$ GSPS.

Table 2. ADC electrical characteristics.

Parameter	Typical	Max
Analog input parameter		
Analog supply voltage (V)	3.3	
Digital supply voltage (V)	3.3	
Analog output voltage (V)	2.25	
Analog supply current (mA)	275	
Digital supply current (mA)	180	
Analog output current (mA)	70	
Nominal dissipation (W)	1.66	
Standby dissipation (mW)	140	
Analog input voltage (mVpp)	500	
Analog input frequency (MHz)	484	
Sample rate (GSPS)	2	
Static characteristic		
DNL (LSB)	± 0.3	± 0.4
INL (LSB)	± 0.3	± 0.6
Gain error	± 2%	
Dynamic characteristic		
ENOB (bit)	7.3	
SNR (dB)	45.84	
SINAD (dB)	44.57	
THD (dB)	–50.4	
SFDR (dB)	52	
IMD (dB)	–50	

3. Design verification

The 8-bit 2-GSPS ADC is designed in 0.35-μm BiCMOS technology. The die area is 5.25 × 5.168 mm^2, as shown in Fig. 12.

The test board is shown in Fig. 13.

The measured ADC electrical characteristics are shown in Table 2.

The analog input bandwidth is up to 1.5 GHz. At 2 GSPS sampling rate, 7.4 ENOB are achieved for a 50-MHz input with calibration enabled, while 6.0 ENOB with calibration disabled.

In Fig. 14, at 2 GS/s and at a 484-MHz sine wave input, if calibration is enabled, the differential nonlinearity (DNL) < ±0.3 LSB and integral nonlinearity (INL) < ±0.3 LSB; if calibration is disabled, DNL < ±1.8 LSB and INL < ±2.0 LSB.

The converter samples a 484-MHz, 500 mV different sine wave at 2 GS/s. Figure 15 shows the output spectrum of the reconstructed analog signal from ADC output by DAC. The SFDR is 52 dB, the SNR is 45.8 dB, and the ENOB is 7.32 bits. With Nyquist input, the SFDR is 50.8 dB, the SNR is 44.2 dB, and ENOB is 7.1 bits.

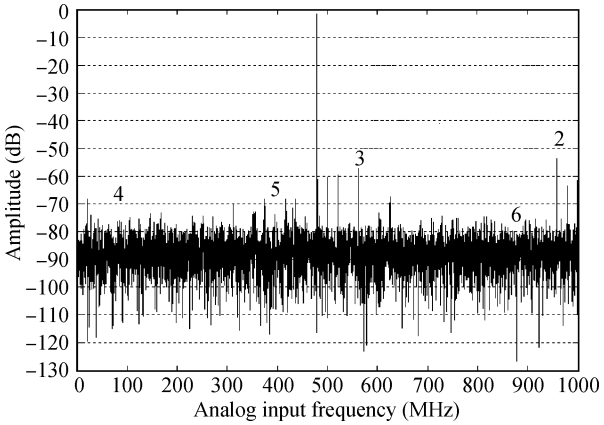

Fig. 15. SFDR at $F_{in} = 484$ MHz, $F_s = 2$ GSPS.

4. Conclusion

We have demonstrated that significant performance enhancement calibration has been brought to F&I ADC. Offset calibration and gain calibration in the system are very effective in enhancing the performance of the converter. The ADC, processed in 0.35-μm BiCMOS, with a 3.3 V supply voltage, can achieve a conversion rate greater than 2 GS/s, 0.3 LSB DNL, 0.3 LSB INL, 7.32 ENOB at 484 MHz input, and 7.1 ENOB at Nyquist. The ADC uses 2X interleaving, with each channel at 1 GSPS.

References

[1] Yu Jinshan, Zhang Ruitao, Zhang Zhengping, et al, A digital calibration technique for an ultra high-speed wide-bandwidth folding and interpolating analog-to-digital converter in 0.18 μm CMOS technology. Journal of Semiconductors, 2011, 32(1): 015006

[2] Flynn M P, Sheahan B. A 400-Msample/s, 6-b CMOS folding and interpolating ADC. IEEE J Solid-State Circuits, 1998, 33(12): 1932

[3] Lee D, Song J, Shin J, et al. Design of a 1.8 V 8-bit 500 MSPS folding-interpolation CMOS A/D converter with a folder averaging technique. 18th European Conference on Circuit Theory

Design, 2007: 356
[4] Ali A M, Morgan A, Dillon C, et al. A 16 b 250 MS/s IF-sampling pipelined A/D converter with background calibration. IEEE International Solid-State Circuit Conference Digest of Technical Papers, 2010: 292
[5] Taft R C, Menkus C A, Tursi M R, et al. A 1.8-V 1.6-Gsamples/s 8-b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency. IEEE J Solid-State Circuits, 2004, 39(12): 2107
[6] Chu M, Jacob P, Kim J W, et al. A 40 Gs/s time interleaved ADC using SiGe BiCMOS technology. IEEE J Solid-State Circuits, 2010, 45(2): 380
[7] Hiremath V, Ren S. An ultra high speed encoder for 5 GSPS flash ADC. Instrumentation and Measurement Technology Conference, 2010: 136
[8] Zhang R T, Yu J S, Zhang Z P, et al. Linearity improvement base on digital foreground calibration algorithm for a ultra high-speed analog-to-digital converter. International Conference on Anti-Counterfeiting, Security and Identification, July 2010: 130