A new low-voltage and high-speed sense amplifier for flash memory

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Abstract: A new low-voltage and high-speed sense amplifier is presented, based on a very simple direct current-mode comparison. It adopts low-voltage reference current extraction and a dynamic output method to realize its performance indicators such as low voltage, low power and high precision. The proposed amplifier can sense a 0.5 μA current gap and work with a lowest voltage of 1 V. In addition, the current power of a single amplifier is optimized by 15%.

Key words: flash memory; sense amplifier; current-mode; low-voltage

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1. Introduction

Flash memories are used as storage devices for a wide variety of equipment. In particular, flash memories are suitable for portable electronic equipment, such as personal digital assistants, MP3 players and palm-top computers. As microelectronic technology develops, portable equipment has an increasing requirement for high speed and low power for flash memory. In addition, the sense amplifier, as an important part of flash memory, will also vary to be adaptive to low voltage and high speed. The power supply voltage has been scaled down to sub-1.5 V. One of the main challenges for the new generation flash memories is to develop a robust and high-speed sense circuit with a supply voltage of sub-1.5 V[1, 2].

There are two kinds of differential sense amplifiers from the perspective of what will be compared here, one of which is based on a voltage-mode amplifier (Fig. 1)[4] whose read operation is performed by directly comparing the input voltage, and then issuing "0" or "1" through the voltage-mode sense amplifier. The two input voltages are obtained by the current–voltage conversion of the current coming from the selected memory cell and from a reference cell. The voltage-mode approach has scaling limitations as the power supply voltage is reduced[5]. The other is based on the current mode approach (Fig. 2),[5, 6] which implements a pure current comparison operation. The selected memory cell current can be obtained by a current mirror and then directly compared with a reference current, which is also be obtained by current mirror. The comparison results lead to a wide swing aptitude on node SO. The aptitude as an input of the inverter is compared with the trip point voltage of the sense amplifier and then "0" or "1" is output. The current-mode sense amplifier is able to operate robustly with a nominal supply voltage higher than 1.5 V. However, as the power supply scales down, the threshold voltage of the memory cell cannot be scaled in the same manner since the cell channel doping is optimized for programming and erasing[4]. Likewise, the threshold voltage of PMOS (used as current mirror) cannot be scaled down. So this scheme cannot work very well with a low power supply under 1.5 V.

Aiming at these problems presented for existing voltage-mode and current-mode sense amplifiers, this paper presents a new high-performance sense amplifier based on current-mode. The amplifier adopts a direct current comparison curtailing current mirror, which reduces device mismatch and magnifies current gap. Meanwhile the amplifier substitutes an inverter for a dynamic amplifier in the output, which raises sense and output speed. Finally, the reference path circuit adopts separation method of drain and gate, which enables it to work with low voltage at 1 V. Based on these changes, the amplifier can work with super-low voltage and has a high read access speed.

2. Conventional current-mode sense amplifier

2.1. Description of a conventional current-mode sense amplifier

A typical sense amplifier based on current-mode is illustrated in Fig. 2 and is used to compare the current coming from the selected memory cell with the current of a reference cell.

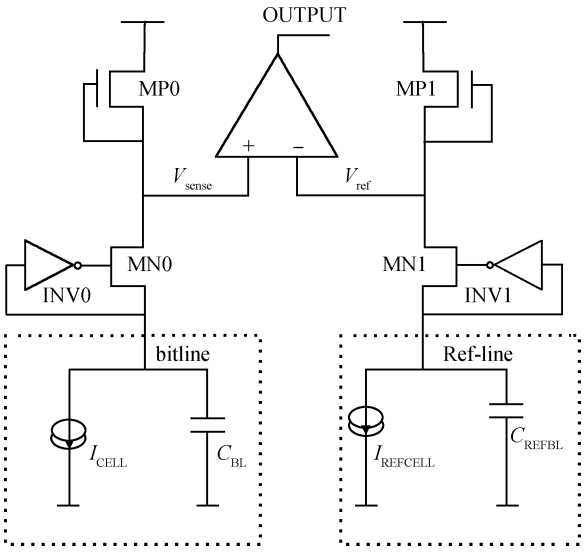

Fig. 1. Differential sense amplifier based on voltage-mode[4].

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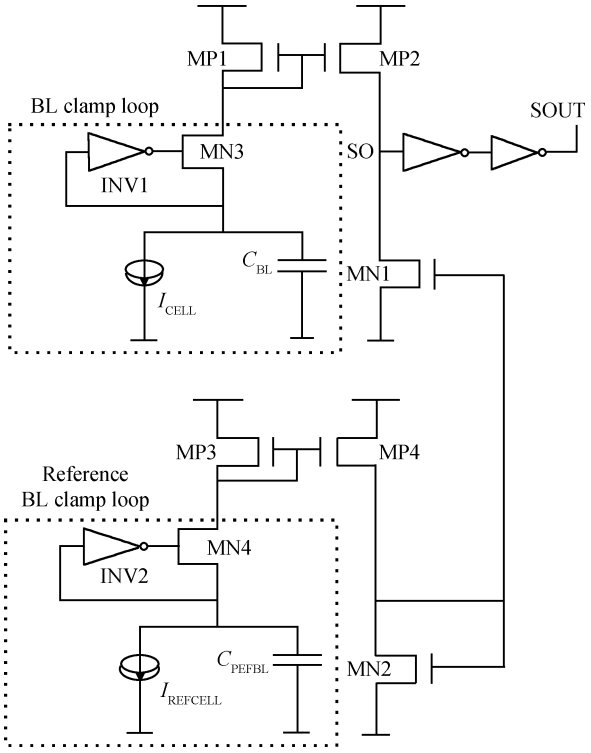

Fig. 2. Differential sense amplifier based on current-code.

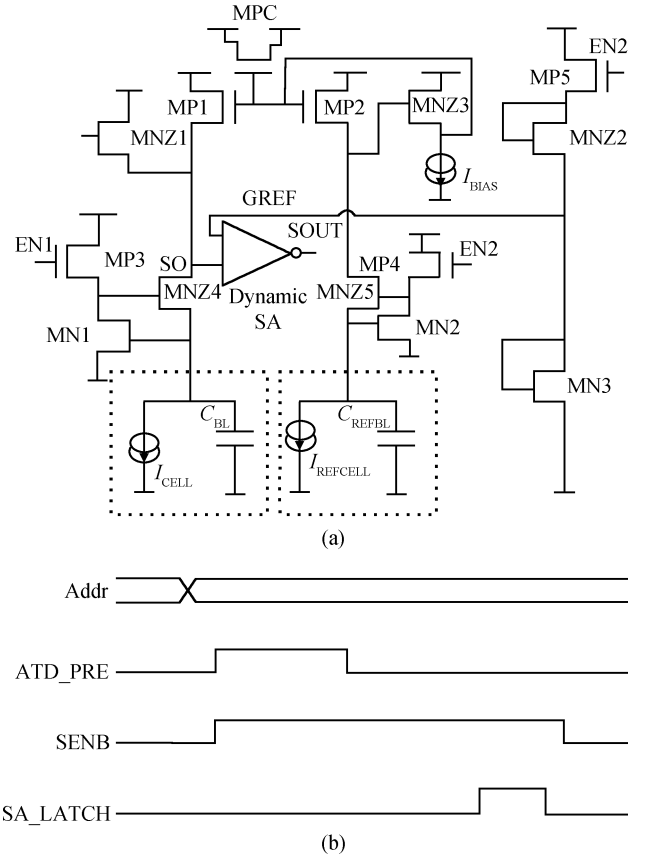

Fig. 3. (a) Circuit diagram of the proposed sense amplifier. (b) Timing diagram for the operation of the proposed sense amplifier.

The circuit is composed of cell path circuit, which extracts the cell current, a reference path circuit, which extracts reference current, and a comparison output circuit by which cell current and reference current are compared and then the result is issued. I_{CELL} is the cell current flowing through BL clamp loop and then is mirrored one time by the current mirror. $I_{REFCELL}$ is the reference current flowing through the reference BL clamp loop and then is mirrored two times by the current mirror. I_{CELL} and $I_{REFCELL}$ then are compared generating differential current converted into differential voltage on node SO, and SOUT representing the output logical value is then issued from the comparison. In addition, the BL clamp loop circuit is responsible for guaranteeing minimal mismatch between the BL voltage and the reference BL voltage, which guarantees matching between the cell and reference currents.

2.2. Drawback of the above sense amplifier

(1) The structure cannot realize a very high read access speed.

Since the relation between I_{CELL} and $I_{REFCELL}$ is unknown during pre-charge, the voltage on node SO may be any value. Even worse, the node SO will need a long time to be charged or discharged, which directly affects read access speed and even leads to error during fast access times.

(2) The structure has a bad power noise.

Taking account of high read access speeds, a large capacitance cannot be inserted into the immediate node. When the VDD suddenly varies, the PMOS's gate (MP1, MP2, MP3, MP4) or the NMOS's gate (MN1, MN2) cannot over time keep up with the variation, which directly leads to a current gap between I_{CELL} and $I_{REFCELL}$, and even worse, causes error switches on node SO and error of SOUT.

(3) The structure has low sense precision.

Current mirror pairs are used many times in the structure and process mismatch between devices is large, which directly affects the sense accuracy. Another reason is that node SO has large output swing; the channel modulation effect is fatal for sense accuracy.

(4) The structure cannot work with a low voltage supply under 1.5 V.

The equation of the lowest voltage for the structure is expressed as follows:

$$V_{DDmin} = V_{BL} + V_{dsMN3} + V_{thMP1} + V_{ovMP1}, \qquad (1)$$

where V_{BL} is at least designed as V_{th} thanks to the need for guaranteeing the size of cell current, which results in the lower work voltage is large.

(5) The structure has large power consumption.

The reference current is used only once and the cell current is duplicately used due to many bits read simultaneously. So the equation of power is expressed as follows:

$$I_{vdd} = N(I_{CELL} + I_{REF\text{-}com} + I_{BL\text{-}precharge}) + I_{REF}, \qquad (2)$$

where $I_{REF\text{-}com} = 0.35I_{CELL}$ and data 0.35 is reference cell current trip point.

In Eq. (2), N is the times that the sense amplifier is repeatly used. $I_{REF\text{-}com}$ is the reference comparison current. I_{REF} is the current of reference current generator. $I_{BL\text{-}precharge}$ is BL precharge current.

3. Proposed high-performance sense amplifier

3.1. Description of new system

The new sense structure and timing chart are illustrated in Fig. 3, making improvements in the cell path in which the cell current need not be extracted and is directly compared with the reference current, reference current management, which only uses a mirror pair adopting drain and gate separation method different from traditional method to guarantee the system can work with low voltage at 1 V, and an output adopting dynamic output amplifier named as SOAMP. The detailed description of the proposed sense amplifier is described in the following. The system firstly completes pre-charge and maintains a stable voltage on the bit-line to make matching between the cell current and the reference current through a BL clamp loop, composed of MN1, MNZ4 and MP3, and a REFBL clamp loop composed of MN2, MNZ5 and MP4 in the structure. Simultaneously, the system makes V_{SO} and V_{GREF} balanced during pre-charge, which makes the device strong when used by reducing overdrive. Once the pre-charge stage ends, the cell current, which is the current of MN3, need not be extracted and is directly compared with the reference current I_{MP1} and pre-amplified. The current of MP2 is the reference cell current. Taking the amount of low power supply operation, MN3 is inserted for separating MP2 gate voltage and drain voltage, which avoids MP2 VT suffering. The system adopts zero VT NMOS as MNZ3 in order to guarantee that MP2 is always in the saturation region. The global voltage reference block composed of MP5, MNZ2 and MN5 provides a good voltage reference to be compared with the voltage on node SO for correct and high speed output. At the same time, MNZ2 should match very well with MNZ1.

There are many merits of the new structure.

(1) The new structure enhances read access speed.

The system firstly makes V_{SO} and V_{GREF} balanced during pre-charge. A small differential voltage (named as ΔV) between them is needed because of positive feedback, which enhances read access speed.

(2) The new structure can work very well with ultra low power supply at 1 V.

The result may be obtained by the value of voltage needed by the cell path and the reference path in the new structure. It will be detailed in the first-order model section.

(3) The new structure has the good noise immunity.

Decouple capacitance MPC is inserted between MP1 gate and V_{DD}. The reference current is always on, which takes an amount of speed and results in V_{DD} noise being completely added to MP1 gate. Current gap does not vary with V_{DD} noise, so good noise immunity performance can be obtained.

3.2. First order modeling

First order modeling is necessary to drive the design before simulations. The objective of the sense amplifier is to achieve its performance target in terms of access time and low voltage. We will firstly discuss the lowest work voltage from the cell path and the reference path. The equation of the lowest work voltage of cell path will be expressed as follows:

$$V_{\text{DD cell-min}} = V_{\text{thMN1}} + V_{\text{dsMNZ4}} + V_{\text{dsMP1}} + V_{\text{dsMN1}}, \quad (3)$$

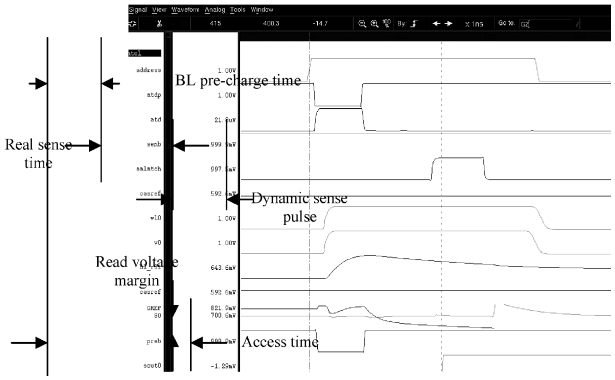

Fig. 4. Read operation simulated wave.

where if $V_{\text{thMN1}} = 0.7$ V, $V_{\text{dsMNZ4}} = 50$ mV, $V_{\text{dsMN1}} < 50$ mV and $V_{\text{dsMP1}} = 150$ mV, $V_{\text{DDmin}} < 0.95$ V.

In the reference path, the equation of the V_{DD} is as follows:

$$V_{\text{DD ref-min}} = V_{\text{thMN2}} + V_{\text{dsMNZ5}} + V_{\text{dsMP2}}, \quad (4)$$

where if $V_{\text{thMN2}} = 0.7$ V, $V_{\text{dsMN5}} = 100$ mV and $V_{\text{dsMP2}} = 100$ mV, $V_{\text{DDmin}} = 0.9$ V.

The result exhibits the sense amplifier may work with low-voltage at 1 V.

Secondly, for read access time, read operation delay can be written as:

$$T_{\text{total-delay}} = T_{\text{BL}} + \frac{\Delta V C_{\text{SO}}}{\Delta I} + T_{\text{dynamic}}, \quad (5)$$

where $\Delta V = |V_{\text{SO}} - V_{\text{GREF}}|$, $\Delta I = |I_{\text{cell}} - I_{\text{ref}}|$ C_{SO} is metal line capacitance and parasitic capacitance on node SO, including C_{MP1dg}, C_{MNZ1sg}, C_{MNZ4dg}, $C_{\text{dynamicsa}}$ and junction capacitance. The capacitance must be minimized taking amount of high-speed read access. T_{dynamic} is the delay of second-stage amplifier varying normally from 2 to 5 ns.

Generally speaking, ΔI has been designed by a process team before circuit design. However, there is still a different access time of the read operation of data-1and data-0.

When data-1 is read, I_{CELL} is equal to the result of I_{MNZ1} added to current I_{MP1}, and I_{REF} is equal to I_{MP1} after pre-charge stage ends, so ΔI is actually equal to current I_{MNZ1} by the expression of differential current ΔI. V_{SO} begins to go down thanks to differential current ΔI, which generates differential voltage ΔV. When the ΔV meets the requirement of the dynamic sense amplifier, data-1 will be issued.

When data-0 is read, I_{CELL} is smaller than I_{REF}. MNZ1 should be cut-off due to a small cell current during BL pre-charge. The V_{SO} does not have equilibrium point and will continue to go up until MP1 goes into the linear region, which leads to larger ΔV enabling second-stage amplifier over a short time. So operation for data-0 has higher read speed than that for data-1 in the new design.

4. Results

The simulated waveforms of the proposed sense amplifier are shown in Fig. 4. The read margin is defined as the voltage difference between V_{SO} and V_{GREF} at the beginning of dynamic

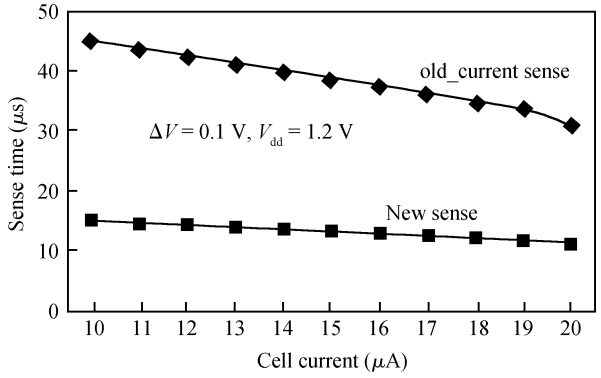

Fig. 5. Sense time with respect to cell current.

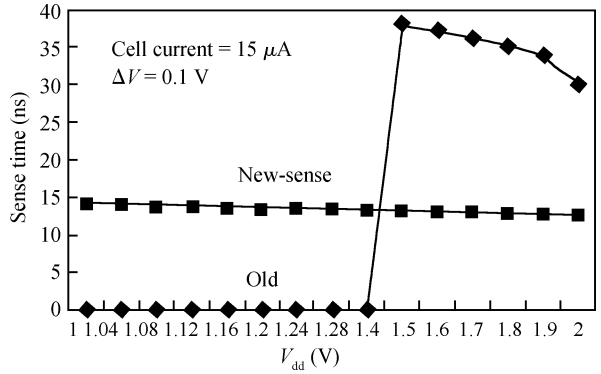

Fig. 6. Sense time with respect to V_{DD}.

sense being enabled. It can be seen that read access time is composed of three parts. They are, respectively, BL precharge time, real sense time and dynamic sense pulse. For flash memory, data is stored in a memory cell as a threshold voltage change accomplished by injecting or extracting electrons in its floating gate. In other words, the cell current of the selected memory cell is changed according to the stored data. As has been known, the delay of operation for data-0 is shorter than that for data-1 in the first order model due to the different cell current of data-1 and data-0. Figure 5 shows the simulation result with respect to cell current. Cell current is distributed by the cell current of 0-data and 1-data. As can been observed, the new system needs smaller sense time than the old system, and sense time is not sensitive to cell current in an individual region. So we can expect a very limited access time variation due to the memory cell current variation using the proposed sense amplifier. Simultaneously, cell current relative to data-1 needs much more delay than cell current relative to data-0.

As has been mentioned, the new structure can work with low voltage at 1 V. Figure 6 illustrates the sense time with respect to the supply voltage using new proposed sense amplifier. It is clear that the proposed sense amplifier has a smaller sense time at a wide range of supply voltage that is larger than or equal to 1 V. Therefore, the proposed sense amplifier is very suitable for low voltage applications.

Figure 7 represents the comparison of the current consumption of the new sense amplifier with a conventional amplifier both used in read of 32 bits. The current consumption is estimated as an average value in one read cycle. As can been seen

30 μA	28 μA	Control block
5 μA × 32	25 μA × 32	Sense amp current mirror
50 μA × 32	48 μA × 32	Bitline charge
20 μA	0 μA	GREF GEN
78 μA	65 μA	Irefcell GEN
5 μA × 32	0	Dynamic sense
5 μA × 32	5 μA × 32	BL clamp
2.2 mA	2.6 mA	Total current consumption

Fig. 7. Current consumption comparison between proposed and conventional structure.

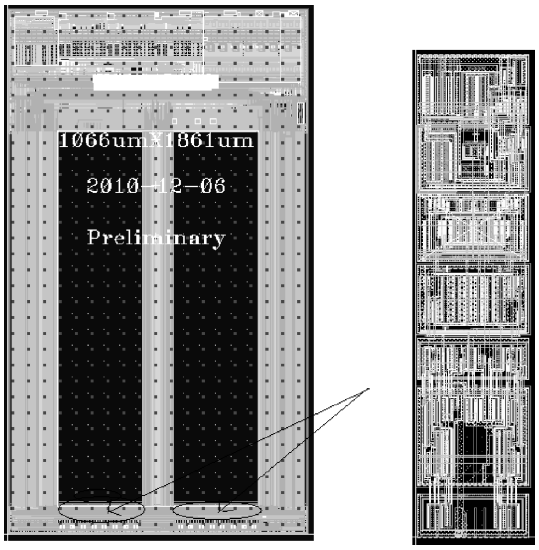

Fig. 8. Flash memory and sense amplifier layout.

in Fig. 7, current consumption is much smaller using new sense amplifier than in a conventional scheme. There are mainly two reasons for this. One is that new structure reduces the current mirror number used, and the other is that current mirror used adopts a new method. Likewise, based on new current mirror method, reference cell current generation circuit consumes smaller consumption than a conventional structure. Total current consumption is reduced by about 15%.

Through these simulations, it can be seen that the new structure has advantages over a conventional sense amplifier. Firstly, it can work with low voltage at 1 V and has a smaller consumption than a conventional sense amplifier. Secondly, it has smaller read access time than conventional structure.

A 64k × 32 memory with a sense amplifier has also

Table 1. Test result of memory with the sense amplifier.

V_{DD} (V)	1.0	1.1	1.2	1.3	1.4	1.6	1.7	1.8	2
T_{aa_x} (ns)	16.5	16	16	15	13	12.5	12	12	13
T_{aa_y} (ns)	16.5	16	16	15	13	12.5	12	12	13

been simulated based on SMIC 90nm process and about 100%–200% improvement of the access time has been obtained at 1 V. Because of the direct sensing scheme both the reliability and the performances of the memory are optimized. The layouts of the flash memory and the sense amplifier are illustrated in Fig. 8. Simultaneously, the test result is shown in Table 1. In the table, T_{aa_x} represents access time relative to the change of X address and T_{aa_y} represents access time relative to the change of Y address.

As can be seen, the access time relative to voltage V_{DD} in the table is slower than that in design simulation and the gap ranges from 0.5 to 1 ns. Simultaneously, the total current consumption of test is around 2.25 mA, which is nearly equivalent to that of design simulations under the same condition.

5. Conclusion

A new sense amplifier for flash memory has been designed in this paper. Low-voltage reference current extraction and a dynamic output approach are employed to realize performance indicators such as low voltage and high speed. The sense time is enhanced a great deal according to the simulation result. The amplifier can work with low voltage at 1 V and the power of single dynamic amplifier is optimized by 15%.

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