ESD robustness studies on the double snapback characteristics of an LDMOS with an embedded SCR*

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Abstract: Criterion for the second snapback of an LDMOS with an embedded SCR is given based on parasitic parameter analysis. According to this criterion, three typical structures are compared by numerical simulation and structural parameters which influence the second snapback are also analyzed to optimize the ESD characteristics. Experimental data showed that, as the second snapback voltage decreased from 25.4 to 8.1 V, the discharge ability of the optimized structure increased from 0.57 to 3.1 A.

Key words: ESD; LDMOS; SCR; double snapback

DOI: 10.1088/1674-4926/32/9/094002 **EEACC:** 2560

1. Introduction

Double snapback is a special phenomenon that often occurs in high voltage (HV) devices under electro-static discharge (ESD) stress. After conventional snapback caused by the triggering of parasitic bipolar, an additional snapback may occur and influence the ESD characteristics[1].

For an LDMOS used as an ESD protection device, it should have excellent current discharge ability and clamp the ESD stress voltage at a low level as quickly as possible. The current discharge ability of ESD protection devices is always determined by the second breakdown current (I_{t2}), which is closely related with the power dissipation. However, a second snapback with a high voltage and current weakens the ESD robustness. First of all, power dissipation is determined as $P = IV$. With the high voltage and current of the second snapback (V_{S2}, I_{S2}), the power dissipation increases quickly and generates a lot of heat. As a result, the devices are susceptible to burn out at a low discharge level. Secondly, high V_{S2} leads to a high peak voltage that threatens the internal circuits with a thin oxide. Thirdly, high V_{S2} also slows down the voltage clamp speed, and leads to deterioration under a machine model (MM) and charge device model (CDM) event.

In an HV process, laterally diffused MOS (LDMOS) are widely integrated for their good operative performances and process compatibility[2, 3]. In order to get reliable ESD protection with smaller layout size in these built-in LDMOS process, an LDMOS with an embedded silicon-controlled rectifier (SCR) is an excellent choice, not only for its good discharge ability but also because it can be fabricated without additional masks or process steps[4–6].

In this paper, the double snapback characteristics of an LDMOS with an embedded SCR (LDMOS-SCR) are studied, and a criterion for second snapbacks is proposed based on consideration of the parasitic parameters. According to this criterion, LDMOS-SCRs with optimized double snapback characteristics are analyzed with a numerical simulator, and verified by experiment and transmission line pulsing (TLP) testing.

2. Criterion for double snapback characteristics of an LDMOS-SCR

The cross-section of an LDMOS-SCR structure is shown in Fig. 1, in which a P^+ implant region is added in NW between the channel and the N^+ implant, and this structure is defined as structure A. From Fig. 1, PNP and NPN constitute the parasitic SCR and form a main discharge path; R_{PW} is the base resistor for an NPN and significantly influences the first snapback characteristics; R_{NW} is the parasitic resistors in the drift region below shallow trench isolation (STI) and it is bound up with the device breakdown voltage by the length of the drift region. As shown in the current discharge path, the parasitic resistors which influence the double snapback characteristics can be classified as lateral resistor R_{LP} below P^+ implant, lateral resistor R_{LN} and vertical resistor R_{VN} below N^+ implant.

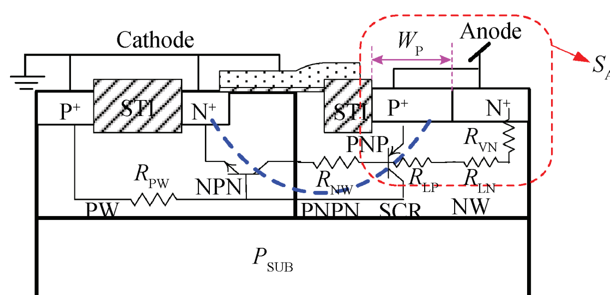

Fig. 1. Cross-sectional view of an LDMOS-SCR (structure A) with important parasitic parameters, in which the drain side structure is labeled as S_A in dash box.

* Project supported by the Analog Devices Inc and the National Natural Science Foundation of China (No. 60906038).
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Received 17 March 2011, revised manuscript received 9 May 2011
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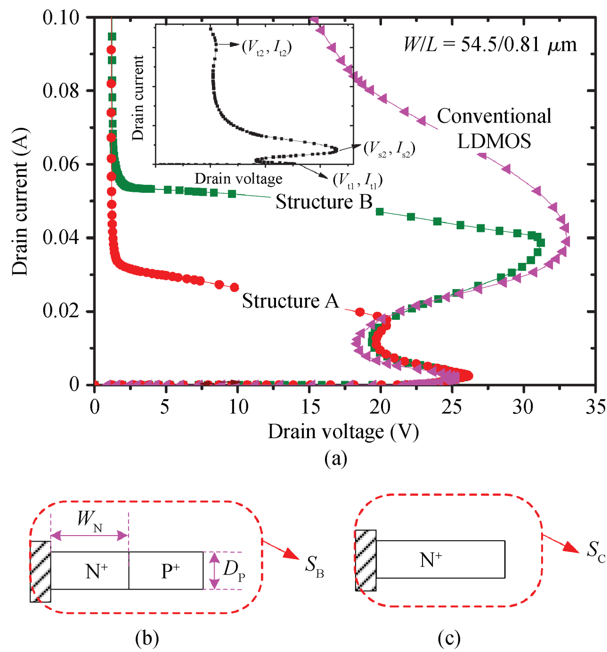

Fig. 2. (a) Sentaurus simulated I–V curves for conventional NLDMOS and structure A / B. Local cross sectional views at the drain side of (b) structure B (LDMOS-SCR) and (c) conventional NLDMOS, which are contrasted with structure A in dash box $S_{\rm A}$ of Fig. 1.

After the first snapback caused by the triggering of parasitic NPN, current flows from drain N$^+$ to the source and a voltage is dropped on the parasitic resistors between the P$^+$ and NW region. When this voltage drop is high enough to forward bias the EB junction of PNP ($V_{\rm EB,\,on}$), this parasitic bipolar turns on and the SCR begins to discharge ESD current. Then current increases sharply at low voltage and a second snapback presents in the I–V curve. Thus, the criterion for double snapback of an LDMOS-SCR can be obtained as:

$$I_{\rm S2}(R_{\rm LP}+R_{\rm LN}+R_{\rm VN}) \geqslant V_{\rm EB,\,on}, \quad (1)$$

in which $I_{\rm S2}$ is the total discharge current when the second snapback occurs.

Double snapback characteristics of conventional NLDMOS and two LDMOS-SCRs are compared to substantiate our analysis. As shown in Figs. 1, 2(b) and 2(c), LDMOS-SCRs have additional P$^+$ implanted in the drift region NW compared with conventional NLDMOS. Structures A and B share almost the same dimension but are distinguished by the relevant location of N$^+$ and P$^+$ in the NW region.

Sentaurus$^{\rm TM}$ simulated I–V curves for NLDMOS with structures A and B are shown in Fig. 2(a). Device simulations in this paper used uniform doping to simply our discussion. Although the specific values for ESD characteristics are not precise, these simulation data still represent the variation trend well.

Unlike in LDMOS-SCRs, the second snapback in NLDMOS is caused by the altering of electric field distribution. With more and more carriers injected into the drift region, the peak of electric field alters from PW/NW junction to the N$^+$/NW junction and leads to a second snapback[3].

With identical dimension of N$^+$ in drain, structures A and B share almost the same $R_{\rm LN}$ and $R_{\rm VN}$. Before the second snapback occurs, the parasitic NPN is the main discharge device, all the currents flow to the N$^+$ region in NW. In that case, few currents flow to the P$^+$ region in NW and no effective $R_{\rm LP}$ in structure B contribute to the second snapback. Then,

$$\frac{I_{\rm S2.a}}{I_{\rm S2.b}} = \frac{R_{\rm VN}+R_{\rm LN}}{R_{\rm VN}+R_{\rm LN}+R_{\rm LP}}. \quad (2)$$

According to Eq. (2), the current needed for a second snapback is mainly determined by the parasitic resistors below N$^+$ and P$^+$ in NW. Because of higher $R_{\rm LP}$, structure A has a much lower $I_{\rm S2}$. From the simulation results with devices dimensions (W/L) of 54.4 μm/0.81 μm, $I_{\rm S2}$ of structure B is 0.039 A, while that of structure A is only 0.018 A. Thus, $R_{\rm LP}$ of structure A can be calculated out as 20.94 Ω with Eqs. (1) and (2). Meanwhile, $R_{\rm LP}$ also can be obtained with device parameters: in this simulation, uniform concentration of 7.42×10^{16} cm^{-3} is used for NW, and junction depth of NW and P$^+$ are respectively 1 μm and 0.2 μm, then $R_{\rm LP}$ can be calculated out as 10.04 Ω with rectangle approximate. However, indeed current flows are mainly concentrated only in half of the NW depth, so $R_{\rm LP}$ calculated with structural parameters approximate to 20 Ω, which is very close to the value obtained from Eqs. (1) and (2).

Before a second snapback, discharge current rises up steadily with voltage stress on the anode. With lower $I_{\rm S2}$, a much smaller $V_{\rm S2}$ is resulted for structure A. As shown in Fig. 2, $V_{\rm S2}$ of structure B is 31.2 V, while that of structure A is only 20.4 V which is even lower than the trigger voltage ($V_{\rm t1}$) of 26.0 V.

3. Structure optimization and TLP test

In order to obtain lower $I_{\rm S2}$ and $V_{\rm S2}$ for better ESD robustness, optimizations with larger $R_{\rm LP}$, $R_{\rm LN}$ and $R_{\rm VN}$ are conducted according to Eq. (1).

The influence of P$^+$ width (labeled as $W_{\rm P}$ in Fig. 1) in the second snapback of structure A is studied. As shown in Fig. 3(a), $V_{\rm S2}$ of structure A with different P$^+$ width are all lower than $V_{\rm t1}$ because of larger resistor $R_{\rm LP}$. Furthermore, $R_{\rm LP}$ becomes even larger with wider P$^+$ region, and the parasitic PNP is much easier to be triggered, thus $V_{\rm S2}$ and $I_{\rm S2}$ are both cut down by increased $W_{\rm P}$.

By structural optimization, lower $V_{\rm S2}$ and $I_{\rm S2}$ of structure B also can be obtained. Smaller N$^+$ width (labeled as $W_{\rm N}$ in Fig. 2(b)) will increase $R_{\rm VN}$ by reducing the vertical current flowing area; while this change also decreases $R_{\rm LN}$ for shorter discharge path. However, the effect of $R_{\rm VN}$'s increase is the dominant factor here, and leads to larger summation of these two resistors. As shown in Fig. 3(b), $V_{\rm S2}$ of structure B is lower than $V_{\rm t1}$ when N$^+$ width is 0.4 μm or smaller. Furthermore, with deeper P$^+$ junction (labeled as $D_{\rm P}$ in Fig. 2(b)), the effective vertical current path get longer, and larger $R_{\rm VN}$ also can be obtained. As shown in Fig. 3(c), with P$^+$ depth of 0.4 μm or deeper, structure B has $V_{\rm S2}$ lower than $V_{\rm t1}$.

A TLP generator with a pulse width of 100 ns and rise time of 2–10 ns is used to measure the snapback I–V characteristics of the devices under study. The test results are shown in Fig. 4 and Table 1.

These three structures share the same breakdown voltage under DC test and almost the same trigger voltage. The second

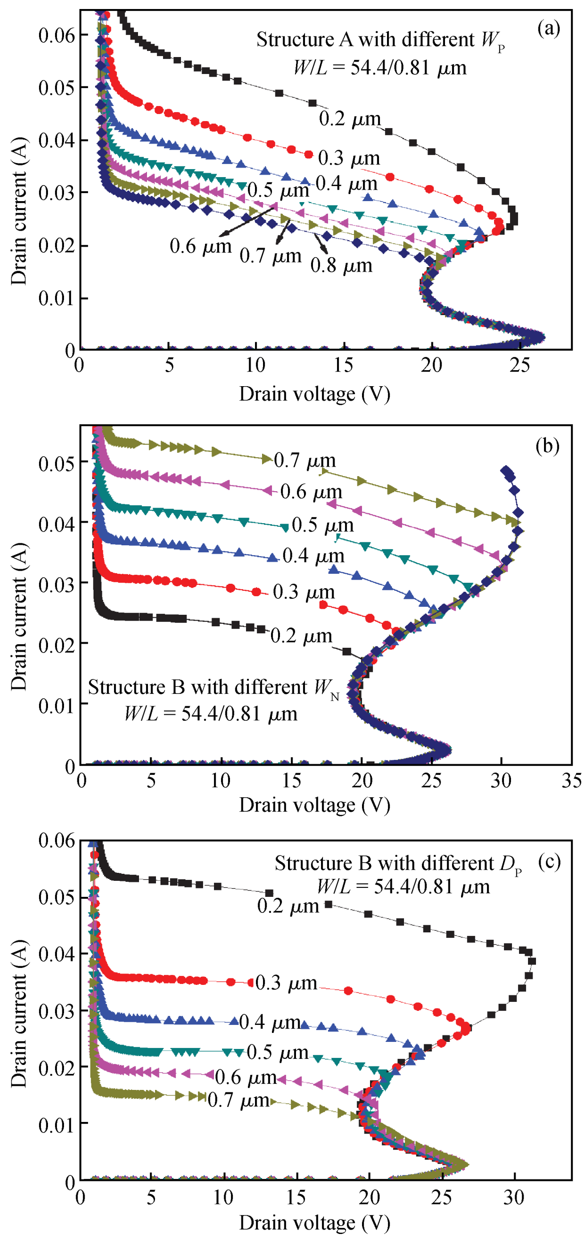

Fig. 3. Simulation results of voltage and current at the second snapback for structural optimization. (a) Structure A with different P^+ widths. (b) Structure B with different N^+ widths. (c) Structure B with different P^+ depths.

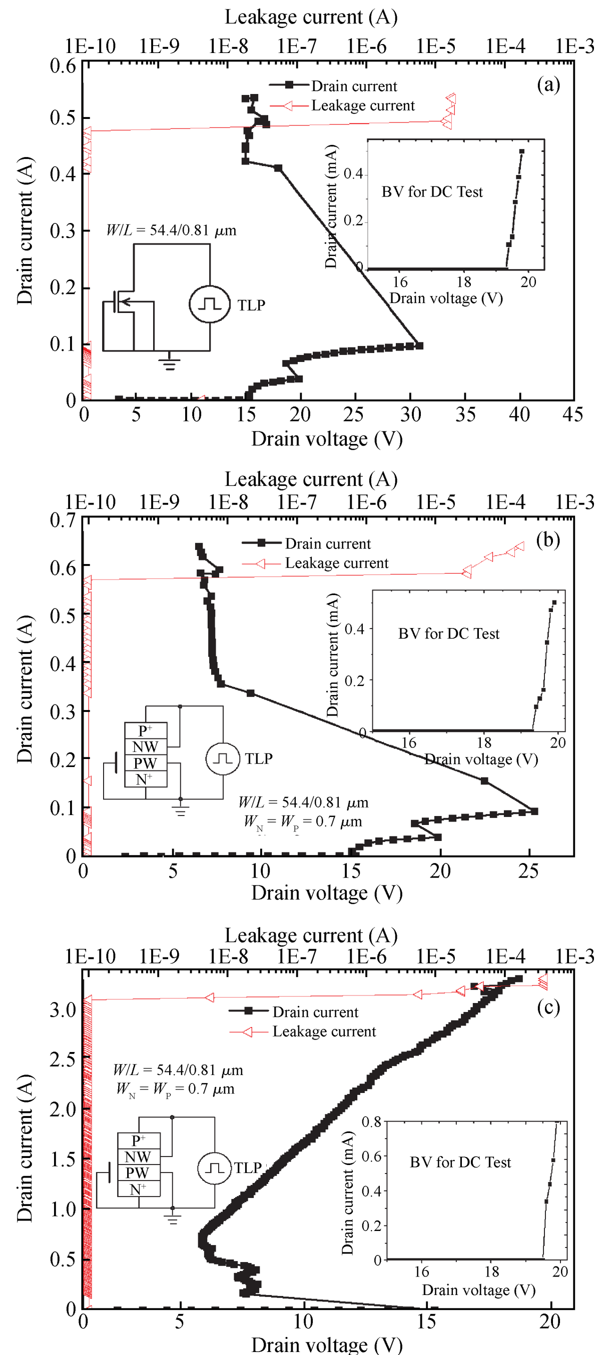

Fig. 4. TLP-measured I–V characteristic of (a) conventional NLDMOS, (b) structure B, (c) structure A fabricated in a 0.5 μm 5 V CMOS process.

snapback of the NLDMOS occurs at 30.9 V compared with the trigger voltage of 15.5 V. As discussed before, high V_{S2} weakens down the ESD robustness, and conventional NLDMOS has very low I_{t2} of 0.48 A.

For structure B, the second snapback voltage decreases to 25.3 V. Although the embedded SCR turns on after the second snapback, and clamps the voltage at about 6.8 V, its discharge ability is limited by the heat generated before the second snapback. I_{t2} of structure B is only 0.57 A, which is still too weak to be used as a robust ESD protection device.

Structure A has much better ESD characteristics. As V_{S2} is less than V_{t1}, the device discharge at a low voltage level. Without high power dissipation and high electric field caused by V_{S2}, structure A has excellent I_{t2} of 3.1 A.

Table 1. DC and TLP test results for conventional NLDMOS, structures A and B.

	BV (DC) (V)	V_{t1} (V)	V_{S2} (V)	I_{t2} (A)
NLDMOS	19.3	15.3	30.9	0.48
Structure B	19.3	15.5	25.3	0.57
Structure A	19.3	15.3	8.1	3.1

4. Conclusion

Double snapback characteristics strongly influence the ESD protection robustness. Higher V_{S2} and I_{S2} will lead to

higher power dissipation, higher peak voltage and slower voltage clamp speed. With structural analysis, criterion of the second snapback of an LDMOS-SCR has been proposed in this paper. According to this criterion, it is suggested that device optimization for double snapback should be focused on the parasitic resistors below N^+ and P^+ in the drain region. The criterion is also confirmed by both the numerical simulations and TLP test with different structural parameters. From the test results, structure A with optimized structural parameters has an excellent I_{t2} of 3.1 A which is 5–6 times of the conventional NLDMOS and structure B.

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