Harmonic-suppressed quadrature-input frequency divider for OFDM systems*

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Abstract: A fully balanced harmonic-suppressed quadrature-input frequency divider is proposed. The frequency divider improves the quadrature phase accuracy at the output by using both input I/Q signals. Compared with conventional dividers, the circuit achieves an output I/Q phase sequence that is independent of the input I/Q phase sequence. Moreover, the third harmonic is effectively suppressed by employing a double degeneration technique. The design is fabricated in TSMC 0.13-μm CMOS and operated at 1.2 V. While locked at 8.5 GHz, the proposed divider measures a maximum third harmonic rejection of 45 dB and a phase noise of –124 dBc/Hz at a 10 MHz offset. The circuit achieves a locking range of 15% while consuming a total current of 4.5 mA.

Key words: quadrature-input; Miller divider; UWB
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1. Introduction

In a classical PLL used in orthogonal frequency division multiplexing (OFDM) frequency synthesizers, such as the ultra-wide band (UWB), both quadrature voltage-controlled oscillators (QVCO) and frequency dividers are employed to provide the required quadrature signals at every stage[1, 2]. Most of these quadrature signals are necessary in order to produce the desired LO frequencies by using a single-sideband (SSB) mixer.

To achieve the correct upper-sideband or lower-sideband selection, a deterministic quadrature phase sequence is required at the inputs of the SSB mixer. However, the output phase sequence of the QVCO is typically uncertain. The LC tank adopted in the first divider always introduces another uncertain phase shift. The uncertainties of the input phase sequence cause the SSB mixer to work incorrectly.

Conventional frequency dividers, such as dynamic frequency dividers, only need differential input signals to achieve divide-by-2 operation[3]. An identical dummy divider is normally implemented. The dummy divider doubles power consumption and chip area. For example, the frequency divider in Ref. [3] draws 16.8 mW and occupies an area of 0.5×0.7 mm^2 for a differential input signal. When cascaded with a quadrature signal generator, the same two frequency dividers will be required to match the load. Therefore, the first divider will dissipate 33.6 mW, which is unacceptable for a phase-locked loop. Moreover, the output phase accuracy of conventional frequency divider is dependent on the accuracy of the input phase. The phase mismatch accumulates from the first divider to the last divider. The signal quality of an OFDM UWB eventually deteriorates. In addition, a phase error of less than 3° is required OFDM UWB systems. The unwanted sideband has to lie 32 dB lower than the wanted sideband. However, the existing frequency divider can only suppress the sideband by about 20 dB.

To overcome all of the problems mentioned above, a harmonic-suppressed quadrature-input divide-by-2 frequency divider is proposed. The frequency divider achieves an output I/Q phase sequence that tracks the input I/Q phase sequence. The output phase accuracy of the proposed Miller-based divider is independent of input phase accuracy. Meanwhile, the proposed divider achieves better I/Q loading to the QVCO and lower power consumption by removing the dummy divider. The output harmonics of the divider are suppressed effectively by using a double degeneration technique. The divider achieves a maximum harmonic suppression of 45 dB. The analytical model and transistor level implementation of the proposed circuit are presented in detail.

2. Circuit analysis and design

As shown in Fig. 1, a conventional Miller divider consists of a feedback loop with a mixer, driven by the divider's output signal, and a band-pass filter in the forward path. In order for the feedback loop to operate properly, the total phase shift around the loop must be zero and the loop gain must be at least unity.

In a balanced Miller divider, the mixer input signal has no

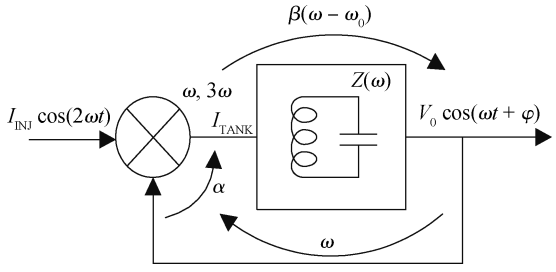

Fig. 1. Behavioral block diagram of the Miller divider.

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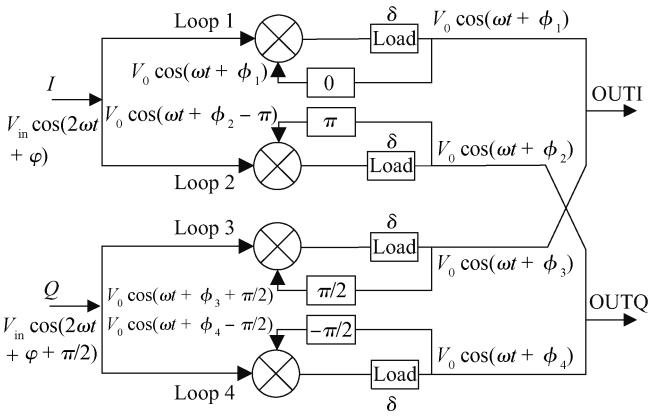

Fig. 2. Simplified block diagram of a quadrature input divider.

DC term. The balanced mixer can compensate for an arbitrarily large phase shift introduced by the LC tank[4]. If the loop gain is higher than unity, the loop regenerates oscillation. In other words, the divider is always locked as long as the output voltage is large enough to force the switching pair to communicate. The operation range can be extended by dynamically regulating the bias current. Furthermore, the differential driving of the balanced divider makes the accuracy of output waveforms insensitive to amplitude and phase mismatches of the input signals.

To provide exact quadrature outputs and to employ both I/Q inputs, a harmonic-suppressed quadrature-input frequency divider based on a balanced Miller divider is proposed. The frequency divider comprises four different feedback loops with an appropriate phase shift and, by using the divider, the output phase sequence tracks the input phase sequence. Moreover, the output phase accuracy of the proposed divider is independent of input phase accuracy.

A behavioral block diagram of the quadrature-input frequency divider is shown in Fig. 2. Four balanced Miller dividers are employed in this circuit. Loops 1 and 3 are combined to form in-phase outputs, the other two loops are for quadrature outputs. The added loops 3 and 4 are used to generate the deterministic phase sequence. To simplify the analysis, it can be assumed that the in-phase input lags the quadrature input by $\pi/2$. The input signals are represented by $V_{\text{in}}\cos(2\omega t+\varphi)$ and $V_{\text{in}}\cos(2\omega t+\varphi+\pi/2)$, respectively. The initial phase for the input signal is denoted by φ. The output signal at each loop is given by $V_0\cos(\omega t+\phi_{\text{i}})$. The phase shift introduced by the tank is δ. In loop 1, the output current is expressed by

$$I_1=\frac{1}{2}V_{\text{in}}V_0\left[\cos\left(3\omega t+\varphi+\phi_1\right)+\cos\left(\omega t+\varphi-\phi_1\right)\right]. \tag{1}$$

This equation shows that a phase shift of $\varphi-2\phi_1$ is needed to compensate the tank's phase shift. As a consequence, the output phase in loop 1 is given by

$$\phi_1=(\delta+\varphi)/2. \tag{2}$$

A 180° phase shift is introduced in loop 2, the output phase in loop 2 is

$$\phi_2=\phi_1+\frac{\pi}{2}. \tag{3}$$

From the above equation, loops 1 and 2 achieve the quadrature output.

A 90° phase shift is introduced in loops 3 and 4, respectively. The output of loop 3 is tied to the output of loop 1. The output phase of loop 3 becomes

$$\phi_3=\phi_1. \tag{4}$$

Loops 1 and 3 have the same phase. A larger loop gain can be expected from this connection. Finally, adding the output of loops 1 and 3 gives the output signal OUTI.

$$\begin{aligned}\text{OUTI}&=I_1+I_3\\&=\frac{1}{2}V_{\text{in}}V_0\cos\left(\omega t+\varphi-\phi_1\right)+\frac{1}{2}V_{\text{in}}V_0\cos\left(2\omega t+\varphi-\phi_3\right)\\&=V_{\text{in}}V_0\cos\left(\omega t+\varphi-\phi_1\right)=V_{\text{in}}V_0\cos\left(\omega t+\varphi/2-\delta/2\right).\end{aligned} \tag{5}$$

Similarly, the output of OUTQ is expressed by

$$\text{OUTQ}=V_{\text{in}}V_0\cos\left(\omega t+\varphi/2-\delta/2+\pi/2\right). \tag{6}$$

From the above equations, the output phase sequence tracks the input phase sequence as desired. The phase uncertainty found in conventional dividers is eliminated.

Without loss of generality, it can be assumed that a phase error of θ exists at the in-phase input and that no phase error exists at the quadrature input. The output of OUTQ remains unchanged. The output of OUTI is approximately given by

$$\text{OUTI}=\frac{1+\cos\theta}{2}V_{\text{in}}V_0\cos\left(\omega t+\varphi/2-\delta/2\right). \tag{7}$$

According to Eq. (7), the phase mismatch at the input translates into the amplitude mismatch. The phase accuracy of the proposed divider at the output is independent of the phase accuracy at the input.

A detailed schematic of the proposed divider is shown in Fig. 3. The proposed divider consists of 4 balanced Miller dividers. The inverted phase shift is realized by interchanging the differential feedback in loop 2. Cross-coupling the mixers used in loops 3 and 4 introduces a 90° phase shift. The output signals are fed back to the switching pairs. The input signals are connected with the transconductance stage rather than the switching stage. This solution decreases the capacitive loading to the previous stage with lower power consumption. To extend the operation frequency range, a 3 bits current DAC is adopted. The biasing current ranges from 4.5 to 8 mA with a 0.5 mA step. The proposed divider employs the degeneration technique in both the switching stage and the transconductance stage to further improve the linearity. Here, R17–R20 linearize the switching stage transistors M11–M26 with no voltage headroom consumption. The transconductance-stage devices also get degenerated by R9–R16.

To verify the independence of the output phase accuracy, a passive quadrature mixer is used to up-convert a 100 MHz quadrature baseband signal[5]. The orthogonality of the output is calculated by the relative rejection of the unwanted sideband (image rejection ratio), assuming that the 100 MHz baseband signal is in exact quadrature[6]. The four output terminals of the

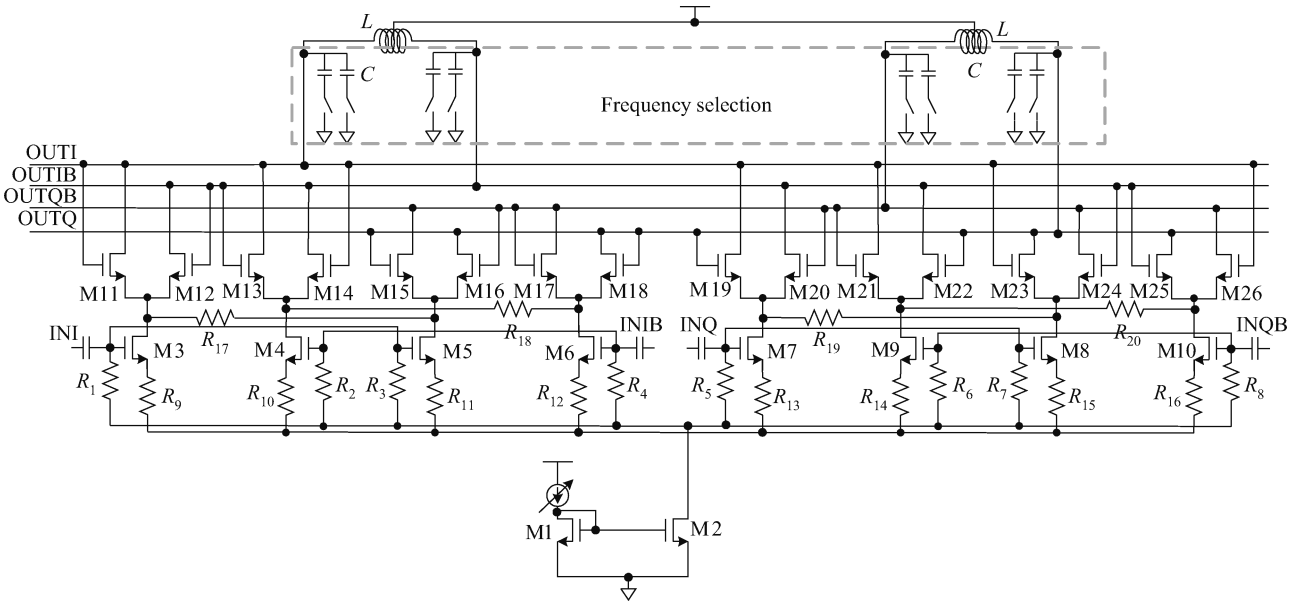

Fig. 3. Schematic block diagram of the QIQO divider.

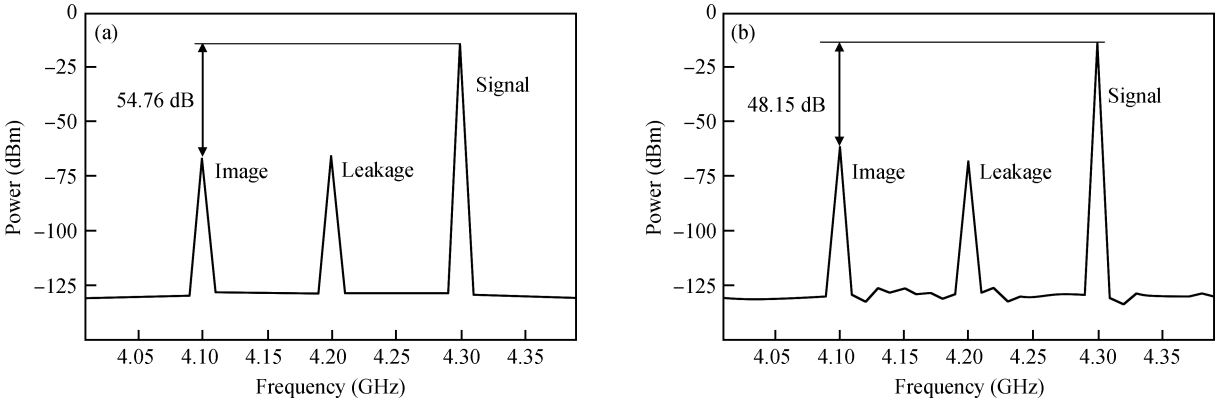

Fig. 4. Output spectra for the highest image rejection. (a) 5° phase error at the input. (b) 20° phase error at the input.

proposed divider are connected to the gates of the mixer, without a buffer. Due to the inaccuracies in amplitude and quadrature caused by mismatches in the divider and mixer, some energy will leak into the output spectrum. When a 5° phase error exists at the input of the proposed divider, the unwanted sideband lies 54.76 dB lower than the wanted sideband, as shown in Fig. 4(a). The gain in the passive mixer is expected to be exactly the same, implying that output signals of the proposed divider are less than 1° from perfect quadrature. Figure 4(b) shows an extreme case in which 10° phase mismatch occurs at the input of the proposed frequency divider. The image rejection of 48.15 dB, which corresponds to a phase error of 0.45°, is achieved. As expected, the output phase accuracy is not sensitive to phase mismatches of the input.

Quadrature-input frequency dividers with and without double degeneration are simulated with the same operating frequency and power dissipation. The output spectra of the two circuits are shown in Fig. 5. The double degeneration technique suppresses the third harmonic by 12 dB.

Compared with conventional dividers, the proposed harmonic-suppressed quadrature-input divider achieves better-matched input loading to the QVCO with a smaller power consumption by using both input I/Q signals. The phase accuracy of the input I/Q signals does not affect the phase accuracy of the output I/Q signals. The proposed divider improves quadrature phase accuracy. In addition, the third harmonics are effectively suppressed.

3. Experimental results

The harmonic-suppressed quadrature-input divider is fabricated in a TSMC 0.13-μm CMOS process and operates at 1.2 V. Figure 6 shows the chip photograph of the proposed divider. The circuit occupies an active area of 0.72×0.28 mm^2 excluding testing pads, and consumes a total current of 4.5 mA as the input frequency varies from 8.54 to 9.85 GHz.

The circuit has been tested on a PCB board. The quadrature voltage controlled oscillator is used to deliver the required quadrature LO signals. A one-stage common-source amplifier is implemented as the test buffer. The output signal is ana-

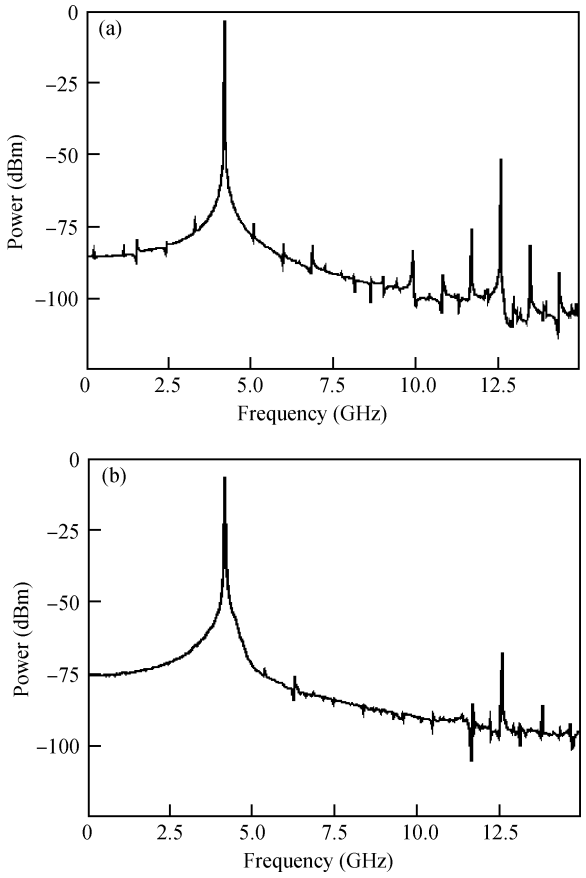

Fig. 5. Simulated spectra of frequency dividers (a) without and (b) with double degeneration.

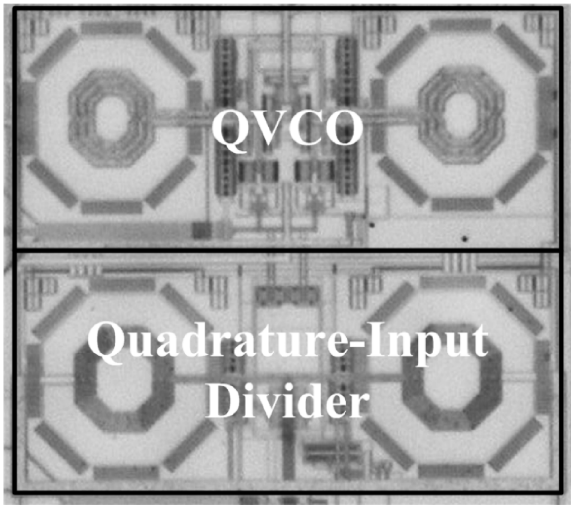

Fig. 6. Chip photo.

lyzed by using an Agilent E4440A spectrum analyzer. Figure 7 shows the output spectra of the QIQO divider at the minimum and maximum input frequencies with maximum third harmonic suppressions of 45 dB and 36 dB. The locking range of the proposed divider is limited by the frequency tuning range of the QVCO.

To verify the noise contribution of the proposed divider, the phase noise at both the QVCO and divider outputs are mea-

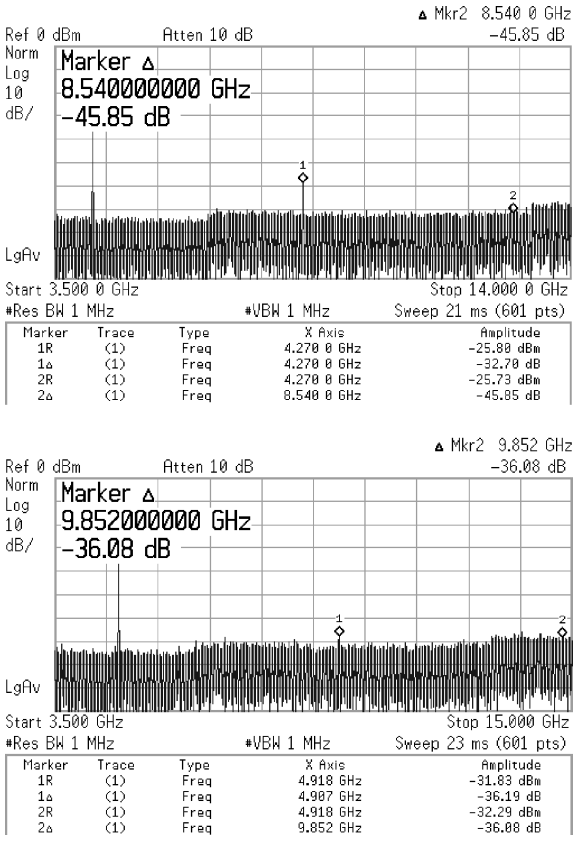

Fig. 7. Measured output spectra of the quadrature-input frequency divider.

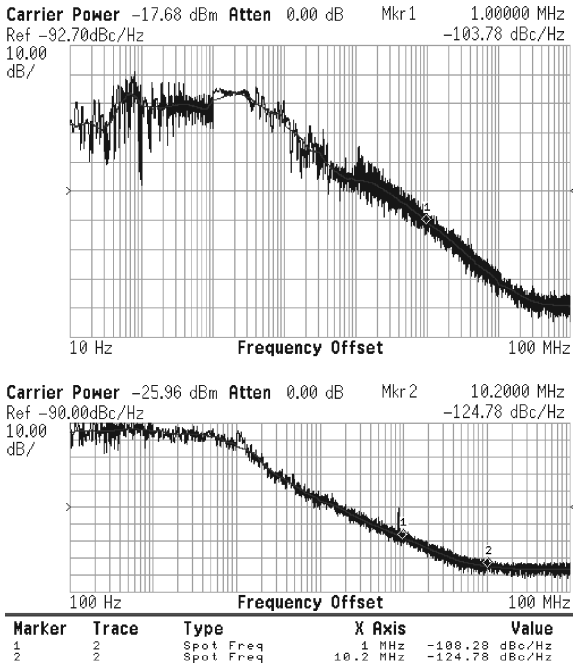

Fig. 8. Measured phase noise at the QVCO and divider output.

sured with open loop measurement in the phase-locked loop system. Figure 8 compares the phase noise at both the QVCO output and the quadrature-input divider output. As expected, the phase noise at the output of the proposed divider is about

6 dB lower than at the QVCO output at low offset frequency. The phase noise of the proposed divider at 1 MHz offset is 4 dB lower than that of the free running QVCO.

4. Conclusion

A harmonic-suppressed quadrature-input frequency divider has been presented. The proposed divider uses both input I/Q signals to achieve smaller and better-matched input loading to a previous stage circuit with smaller power consumption. The output I/Q phase sequence of the frequency divider tracks the input I/Q phase sequence and the output phase accuracy is independent of input phase accuracy. Moreover, the third harmonic is effectively suppressed. The quadrature-input divider achieves a harmonic rejection of 45 dB while dissipating 4.5 mA from a 1.2 V supply at an input frequency of 8.5 GHz.

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