A 3.4–3.6 GHz power amplifier in an InGaP/GaAs HBT*

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Abstract: This paper presents a 3.4–3.6 GHz power amplifier (PA) designed and implemented in InGaP/GaAs HBT technology. By optimizing the off-chip output matching network and designing an extra input-matching circuit on the PCB, several problems are resolved, such as resonant frequency point migration, worse matching and lower gain caused by parasitics inside and outside of the chip. Under $V_{cc} = 4.3$ V and $V_{bias} = 3.3$ V, a P_{1dB} of 27.1 dBm has been measured at 3.4 GHz with a PAE of 25.8%, the 2nd and 3rd harmonics are –64 dBc and –51 dBc, respectively. In addition, this PA shows a linear gain more than 28 dB with $S_{11} < -12.4$ dB and $S_{22} < -7.4$ dB in 3.4–3.6 GHz band.

Key words: 3.4–3.6 GHz; InGaP HBT; PA

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1. Introduction

As the next generation of wireless communication system technology matures, designs for commercial products that provide a higher data rate and wideband multimedia services have attracted a great deal of attention[1]. Frequency distribution has been a key problem and the frequency band of 3.4–3.6 GHz is one research hotspot[2].

The power amplifier (PA) is one of the key components in a wideband wireless transceiver system. This paper presents a 3.4–3.6 GHz PA designed and implemented in InGaP/GaAs HBT technology. The output matching network and RF chokes are implemented off-chip on the PCB. Due to the on-chip and off-chip parasitics, the resonant frequency point migration is occurred, along with worse matching and lower gain. The performance of this power amplifier is improved by optimizing the output match and designing an off-chip circuit to adjust the input match. Under $V_{cc} = 4.3$ V and $V_{bias} = 3.3$ V, the measured results obtained from this PA show a linear gain over 28 dB with $S_{11} < -12.4$ dB and $S_{22} < -7.4$ dB. At 3.4 GHz, this PA delivers a P_{1dB} of 27.1 dBm with a PAE of 25.8%, the 2nd and 3rd harmonics are –64 dBc and –51 dBc, respectively.

2. Circuit design

A three-stage cascade configuration is designed to achieve the desired output power and gain. The emitter area of single HBT is 80 μm^2, the total emitter areas of three stages are 160 μm^2, 640 μm^2 and 2560 μm^2, respectively. The chip area is 2×1 mm^2. The topology of the whole circuit is shown in Fig. 1. The power supply voltages are $V_{cc} = 4.3$ V and $V_{bias} = 3.3$ V, respectively. The driver stage is biased at class-A operation, while the gain and output stages operate as normal class-AB amplifiers to minimize power consumption while maintaining high linearity. The output matching network and RF chokes of three stages are implemented off-chip using high Q surface mount devices (SMD) on the PCB. The RC feedback circuits are used in the first and second stages to increase the stability and linearity of PA[3–5], moreover, base-ballasting resistors are used in all three stages to control current collapse[6–8], along with small coupling capacitors to suppress the gain of lower frequency band. Bonding wires are used to connect the chip and the PCB.

As we all know, one of the most challenging tasks in PA design is to determine the optimal loading resistance R_{opt}, which ensures that maximum output power can be achieved. In this circuit, the R_{opt} is obtained by using load pull simulation in ADS (Agilent) software and the output matching network is designed based on the R_{opt} accordingly. In addition, the input and inter-stage matching networks are completed by conjugate matching for maximum gain. The excellent simulated results are obtained after optimizing the circuit repeatedly, as shown in Fig. 2, the input and out match are satisfactory with a linear gain over 33 dB in the working frequency band and the P_{1dB} is more than 30 dBm at 3.4 GHz.

For PA implementation, the off-chip circuit on the PCB for output matching is crucial for performance realization of the PA. In this paper, an FR4 PCB is used and the PCB circuit is designed based on the simulation circuit completely. The preliminary S parameters are tested using a network analyzer and imported into ADS simulation software, as shown in Fig. 3, the resonant frequency point skew toward a higher frequency band in the input matching S_{11} and a high Q S_{22} curve with the resonant point 3.1 GHz is obtained. The linear gain S_{21} at 3.4 GHz is only about 20 dB because of the above mismatch and power loss. To achieve good matching, more important work to analyze and optimize the off-chip matching network should be performed.

3. Optimization of off-chip matching networks

3.1. Optimization of output matching network

The output matching circuit in simulation schematic is

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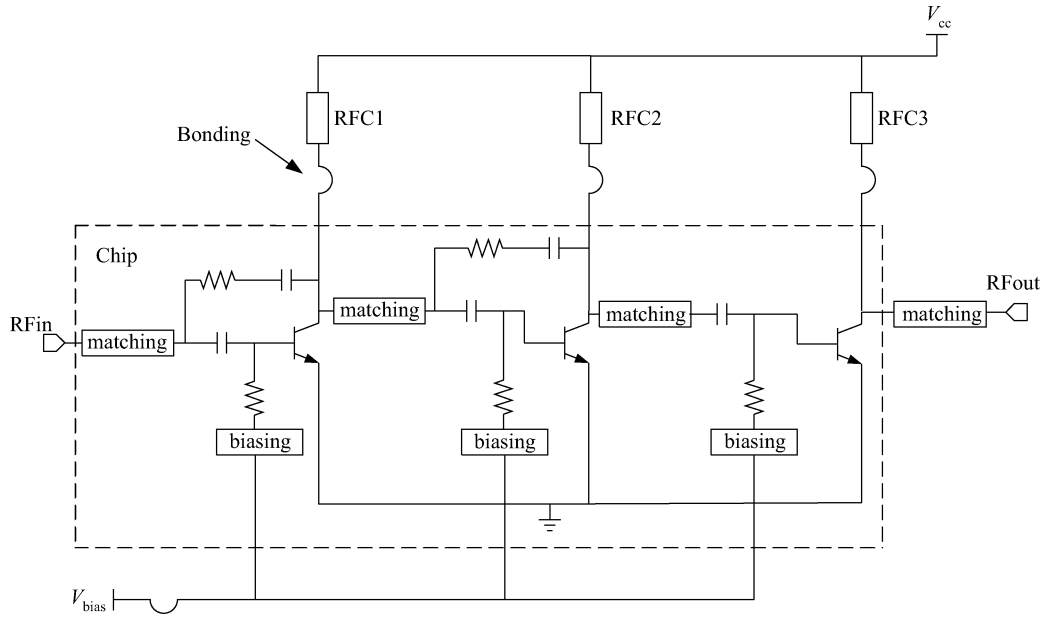

Fig. 1. Simplified schematic of a 3.4–3.6 GHz PA. On-chip components are surrounded by a dashed line.

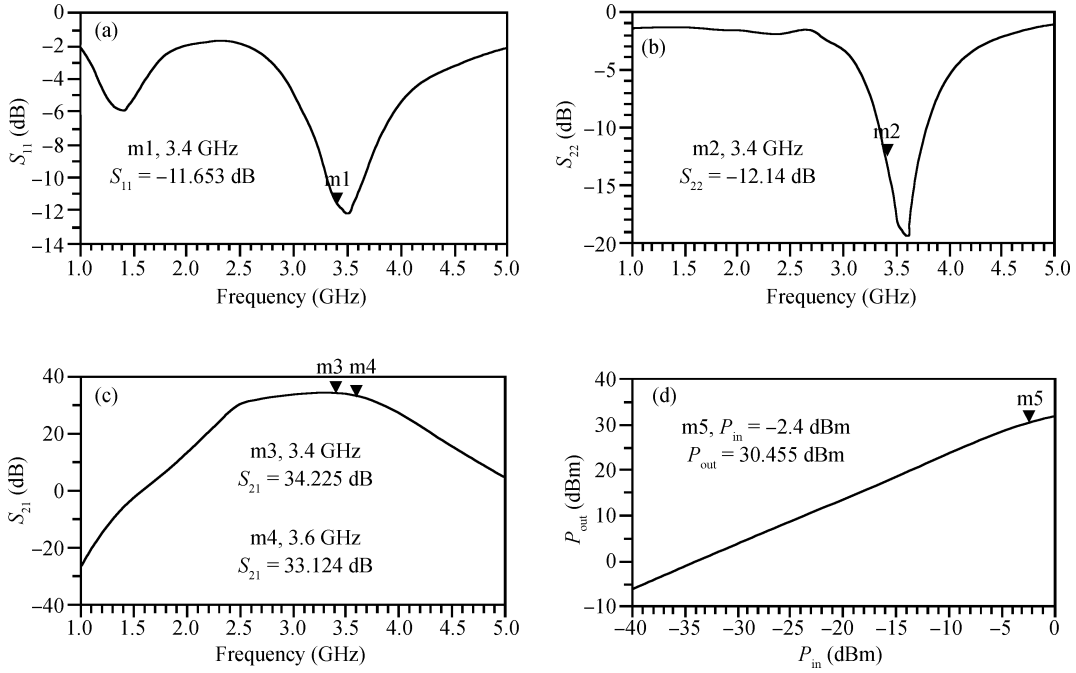

Fig. 2. Simulated results of the 3.4–3.6 GHz PA circuit. (a) S_{11}. (b) S_{22}. (c) S_{21}. (d) $P_{\text{out\_1dB}}$.

shown in Fig. 4, including microstrips named TL1–TL4, a coupling capacitor, a shunt capacitor and a LC parallel resonant circuit. The parallel resonant circuit involves C_3, L_1 and R_1 resonating in or near the working frequency band to adjust the gain flatness by designing the resonant point flexibly. The power loss can be ignored when R_1 is a large resistor.

As shown in Fig. 5(a), the parallel resonant circuit is analyzed. C_3 is ATC100A 1.8 pF and L_1 is 1 nH with the Muruta 0402 type and R_1 is 600 Ω. The attenuation of the signal power is the minimum at the parallel resonant frequency point where the impedance is the highest value as shown in Fig. 5(b). Therefore, the signal will be attenuated with the decreasing of the impedance away from the resonant point. In addition, the quality factor Q is very high in this circuit, however, the resonant point could skew easily in testing caused by parasitics, which is adverse for the circuit debugging. Therefore, the output matching network should be improved.

As shown in Fig. 6(a), the new output matching circuit is designed and optimized based on the test results, along with adjusting the bonding wires and RF chokes. The simulation results for the output matching is shown in Fig. 6(b), a gentle S_{22} curve is obtained.

3.2. Design of input matching circuit

An extra off-chip input matching circuit is designed to

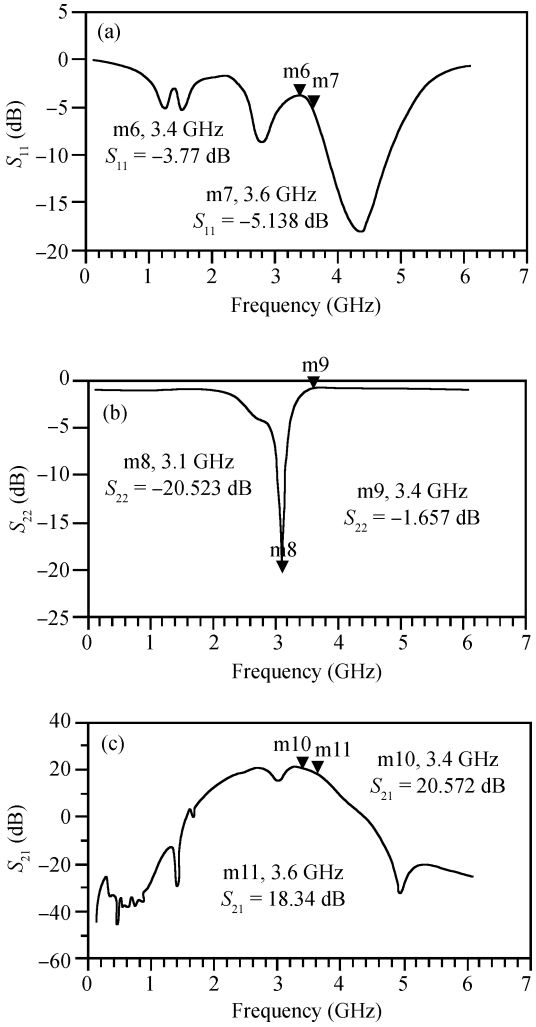

Fig. 3. Preliminary tested S parameter results. (a) S_{11}. (b) S_{22}. (c) S_{21}.

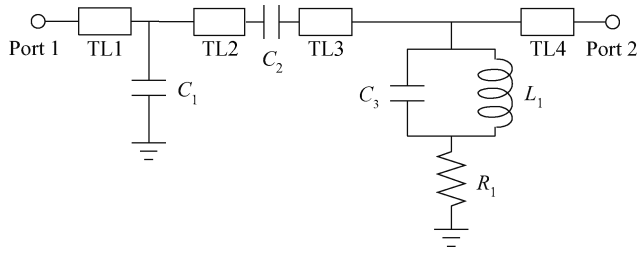

Fig. 4. Output matching network in simulation schematic.

adjust the resonant point back in the working frequency band, as shown in Fig. 7. Two circuit types are used and compared because the inductor L is lower than 1 nH. In the first circuit type, L is an SMD inductor and, in the second type, it is a bonding wire. However, two or three parallel SMD inductors should be soldered because the inductance is very small, which is not convenient in soldering and extra parasitics would be brought in this circuit. Thus, the second method is adopted and proved to be effective in adjusting the input match, and the number of bonding wires can be changed flexibly. As shown in Fig. 7(b), the inductor L can be replaced with 5 bonding wires based on the distance of microstrip TL2 and TL3 in this PCB circuit.

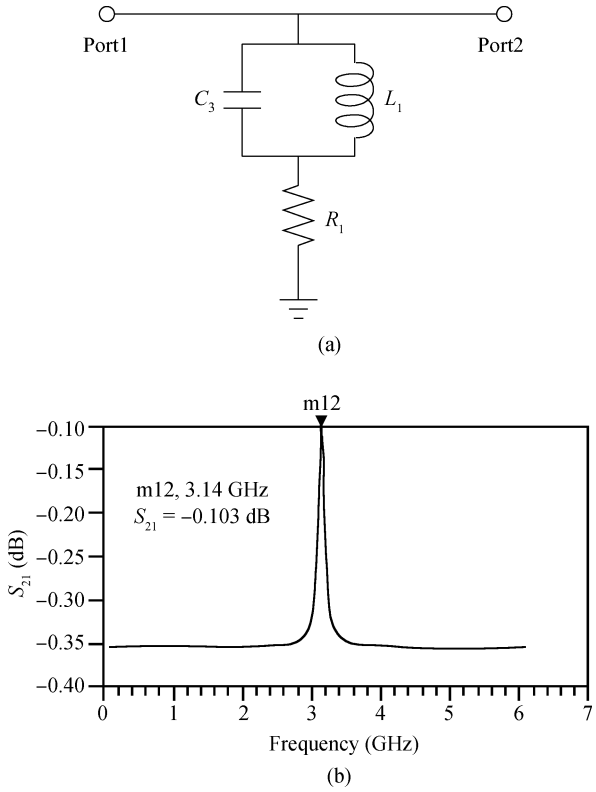

Fig. 5. Parallel resonant circuit of output matching network in the simulation schematic. (a) Parallel resonant circuit. (b) Transfer loss of this parallel resonant circuit.

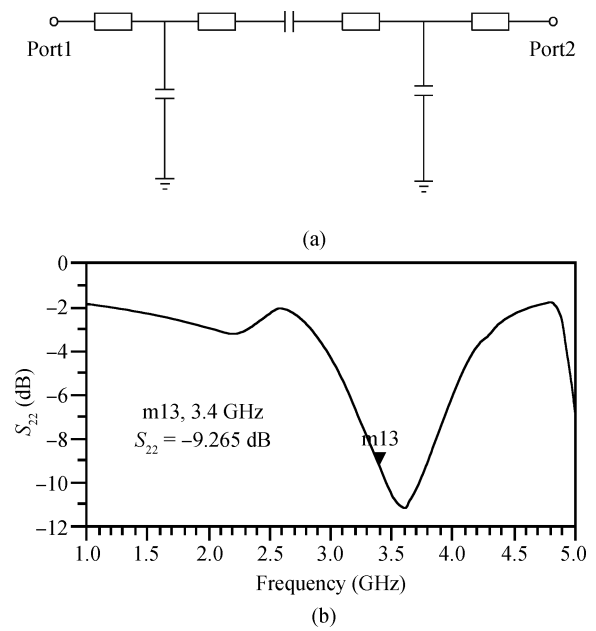

Fig. 6. (a) The improved output matching circuit. (b) The simulated S_{22}.

The simulation result of return loss S_{11} is obtained as shown in Fig. 8. The resonant point is moved to a lower frequency point outside of the working band. Back to Fig. 3(a), it could be estimated that a good input match will be obtained.

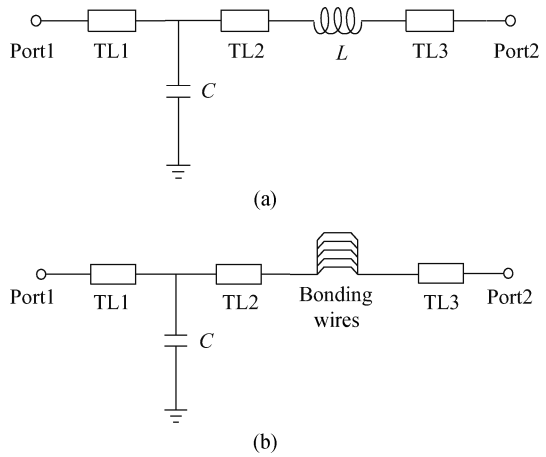

Fig. 7. Design of input off-chip matching circuit. (a) First circuit type. (b) Second circuit type.

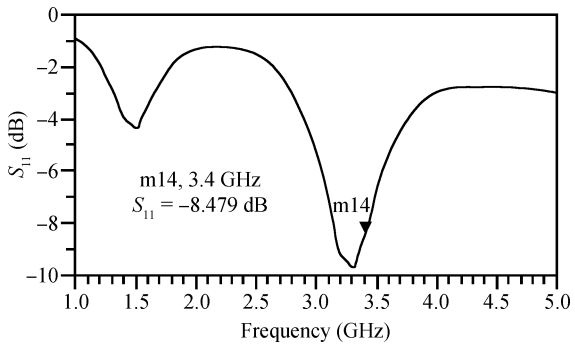

Fig. 8. Simulation of S_{11} after new input matching circuit used.

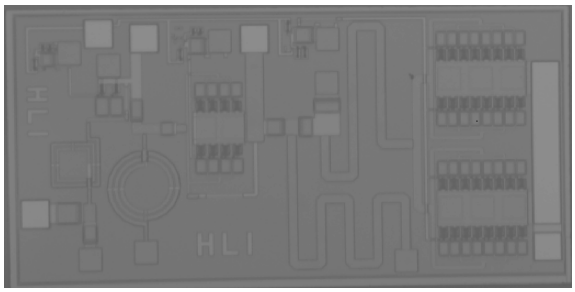

Fig. 9. Microphotograph of the implemented 3.4–3.6 GHz PA chip.

4. Measured results

Figure 9 presents a microphotograph of the 3.4–3.6 GHz PA with a chip size of 2 × 1 mm^2 including the bonding pads. The chip was directly mounted on the FR4 PCB. After optimizing the circuit on the PCB, the whole circuit of the test component is determined, as shown in Fig. 10. Multiple different capacitors are placed in every DC pach for filtering. Under V_{cc} = 4.3 V and V_{bias} = 3.3 V, the total quiescent current consumption is 155 mA. With an HP8720ES vector network analyzer, the linear gain is over 28 dB during the whole working band, the gain flatness is only ± 0.25 dB, S_{11} and S_{22} are below –12.4 dB and –7.4 dB, respectively, as shown in Fig. 11. Figure 12 shows that the measured output power at the –1 dB compression point is 27.1 dBm at 3.4 GHz corresponding input power 0 dBm. At the output power of 27.1 dBm, the PAE is 25.8% and the 2nd and 3rd harmonics are –64 dBc and –51 dBc, respectively. The results show that this PA has good linearity.

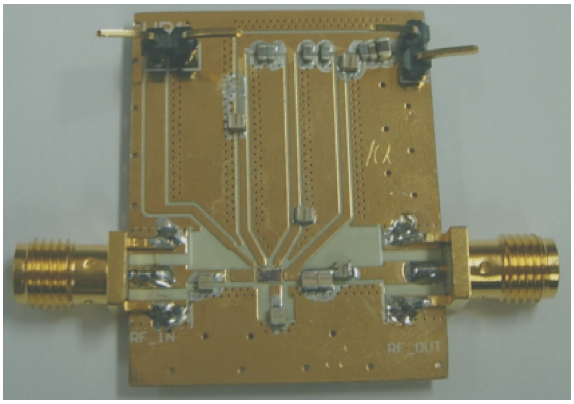

Fig. 10. Test component.

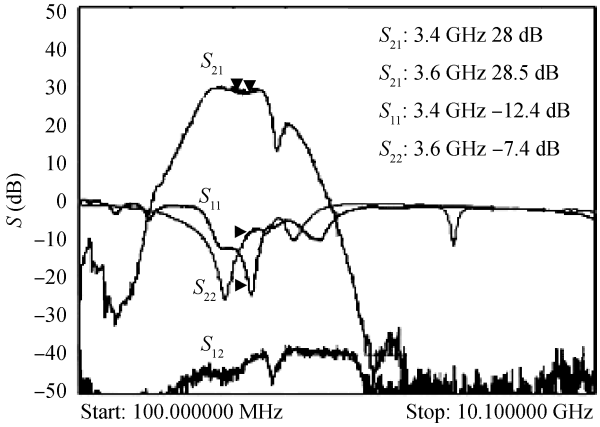

Fig. 11. Measured S parameters.

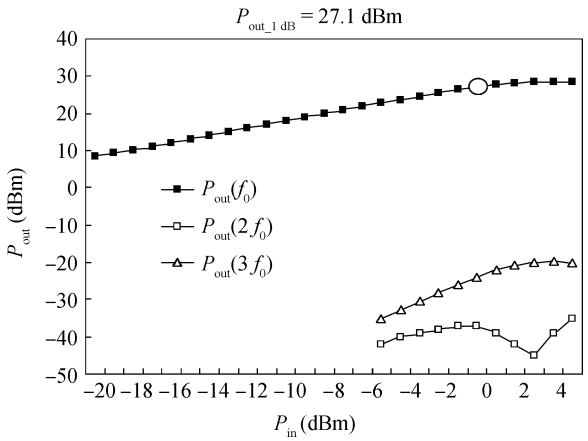

Fig. 12. Measured P_{out} at the –1 dB compression point.

5. Conclusion

A 3.4–3.6 GHz PA is designed and implemented in InGaP/GaAs HBT technology. The excellent matching is obtained by optimizing the output matching network and design-

ing an extra off-chip input matching network with bonding wires instead of SMD inductors on the PCB. Under $V_{cc} = 4.3$ V and $V_{bias} = 3.3$ V power supply, this PA shows a linear gain over 28dB during the whole working band with $S_{11} < -12.4$ dB and $S_{22} < -7.4$ dB, the output power at the –1 dB compression point is 27.1 dBm at 3.4 GHz with a PAE of 25.8%. The 2nd and 3rd harmonics are –64 dBc and –51 dBc, respectively, which means that the PA has good linearity.

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