Drive current of accumulation-mode p-channel SOI-based wrap-gated Fin-FETs*

Zhang Yanbo(张严波)[1,2], Du Yandong(杜彦东)[1], Xiong Ying(熊莹)[1], Yang Xiang(杨香)[1], Han Weihua(韩伟华)[1,†], and Yang Fuhua(杨富华)[1,3]

[1]Engineering Research Center for Semiconductor Integration Technology, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China
[2]Department of Electronic Engineering, Tsinghua University, Beijing 100084, China
[3]State Key Laboratory for Superlattices and Microstructures, Beijing 100083, China

Abstract: Comparisons are performed to study the drive current of accumulation-mode (AM) p-channel wrap-gated Fin-FETs. The drive current of the AM p-channel FET is 15%–26% larger than that of the inversion-mode (IM) p-channel FET with the same wrap-gated fin channel, because of the body current component in the AM FET, which becomes less dominative as the gate overdrive becomes larger. The drive currents of the AM p-channel wrap-gated Fin-FETs are 50% larger than those of the AM p-channel planar FETs, which arises from effective conducting surface broadening and volume accumulation in the AM wrap-gated Fin-FETs. The effective conducting surface broadening is due to wrap-gate-induced multi-surface conduction, while the volume accumulation, namely the majority carrier concentration anywhere in the fin cross section exceeding the fin doping density, is due to the coupling of electric fields from different parts of the wrap gate. Moreover, for AM p-channel wrap-gated Fin-FETs, the current in channel along ⟨110⟩ is larger than that in channel along ⟨100⟩, which arises from the surface mobility difference due to different transport directions and surface orientations. That is more obvious as the gate overdrive becomes larger, when the surface current component plays a more dominative role in the total current.

Key words: accumulation mode; inversion mode; wrap gate; Fin-FET; volume accumulation
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1. Introduction

Nowadays, the gate lengths of field effect transistors (FETs) have scaled down to tens of nanometers and are predicted to scale further in the future. One important issue of further scaling is the short channel effect (SCE), where the gate encounters competition with the drain in controlling the channel. Therefore, structural improvements are essential for the enhancement of FET performance. The wrap-gated Fin-FET has proven to be a promising candidate thanks to its excellent gate electrostatic control and thus good SCE immunity[1,2].

Another important issue of nano-FET scaling is doping profile adjustment in the channel region[3]. Controlling the overlap between the gate and the source/drain extension is a challenge for inversion-mode (IM) FETs. An alternative solution is to use an accumulation-mode (AM) FET, whose channel region is doped with the same type of dopant as the source/drain region. When the AM FET is turned off, the channel is fully depleted. When the AM FET is turned on, for a planar structure, carriers transport along both the surface accumulation layer and the neutral part of the body[4]; for a wrap-gated fin structure, however, the whole fin may be in accumulation (i.e. volume accumulation) thanks to the coupling of electric fields from different parts of the wrap gate, causing an obvious current enhancement because of the higher mobility in the fin center with reduced scattering[4], which still needs to be demonstrated.

In contrast with the planar channel, where carriers transport along one surface, carriers in the wrap-gated fin channel transport along the surfaces all around it. The surfaces may have different orientations, which results in mobility difference[5–7] and thus current difference. This may also happen to AM wrap-gated Fin-FETs and needs to be verified.

In this work, comparisons are performed to study the drive current of AM p-channel wrap-gated Fin-FETs. Firstly, with the same wrap-gated fin structure, AM p-channel FETs are compared with IM p-channel FETs in drive current to verify the body current component in the AM FETs. Secondly, AM p-channel wrap-gated Fin-FETs are compared with AM p-channel planar FETs to study the body current difference and the possible volume accumulation. Moreover, AM p-channel wrap-gated Fin-FETs with ⟨110⟩ channel are compared with those with ⟨100⟩ channel to check the current difference arising from different orientations of fin surfaces.

2. Device fabrication

AM p-channel wrap-gated Fin-FETs were fabricated on a boron-doped (1×10^{15} cm^{-3}), (110) oriented silicon-on-insulator (SOI) wafer with 88-nm-thick top silicon. First, e-beam lithography and inductively coupled plasma (ICP) etching were performed to define the active region and the channel fins, followed by a sacrificial oxidation (900 ℃, 30 min) to eliminate the surface damage induced by the etching. Dur-

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† Corresponding author. Email: weihua@semi.ac.cn
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Table 1. Structural and electrical parameters of IM/AM wrap-gated Fin-FETs and planar FETs.

Section	FET type	Fin width/ height (nm)	The number of fins in an FET	Gate length (μm)	Channel direction	V_T (V)	I_{on} (μA)
3.1	IM Fin-FET	90/60	11	0.3	⟨110⟩	−0.91	56.2
	AM Fin-FET	90/60	11	0.3	⟨110⟩	−0.69	64.6
3.2	AM planar FET	5000/60	1	0.3	⟨110⟩	−0.70	68.5
				0.5		−0.69	58.9
				1		−0.74	49.2
	AM Fin-FET	90/60	21	0.3	⟨110⟩	−0.67	102.6
				0.5		−0.75	93.6
				1		−0.75	78.5
3.3	AM Fin-FET	90/60	1	1	⟨110⟩	−0.68	9.8
	AM Fin-FET	90/60	1	1	⟨100⟩	−0.75	8.8

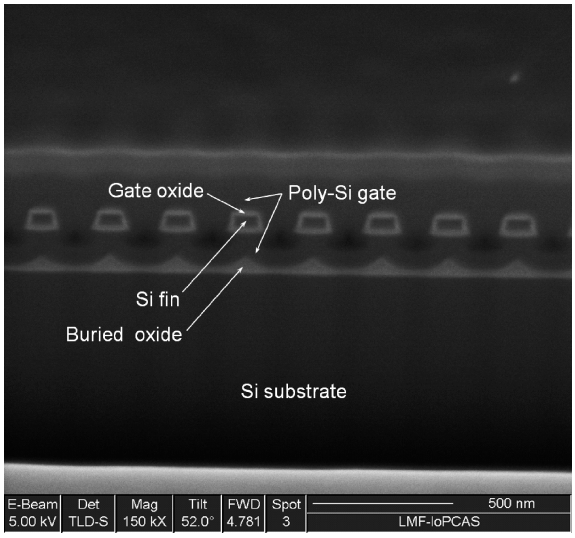

Fig. 1. Cross section SEM of a wrap-gated fin channel.

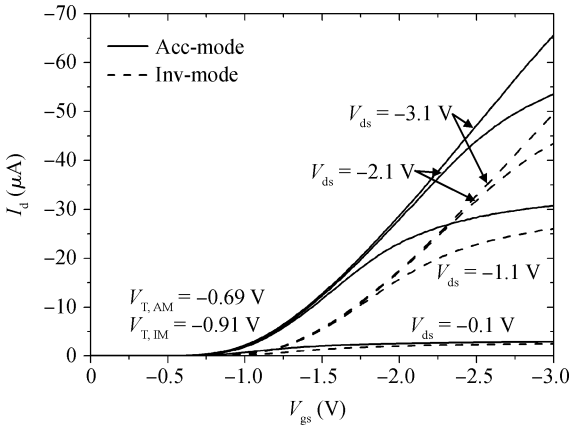

Fig. 2. Transfer characteristics of the AM and the IM p-channel wrap-gated Fin-FETs for 0.3-μm-long gate.

ing the following sacrificial oxide removal in the buffered hydrofluoric solution, an under-etching happened in the buried oxide, causing the silicon fins to be suspended. Then, a 30-nm-thick gate oxide was grown in dry oxygen at 900 ℃, and 150-nm-thick boron-doped polysilicon was deposited by low-pressure chemical vapor deposition (LPCVD), wrapping the fins with the conformal coverage. The polysilicon gate was defined by a round of second e-beam lithography and ICP etching. Source/drain doping was carried out by self-aligned BF_2^+ implantation and rapid annealing at 1050 ℃. After depositing 200-nm-thick silicon dioxide as the protective layer, contact holes were opened using optical lithography and ICP etching. Following 20-nm-thick nickel film evaporation, the ohmic contact layer i.e. nickel silicide (NiSi) was formed by alloy at 500 ℃. The unreacted nickel was removed by a selective etching solution ($H_2SO_4 : H_2O_2 = 3 : 1$) at 80 ℃ without attacking the silicide. To form the electrode pads of source/drain and gate, optical lithography was used to define the pattern in the photoresist and 400-nm-thick aluminum was evaporated and lifted off. The device fabrication process was finished with a 400 ℃ annealing process. Figure 1 shows the cross section of the wrap-gated fin channel. The width and height of the fin are 90 nm and 60 nm, respectively.

For comparison, AM p-channel planar FETs with the same width of active region ($W = 5$ μm) as the AM p-channel wrap-gated Fin-FETs were fabricated on the same SOI wafer. IM p-channel wrap-gated Fin-FETs were fabricated using the same process as the AM p-channel ones except for an additional n-well doping process (1×10^{17} cm^{-3}) before the channel fin definition.

3. Results and discussion

Structural and electrical parameters of the devices are shown in Table 1, where V_T is the threshold voltage extracted using second-derivative method[8] and I_{on} is the drain current when the drain bias (V_{ds}) is –3 V and the gate overdrive ($V_{gs} - V_T$) is –2.3 V. The results will be discussed by comparison in three aspects.

3.1. Accumulation-mode versus inversion-mode

Figure 2 shows transfer curves of the AM and the IM p-channel FETs with the same wrap-gated fin channel along ⟨110⟩. The V_T difference between the AM and the IM FET results from the difference in doping type and density in the channel region. The AM FET is compared with the IM FET in drive current under the same gate overdrive, as shown in Fig. 3. The current of the AM FET is 15%–26% larger than that of the IM FET, and the percentage gets smaller as the gate overdrive increases, indicating that the factor causing the larger current in the AM FET becomes less dominative. The factor is the body

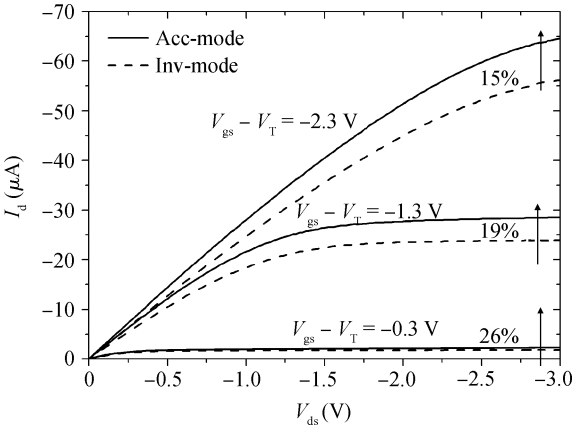

Fig. 3. Output characteristics of the same AM and IM p-channel wrap-gated Fin-FETs in Fig. 2.

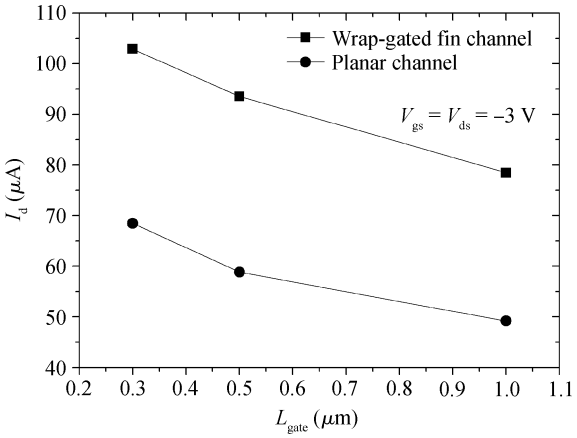

Fig. 4. Drive currents of AM p-channel wrap-gated Fin-FETs and AM p-channel planar FETs for different gate lengths.

current in the AM FET, an additional current component compared with the IM FET. As the gate overdrive increases, more holes are accumulated at the surfaces, which increases the surface current, but screens the body from the gate electric field and thus limits the body hole increasing. So the body current percentage decreases with gate overdrive increasing, making the current difference between the AM FET and the IM FET smaller.

3.2. Wrap-gated fin channel versus planar channel

With the same width of active region ($W = 5$ μm) and fabricated through the same process, AM p-channel wrap-gated Fin-FETs and AM p-channel planar FETs are compared in drive current for different gate lengths. All the AM p-channel FETs here have channels along ⟨110⟩ and have threshold voltages (V_T) around -0.7 V. As shown in Fig. 4, the drive currents of the AM p-channel wrap-gated Fin-FETs are about 50% larger than those of the AM p-channel planar FETs, which indicate a drive current improvement induced by the wrap-gated fin structure.

The current improvement arises from two aspects. First, in contrast with the planar channel with only one conducting surface, the wrap-gated fin has an additional bottom surface

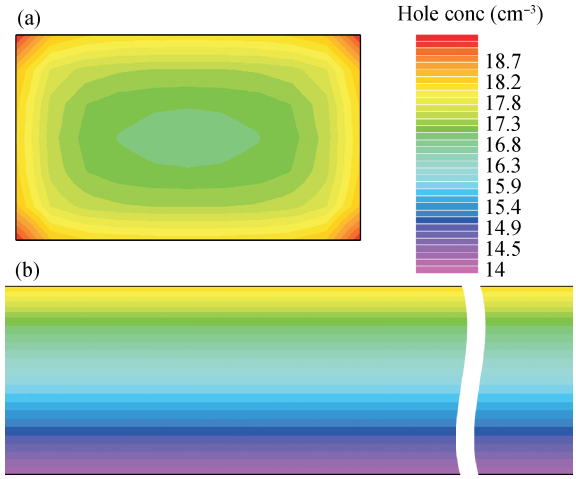

Fig. 5. Simulated hole distribution over the cross section in the middle point of (a) the fin channel and (b) the planar channel, with both the gate and the drain biased at -3 V.

and side surfaces that broaden the effective conducting surface. In our case, neglecting the hole mobility difference on different surfaces, which will not affect the final conclusion because of the largest hole mobility in ⟨110⟩ direction on {110} surface[5−7], the effective width of the conducting surface in the AM planar FETs is 5 μm, while that in the AM wrap-gated Fin-FETs is 6.3 μm. So the effective conducting surface is broadened by 26%.

Obviously, the effective conduction surface broadening is not enough to cause the 50% current difference between the wrap-gated fin channel and the planar channel. Therefore, the body current difference plays another important role, namely, the body current in the wrap-gated fin channel is larger than that in the planar channel. Whereas, owing to the spaces between adjacent fins, the physical cross section of the wrap-gated fin channel is smaller than that of the planar channel. In addition, because the holes in the fin body are closer to the side surfaces than the holes in the body of planar structure, they are more likely to be affected by the surface charge scattering, although this scattering effect is very small due to the surface holes' screening. So the body mobility in the fin channel will not exceed that in the planar channel and the only factor resulting in the body current difference is the body hole concentration, which in the wrap-gated fin channel is larger than that in the planar channel.

To understand that point, the hole distribution over the cross section in the middle point of the channel was simulated using an ATLAS 3D device simulator[9], on which the linear iterative method was used to solve the combination of Poisson's equation, drift-diffusion equations including Lombardi's mobility model[10], and carrier continuity equations including Shockley's carrier generation-recombination model[11]. The structural parameters were set to be 60 nm in channel thickness, 90 nm in fin width, 5 μm in planar channel width, 0.5 μm in gate length and 30 nm in gate oxide thickness. The doping density of the channel region was 1×10^{15} cm^{-3} and the interface charge density was set to be consistent with the threshold voltage ($V_T = -0.7$ V). Both the gate bias and the drain bias were set to be -3 V. As shown in Fig. 5, for the AM planar

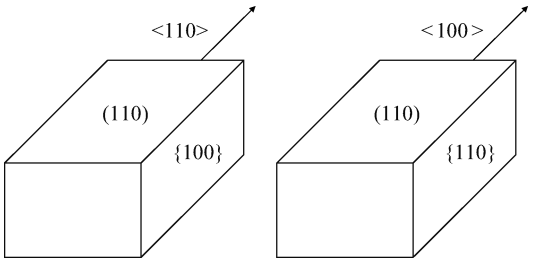

Fig. 6. Schematic of surface orientations of fins along different directions.

channel the hole concentration gets minimum at the bottom interface, and the minimum concentration is less than the doping density (1×10^{15} cm^{-3}) owing to the depletion effect of the interface charge, while for the AM wrap-gated fin channel the hole concentration reaches a minimum in the center of the fin cross section and the minimum concentration is two orders of magnitude greater than the fin doping density, which is due to the coupling of electric fields from different parts of the wrap gate. Therefore, hole accumulation occurs all over the cross section of the wrap-gated fin, in other words volume accumulation occurs, which we think is another reason why the drive currents of the AM p-channel wrap-gated Fin-FETs are larger than those of the AM p-channel planar FETs.

3.3. Considering the different surface orientations of the fin

To check the effect of surface orientation on the drive current of AM p-channel wrap-gated Fin-FETs, fin channels along different directions, ⟨110⟩ and ⟨100⟩, are designed on the same wafer, which result in {100} and {110} side surfaces, respectively, after the fins are etched out, as shown schematically in Fig. 6. Considering different the mobility on surfaces of different orientations, the current in a wrap-gated fin is given by

$$I = I_{\text{body}} + \sum_j \frac{W_j}{2L_{\text{eff}}} \mu_{\text{S},\,j} C_{\text{OX},\,j} \left(V_{\text{gs}} - V_{\text{T}}\right)^2,$$

where I_{body} is the body current, W_j, $\mu_{\text{S},\,j}$, $C_{\text{OX},\,j}$ are the width, the mobility and the gate oxide capacitance per unit area respectively of the jth surface, and L_{eff}, V_{gs}, V_{T} are the effective channel length, gate bias and threshold voltage respectively. In our case, because of the same gate oxide thickness and thus the same $C_{\text{OX},\,j}$, the current along different surfaces is proportional to $W_j \mu_{\text{S},\,j}$. It has been reported that the ratio of hole mobility along different surfaces and transport directions is $\mu_{\langle 110\rangle/(110)} : \mu_{\langle 100\rangle/(110)} : \mu_{\langle 110\rangle/(100)} = 2.5 : 1.6 : 1$[5−7]. Accordingly, the ratio of surface current is evaluated as shown in Table 2.

Figure 7 shows the output characteristics of two AM p-channel wrap-gated Fin-FETs with different channel directions, ⟨110⟩ and ⟨100⟩. Owing to the body current component, the total drain current difference between these two directions is less than 19%, i.e. the surface current difference in Table 2. As the gate overdrive gets larger, the surface current component plays a more dominative role in the total current and thus the surface mobility difference appears more obviously in the total current.

Table 2. Evaluation of the ratio of surface current along ⟨110⟩ to that along ⟨100⟩.

Current direction	Surface orientation	Surface mobility ratio	Surface width (nm)	Surface current ratio
⟨110⟩	{110}	2.5	180	1.19
	{100}	1	120	
⟨100⟩	{110}	1.6	300	1

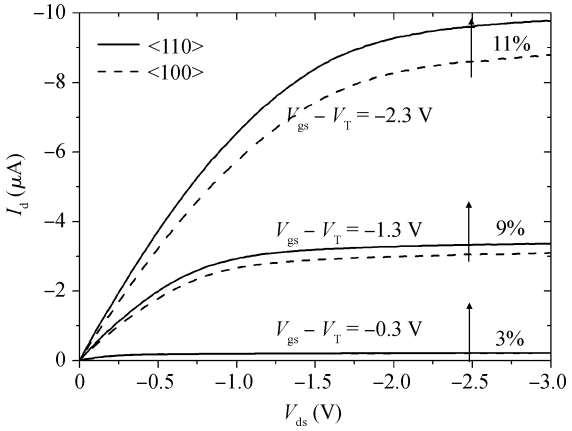

Fig. 7. Output characteristics of AM p-channel wrap-gated Fin-FETs with channel along ⟨110⟩ and ⟨100⟩.

4. Conclusion

Comparisons are performed to study the drive current of AM p-channel wrap-gated Fin-FETs. The drive current of the AM p-channel FET is 15%–26% larger than that of the IM p-channel FET with the same wrap-gated fin channel, due to the body current component in the AM FET, which becomes less dominative as the gate overdrive increases. The drive currents of the AM p-channel wrap-gated Fin-FETs are 50% larger than those of the AM p-channel planar FETs, which arises from effective conduction surface broadening and volume accumulation. Moreover, for the AM p-channel wrap-gated Fin-FETs, the current in the channel along ⟨110⟩ is larger than that in the channel along ⟨100⟩, which arises from the surface mobility difference due to different transport directions and surface orientations. That is more obvious as the gate overdrive gets larger, when the surface current component plays a more dominative role in the total current.

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