An RF front-end with an automatic gain control technique for a U/V band CMMB receiver

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Abstract: This paper presents a fully integrated RF front-end with an automatic gain control (AGC) scheme and a digitally controlled radio frequency varied gain amplifier (RFVGA) for a U/V band China Mobile Multimedia Broadcasting (CMMB) direct conversion receiver. The RFVGA provides a gain range of 50 dB with a 1.6 dB step. The adopted AGC strategy could improve immunity to adjacent channel signal, which is of importance for CMMB application. The front-end, composed of a low noise amplifier (LNA), an RFVGA, a mixer and AGC, achieves an input referred 3rd order intercept point (IIP3) of 4.9 dBm with the LNA in low gain mode and the RFVGA in medium gain mode, and a less than 4 dB double side band noise figure with both the LNA and the RFVGA in high gain mode. The proposed RF front-end is fabricated in a 0.35 μm SiGe BiCMOS technology and consumes 25.6 mA from a 3.0 V power supply.

Key words: CMMB; RF front-end; RFVGA; AGC; LNA; mixer
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1. Introduction

Mobile TV is getting gaining popularity all over the world. At present there are already several handheld TV standards, which include Terrestrial Digital Media Broadcasting (T-DMB) in Korea, MediaFLO (developed by Qualcomm) and Digital Video Broadcast for Handheld (DVB-H, proposed by the DVB organization in Europe). On the China mainland, the mobile TV standard is China Mobile Multimedia Broadcasting, which is backed by the State Administration of Radio, Film and Television (SARFT). CMMB is a mixed satellite and terrestrial wireless broadcasting system designed for providing audio, video and data services for handheld receivers. The satellite network (S band) covers the whole mainland and the terrestrial network (U/V band) provides terrestrial coverage, which is used in dense urban areas to improve system performance. According to CMMB specifications, a U/V band RF tuner for the terrestrial network should be capable of handling broadband signals ranging from 168 to 248 MHz and 470 to 862 MHz, respectively. Moreover, the tuner is required to handle input power levels ranging from –95 to –10 dBm, which means the tuner must have large gain dynamic range. High sensitivity and linearity are also strongly expected, for which the tuner must have small NF when handling a small signal and a large IIP3 when performing at low gain mode. Additionally, the tuner is expected to dissipate as little power as possible to extend the lifetime of battery operated handheld devices.

For CMMB, whose RF bandwidth is 8MHz and baseband bandwidth 4MHz, another key issue is adjacent channel rejection (ACR). The specifications of 37 dB N–1/N+1 digital ACR along with more than 40 dB N–1/N+1 analog ACR[1] call for a front-end with high linearity and high immunity to adjacent channel interference. For example, when a small desired channel signal together with a large undesired adjacent channel signal is inputted to the receiver, the front-end must amplify the desired signal while keeping the undesired adjacent channel signal from saturating the elements. For U-band (470–862 MHz), except for an adjacent signal, the GSM (880–915 MHz and 925–960 MHz) is unfortunately another interruption source. To meet the ACR and anti-interruption requirements, the proposed front-end adopts a new AGC strategy to provide high linearity and high immunity to adjacent channel interference.

Figure 1 shows the block diagram of the front-end for the CMMB receiver and the elements emphasized in the dashed box are presented in this paper. The front-end is composed of an LNA, an RFVGA, a quadrature mixer and an AGC. The U/V LNAs have two gain modes, a low voltage gain of –5 dB and a high gain of 20 dB, and the RFVGA has a voltage gain varying from –24 to 24 dB with a 1.6 dB step. The U/V LNAs amplify RF input signals and send them to a digitally controlled RFVGA, which is followed by quadrature mixers. The AGC detects the output signal strengths at the RFVGA, mixer and filter outputs, and produces gain control signals for the LNA

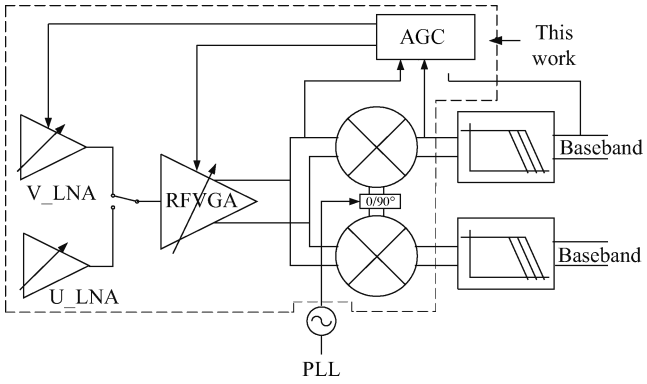

Fig. 1. Block diagram of the front-end.

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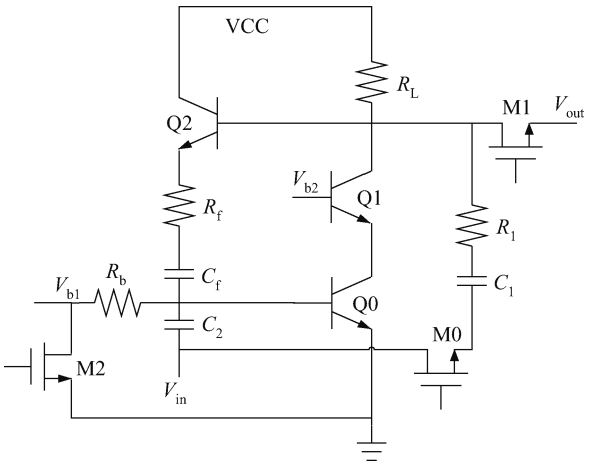

Fig. 2. LNA schematic diagram.

and the RFVGA.

This paper focuses on the design and implementation of each block of the front-end, and provides simulated and measured results.

2. Design and implementation of the circuit

As mentioned above, the zero-IF receiver front-end is composed of a single-ended LNA with two gain modes, a digitally controlled RFVGA, double balanced mixers and an AGC circuit.

2.1. U/V LNA

The LNAs optimized for U-band and V-band are implemented with similar architectures. As seen in Fig. 2, the single-ended LNA is ac coupled with the input and loaded by resistor R_L. M0 and M2 are used to select high or low gain mode. The cascode architecture Q0 and Q1 works in high gain mode, which achieves a voltage gain of 20 dB, IIP3 –12 dBm and NFdsb 2 dB. The shunting feed back architecture of Q2, C_f and R_f is used to broaden the bandwidth of the LNA. R_1 and C_1 compose the low gain signal chain, which achieves a voltage gain of –5 dB, IIP3 15 dBm and NFdsb 9 dB. M2 and M0 are used to select high gain or low gain mode and M1 switches on or off when the LNA is selected or not.

2.2. Digitally controlled RFVGA

As shown in Fig. 3, the RFVGA is composed of four identical G_m cells and a group of NMOSFETs to steer different signal currents to the loads[2]. The capacitors preceding the G_m cells attenuate the input voltage differently so the voltage gain at the input of the four G_m cells varies from 0 to –38.4 dB with a step gain 12.8 dB, which is called coarse tuning. The group of NFETs steer different signal currents to the loads and this technique is called fine tuning.

The NFET group includes the positive output group, which consists of Ma0, Ma1 to Ma7 and Mb1 to Mb7, and the negative output group, which consists of Md0, Mc1 to Mc7 and Md1 to Md7. The positive output group is analyzed only for simplicity. After voltage-to-current conversion, which is performed by G_m, the current signal is split into two paths: one is the main signal path, containing Ma0, Ma1 to Ma7, and the other is a dumping path, containing Mb1 to Mb7. Ma0 is a remaining transistor that is always activated. The transistor Mbx is the mirror of Max and has the reverse gate voltage to Max. The gate voltage of Ma and Mb is lower than the supply voltage, which is beneficial to improve linearity. Every time the voltage gain is enlarged by 1.6 dB a more Ma transistor is turned on, at the same time a corresponding Mb transistor is turned off. To save die area, from the minimum gain to maximum gain, all the transistors of Ma and Mb are reused. To obtain the gain step of 1.6dB, the dimension of the m-th transistor, Mam or Mbm, is designed based on the following equation,

$$20\lg\left[\sum_{n=0}^{m}\left(\frac{W}{L}\right)_n \Big/ \sum_{n=0}^{m-1}\left(\frac{W}{L}\right)_n\right] = 1.6\,\text{dB},$$
$$m = 1, 2, 3, 4, 5, 6, 7. \quad (1)$$

Once the dimension of Ma0 is specified, the dimensions of the other transistors are also specified. Namely, the larger the current intensity directed to the voltage supply directly, the more attenuated the VGA gain is, and the fine tuning can be called a current splitting technique.

Capacitors C_1 to C_4 preceding G_{m1} to G_{m4} are used to attenuate the input signal before the voltage signal is injected into the four G_m cells to provide coarse gain programmability while maintaining good noise performances. The capacitor C_1 preceding G_{m1} is as large as possible in order to obtain a voltage gain of 0 dB and the capacitors preceding G_{m2}, G_{m3} and G_{m4} are designed smaller than C_1 to attenuate input signal. The coarse tuning is achieved by switching only one of the four G_m cells on while the other three G_m cells are turned off.

In order to control gain digitally, 4 bits are assigned to select one of the four G_m cells to be switched on for coarse gain tuning. Another 7 bits are needed to control the gate voltage of cascade transistors, Ma, Mb, Mc and Md for fine gain tuning. Gain tuning leads to a linear-in-decibel with a 1.6 dB step while achieving the gain tuning range of 51.2 dB.

2.3. Double balanced mixer

As shown in Fig. 4, two Gillbert cells with shared transconductance stages compose the double balanced mixer[3, 4]. The degeneration resistor R_{tail} is placed as the tail current source to improve the linearity of the mixer. LOIp, LOIn, LOQp and LOQn are amplified by an LO-buffer before controlling the base voltage of quadrature transistors Q3–Q10. The LO signals are turned on in the order: LOQp, LOIp, LOQn, LOIn. For example, when the RF signal on Q1 is high and the LOQp signal on Q7 is high, the voltage of the collector terminal of Q1 is pulled high and transistors Q3, Q4 and Q8 are shut off. In this way the total available current must flow through only a selected transistor according to the local signal sequence. The mechanism is called Q–I mutual interference and is useful for phase error suppression[5]. The load resistor R_L is connected to C_L in parallel. The 3 dB bandwidth of R_L and C_L is about 150 MHz so that RF and LO frequency and their harmonics can be filtered out to a certain extent.

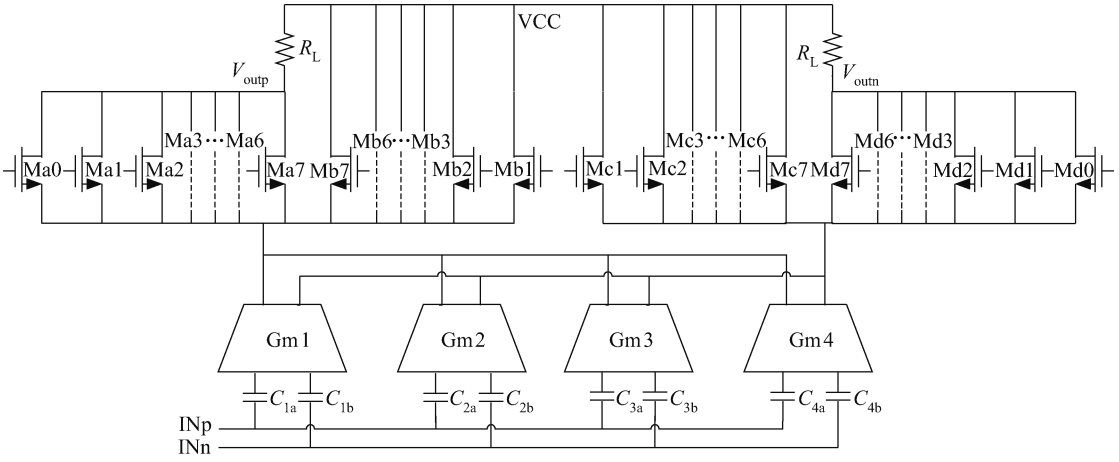

Fig. 3. RFVGA schematic diagram.

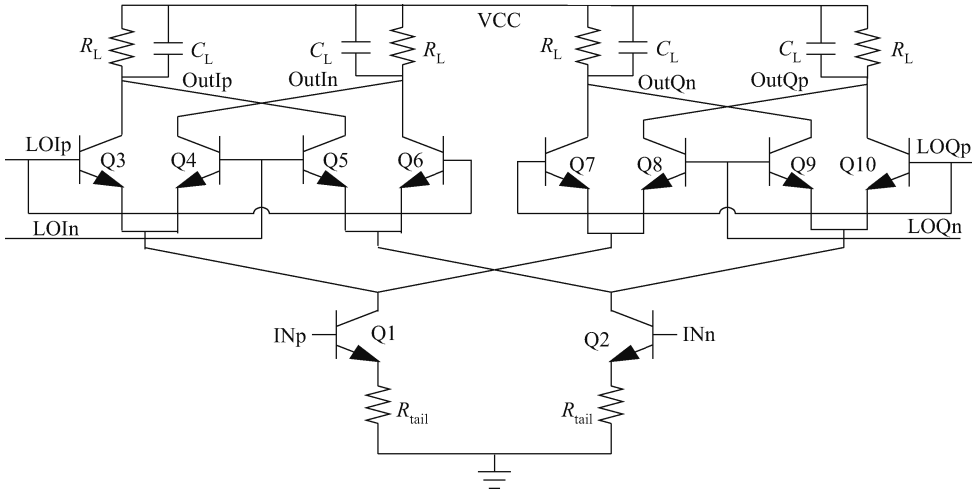

Fig. 4. Quadrature mixer schematic diagram.

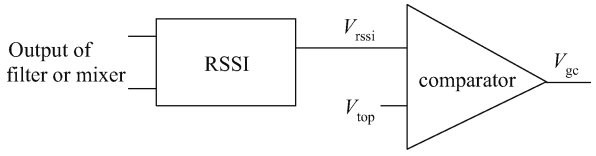

Fig. 5. Schematic of conventional AGC.

2.4. AGC strategy

For an RF front-end applied in CMMB which works in V-band (168–248 MHz) and U-band (470–862 MHz), one of the main challenges is ACR. In a conventional AGC receiver strategy, as shown in Fig. 5, a RSSI detects the output signal of the filter or mixer and produces a voltage of V_{rssi}, which is compared with the voltage V_{top}. The comparator produces the V_{gc} to control the gain of RFVGA, which is continuously tuned. V_{top} defines the received signal strength at the filter or mixer output through the AGC loop. In such a receiver, when a small desired channel signal together with a large adjacent channel signal (ACS) is received, if the RSSI is used to detect the output signal strength of filter, the AGC system is blind to the ACS and the RFVGA will be controlled by the AGC to work in high gain mode to amplify the desired signal and undesired ACS. The large ACS will saturate the front-end elements, LNA, RFVGA and mixer. Moreover, if the ACR is large enough, the elements of the base-band, filter and BBVGA, will get saturated, too. If the RSSI is used to detect the output signal strength of mixer, the conventional AGC strategy treats the desired channel signal and the ACS indistinguishably and makes RFVGA work in low gain mode, in which case the desired signal can not get amplified enough and the required SNR for demodulating can not be obtained.

In this paper another AGC strategy is employed to deal with the above mentioned situation. The architecture of the proposed AGC is showed in Fig. 6. A power detector (PDET) is used to indicate the radio frequency power of output of the RFVGA and at the same time two RSSI, RSSI1 and RSSI2 are used to indicate the signal strength of the mixer and filter outputs, respectively. The output voltage of the PDET is compared with two threshold voltages, V_{TH1} and V_{TL1}, where V_{TH1} is larger than V_{TL1}, and two bits are produced by the comparator CMP1. The RSSI1 output is compared with V_{TH2} and V_{TL2}, and the output of RSSI2 is compared with V_{TH3} and V_{TL3}. The gain control logic makes use of the outputs of three comparators and

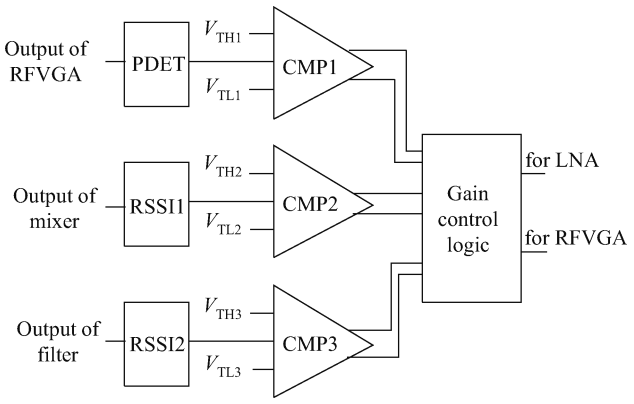

Fig. 6. Schematic of the presented AGC.

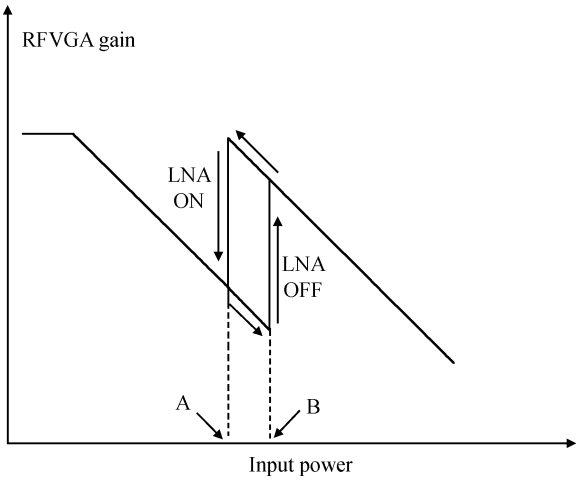

Fig. 7. Gain of the RFVGA with input power.

produces the voltages to control the gain of LNA and RFVGA. When one or more of the three outputs of PDET, RSSI1 and RSSI2 is higher than their corresponding high threshold voltage V_{TH}, the gain control logic reduces the voltage gain of front-end through controlling the voltage gain of the LNA and RFVGA. In addition, in the case where all the outputs of the PDET, RSSI1 and RSSI2 are lower than their corresponding low threshold voltage V_{TL}, the gain control logic enhances the voltage gain of front-end. In this AGC strategy, carefully selecting the values of V_{TH} and V_{TL} is crucial.

In the AGC strategy, another crucial issue is how to tune the gain of RFVGA and LNA when receiving a signal with time varied power. The gain of an ideal continuously tuned RFVGA and LNA is expected to vary with the input power, as shown in Fig. 7. As the RF input level increases or decreases, the gain of the RFVGA decreases or increases. In the middle of the RFVGA operation range, the LNA ON/OFF operation occurs and this operation expands the dynamic range of the front-end. The reason for the LNA ON/OFF hysteresis region is to avoid the LNA toggling action caused by a small noise signal, which is likely to happen if the LNA ON/OFF level is the same. The voltage gain measurement result of presented RFVGA varying with the input signal level is shown in part 3.

There are some other solutions to achieve the compromise of the SNR and normal operation of the receiver. For example,

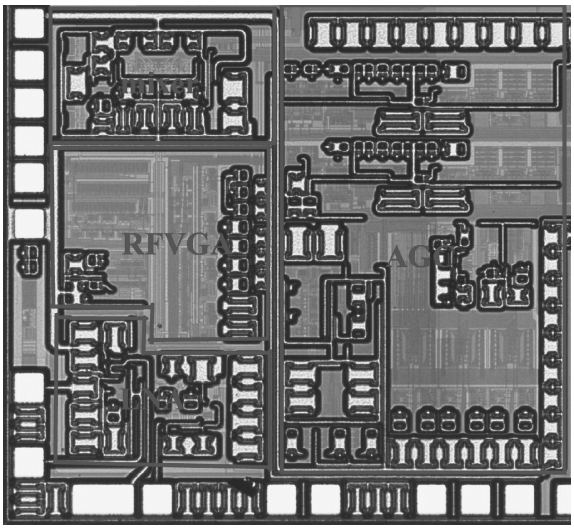

Fig. 8. Micrograph of front-end.

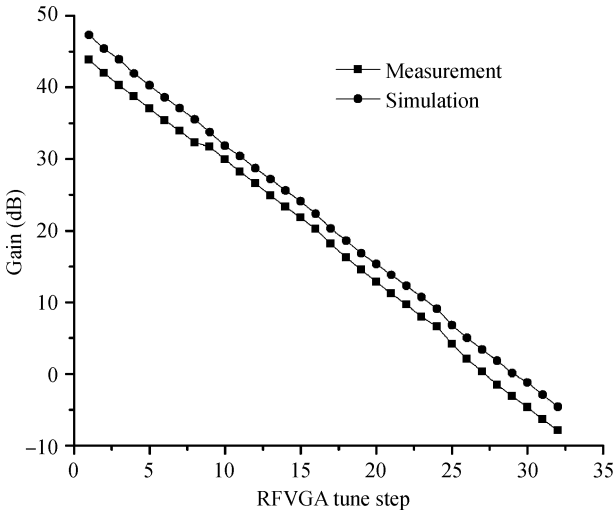

Fig. 9. Result of front-end gain tuning.

increasing the power supply voltage of receiver to improve the dynamic range of front-end could make the receiver perform normally when a small desired channel signal with an undesired channel signal is inputted to it. Additionally, a base-band low pass filter with larger stop-band attenuation could attenuate the adjacent channel signal more and prevent the base-band circuit from being saturated. However, the above mentioned two solutions cause the receiver to dissipate more power which is undesirable for portable devices. For this reason, in this paper those two solutions are not adopted.

3. Measurement result

The micrograph of the front-end, which occupies an area of 1.1×1.2 mm^2, is shown in Fig. 8.

Figure 9 shows the voltage gain of the front-end working in radio frequency of 472 MHz. The measurement result deviates about 3 dB from the simulation result but has the same shape as the simulation result. As mentioned above in Section 2 and shown in Fig. 9, the voltage gain of the front-end is linear-in-

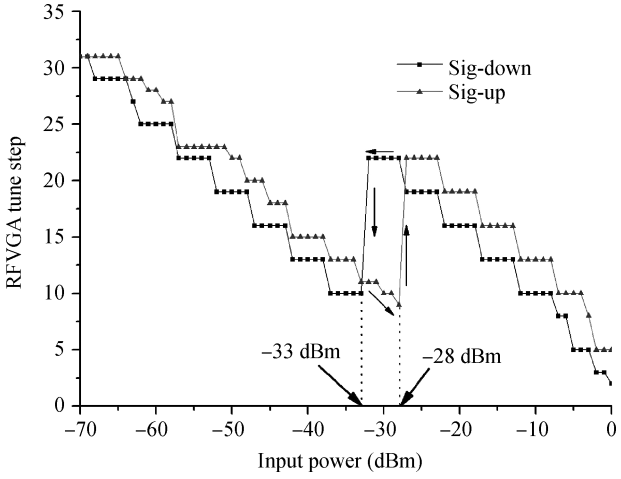

Fig. 10. Measurement result of voltage gain of the RFVGA varying with input level.

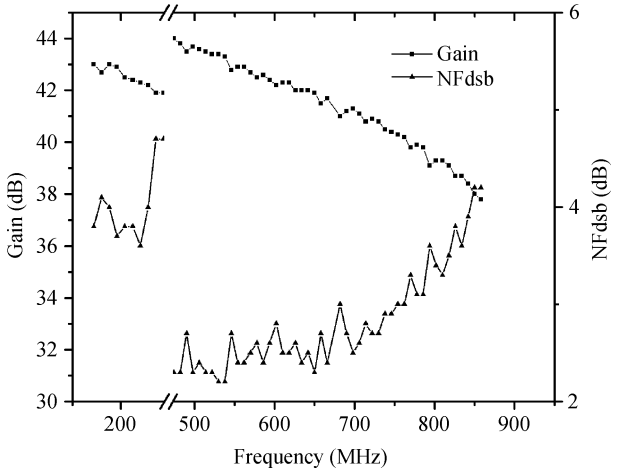

Fig. 11. Measurement result of the NF and gain.

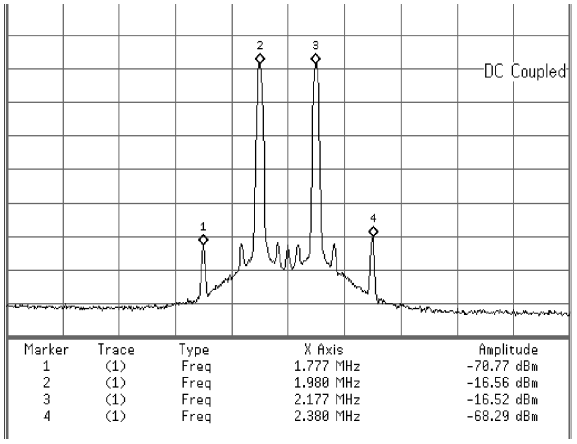

Fig. 12. Result of two-tone testing.

decibel with a 1.6 dB step. The front-end has a voltage gain of 43.8 dB when the RFVGA keeps the maximum gain mode and –7.9 dB when the RFVGA is at the minimum gain mode. Therefore, the RFVGA can obtain a 51.7 dB gain range, which is adequate for receiver gain tuning.

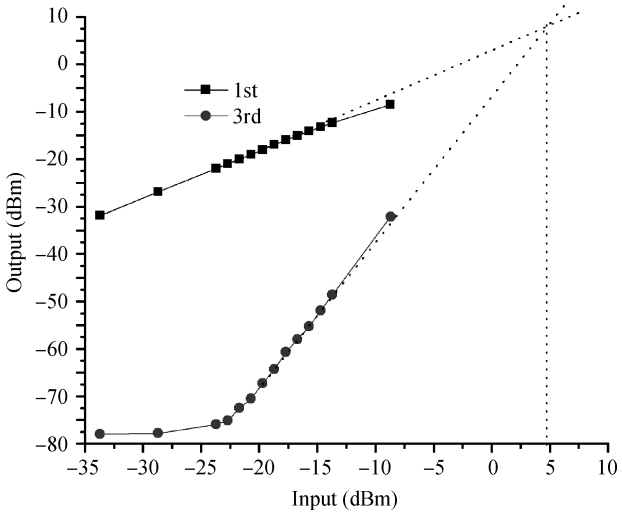

Fig. 13. Measurement result of IIP3.

Figure 10 shows the voltage gain of the RFVGA varying with the input level. The numerical values annotated at the y-axis are not the voltage gain of the RFVGA but the RFVGA tune step, which is directly proportional to the voltage gain of the RFVGA, as shown in Fig. 9. When the input level keeps increasing or decreasing, the LNA ON/OFF level is –28 dBm and –33 dBm.

Figure 11 shows the measurement NF varying with performing radio frequency when the front-end keeps in maximum gain mode. As shown in Fig. 11, the NF increases with the radio frequency increasing in both V-band and U-band. As designed, the NF is less than 4 dB in most of the operation frequency range, which is essential for achieving the required SNR when receiving a small signal.

Figure 12 shows the two-tone test result of the presented front-end. The two-tone radio frequencies are 660 MHz and 660.2 MHz with LO frequency of 658 MHz and the baseband frequencies are 2 MHz and 2.2 MHz. The third-order intermodulation (IM3) item loads at 1.8 MHz and 2.2 MHz. When the LNA stays at low gain mode and RFVGA stays at medium gain mode, the measured gain and IIP3 of the front-end are 2 dB and 4.9 dBm as shown in Fig. 13, which is necessary for a large input signal.

4. Conclusion

The RF front-end for zero-IF CMMB tuner adopts a new AGC strategy to obtain a high dynamic range and high immunity to adjacent channel interference. The front-end is fabricated in a 0.35 μm BiCMOS SiGe technology. The measurement results show that the presented front-end meets the requirement of a gain tuning range of 72 dB, including a 20 dB gain range of the LNA and 52 dB of the RFVGA. The presented front-end achieves a NF of less than 4 dB when operating at maximum gain and IIP3 4.9 dBm when LNA operates in low gain mode and RFVGA in medium gain mode. The die of the front-end occupies 1.32 mm^2 while consuming 25.6 mA from a 3.0 V supply.

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