LC voltage controlled oscillator in 0.18-μm RF CMOS*

Li Wenyuan(李文渊)†, Li Xian(李显), and Wang Zhigong(王志功)

Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China

Abstract: An integrated low-phase-noise voltage-controlled oscillator (VCO) has been designed and fabricated in SMIC 0.18 μm RF CMOS technology. The circuit employs an optimally designed LC resonator and a differential cross-coupling amplifier acts as a negative resistor to compensate the energy loss of the resonator. To extend the frequency tuning range, a three-bit binary-weighted switched capacitor array is used in the circuit. The testing result indicates that the VCO achieves a tuning range of 60% from 1.92 to 3.35 GHz. The phase noise of the VCO is –117.8 dBc/Hz at 1 MHz offset from the carrier frequency of 2.4 GHz. It draws 5.6 mA current from a 1.8 V supply. The VCO integrated circuit occupies a die area of 600 × 900 μm^2. It can be used in the IEEE802.11b based wireless local network receiver.

Key words: VCO; phase noise; Q-factor; load impedance; switched capacitor array

DOI: 10.1088/1674-4926/32/11/115003 **EEACC:** 1205; 1230B; 2570D

1. Introduction

Due to the rapidly growing application of high data rate wireless local networks (WLAN) based on the 2.4 GHz ISM band, the demand for small, cheap and low power RF circuit components are increasing. Since many crystals are expensive and take up a large area, they should be avoided; meanwhile, high frequency communication applications require programmable carrier frequencies for broadband applications. Indirect frequency synthesis techniques based on the phase-locked loop (PLL) are preferred for the generation of programmable carriers. A less accurate RF oscillator whose frequency can be controlled with a control signal is embedded in a feedback loop and its output frequency is locked to an accurate low frequency reference.

The voltage-controlled oscillator (VCO) is one of the most challenging components in on-chip transceivers because it consumes a major proportion of the overall power and area in a frequency synthesizer, and its performance determines, to a large extent, that of the whole system. In the design of a VCO, one of the critical problems is V_{DD} scaling, which results in a small oscillation amplitude. Phase noise, one of the most important specifications of VCOs, is inversely proportional to the oscillation amplitude[1]. Unfortunately, a voltage drop across a current source of VCOs also reduces the oscillation amplitude. Another challenge is a low loaded Q-factor of the total resonance due to the use of a poor on-chip inductor and a low equivalent loaded impedance of the resonant tank.

In this design, a new oscillator topology is presented to overcome these problems. To guarantee a relatively large oscillator amplitude, the tail current source is delimited. To average the loaded Q-factor of the LC-tank[2], an inductor with a low Q factor is inserted to provide high impedance in series with a pair of differential switching MOS transistors. To extend the tuning range, continuous and discrete tuning, not an enlarged PN junction[3], is introduced to decrease frequency sensitivity. Thus, a novel three-bit binary-weighted switched capacitor array with a high Q-factor is designed.

2. SMIC 0.18 μm RF CMOS technology

The rapid advancement of CMOS technology in the last decade has made possible the CMOS implementation of radio frequency (RF) integrated circuits. A major obstacle in CMOS RFIC design is the availability of high quality models for the active and passive components at GHz frequencies.

A well-characterized RF active and passive components model is needed for a successful RFIC design. Figure 1 shows the topology of an RF transistor model in SMIC 0.18 μm CMOS technology for high frequency simulation. In this model, additional parasitic components add to the intrinsic MOS characteristics modeled by BSIM3V3. R_{gate} is used to model gate resistance and L_{gate} is used to model gate induc-

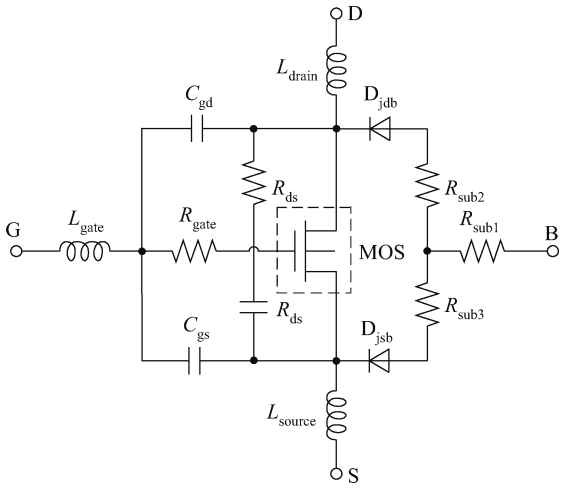


Fig. 1. RF MOSFET equivalent circuit.

* Project supported by the Scientific and Technologic Cooperation Foundation of the Yangtxe River Delta Area of China (No. 2008C16017).

† Corresponding author. Email: lwy555@seu.edu.cn

Received 6 April 2011, revised manuscript received 19 July 2011

Table 1. Technology parameters for NMOS and PMOS in the SMIC 0.18 μm RF CMOS.

Parameter	NMOS	PMOS
K (μA/V^2)	592	156
$\lvert V_T\rvert$ (V)	0.39	0.42
θ (V^{-1})	6.55	5.87
λ (V^{-1})	0.07	0.19
α	0.81	0.81
α_{gd}	0.21	0.21
α_{gb}	0.10	0.10
α_{db}	0.23	0.23
α_{sb}	0.16	0.16
γ	2	2
δ	4	4

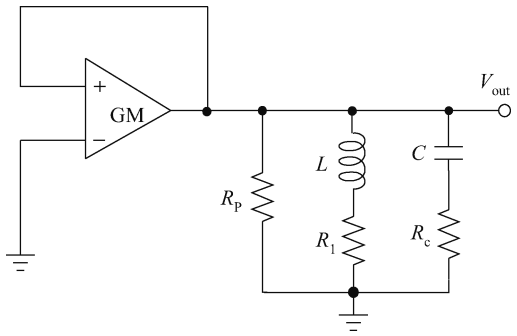


Fig. 2. Linear model of LC VCO.

tance at high frequency, R_{sub1}, R_{sub2} and R_{sub3} represent the substrate resistances network, D_{jsb} and D_{jbd} model the junction diodes of the source/drain to the bulk, C_{ds} and R_{ds} model the high frequency characteristics between drain and source, C_{gd} and C_{gs} represent the gate-to-drain (or to source) overlap capacitance, and L_{drain} and L_{source} represent the drain/source inductance at high frequency.

The simulation was performed using the model and, for hand calculation, several important technology parameters are extracted in Table 1, where K is the transconductance parameter in saturation, V_T is the threshold voltage, θ models the mobility degradation, λ is the channel length modulation parameter and the definitions of the other parameters can be found in Ref. [4].

3. VCO theory

An LC-tuned VCO is basically a feedback network that can be linearly modeled, as shown in Fig. 2[5]. The resonant tank is formed by a parallel resistor R_p, a capacitor C and an inductor L. Both the capacitor and the inductor have losses represented by two series resistors R_c and R_l. The active element, G_M, creates a negative resistance that compensates for these losses. Stable oscillation will occur at the frequency at which the loop transfer function is exactly equal to one. This is known as the Barkhausen criterion. The open-loop transfer function is given as

$$T_{loops}(s) = G_M \frac{sL}{1 + sL/R_{par} + s^2LC}, \tag{1}$$

where R_{par} is the equivalent parallel resistance, given as

$$\frac{1}{R_{par}} = \frac{1}{R} + \frac{R_l}{(sL)^2} + R_c \times (sC)^2. \tag{2}$$

The oscillation frequency can be easily found because the imaginary part of $T_{loop}(s)$ has to be zero at the oscillation frequency, which gives

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{3}$$

In the design of a VCO, the output frequency tuning range is very important. However, the variation of VCO output frequency with process and temperature imposes great challenges in fully integrated CMOS VCO implementation. CMOS VCOs are often designed with a tuning range two times wider than the desired application tuning range in order to compensate for process and temperature variations. Another key specification of a VCO is phase noise, which is defined as the noise power level with respected to the carrier at a given offset frequency. The theory of an LC-VCO is somewhat complicated and can be summarized in the following equations[6]:

$$R_{eff} = R_c + R_l + \frac{1}{R_p \times (\omega_0 C)^2}, \tag{4}$$

$$G_M = R_{eff} \times (\omega_0 C)^2, \tag{5}$$

$$L\{\Delta\omega\} = \frac{kTR_{eff}(1 + F)(\omega_0/\Delta\omega)^2}{P_{signal}}, \tag{6}$$

where R_{eff} is the total equivalent series resistance of the tank, G_M is the total transconductance required to maintain the oscillation, F is the excess noise factor of the amplifier, $\Delta\omega$ is the frequency offset from the carrier, P_{signal} is the power of the carrier signal and $L\{\Delta\omega\}$ is the single-sided spectral noise density at an offset $\Delta\omega$ from the carrier. These equations indicate that the phase noise is proportional to the resistance R_{eff} , as well as is the power consumption.

4. Circuit

4.1. VCO topology

In general, the tail current source in a typically LC-tuned VCO (shown in Fig. 3(a)) plays two important roles: firstly, it stabilizes the bias current and, secondly, it also prevents loaded Q-factor degradation because it provides the high impedance seen from the source of switching transistors, which is connected parallel to the LC-tank[2]. However, there are some drawbacks associated with using a tail current source. Firstly, the voltage headroom is cut down by the tail current sources and the output swing of the VCO is decreased by $2(V_{GS} - V_t)$, so the phase-noise performance deteriorates according to Eq. (6). Furthermore, the low frequency noise from the current source may be modulated to phase noise through up-conversion[5]. In typical VCOs, current source noise plays an important role in the generation of phase noise, especially in the $1/f^3$ region[1].

If the current source is removed from oscillator shown in Fig. 3(b), we can reduce a noise source to form phase noise and increase the oscillator amplitude up to nearly $2V_{DD}$. These are effective factors to gain low phase noise. However, the sources

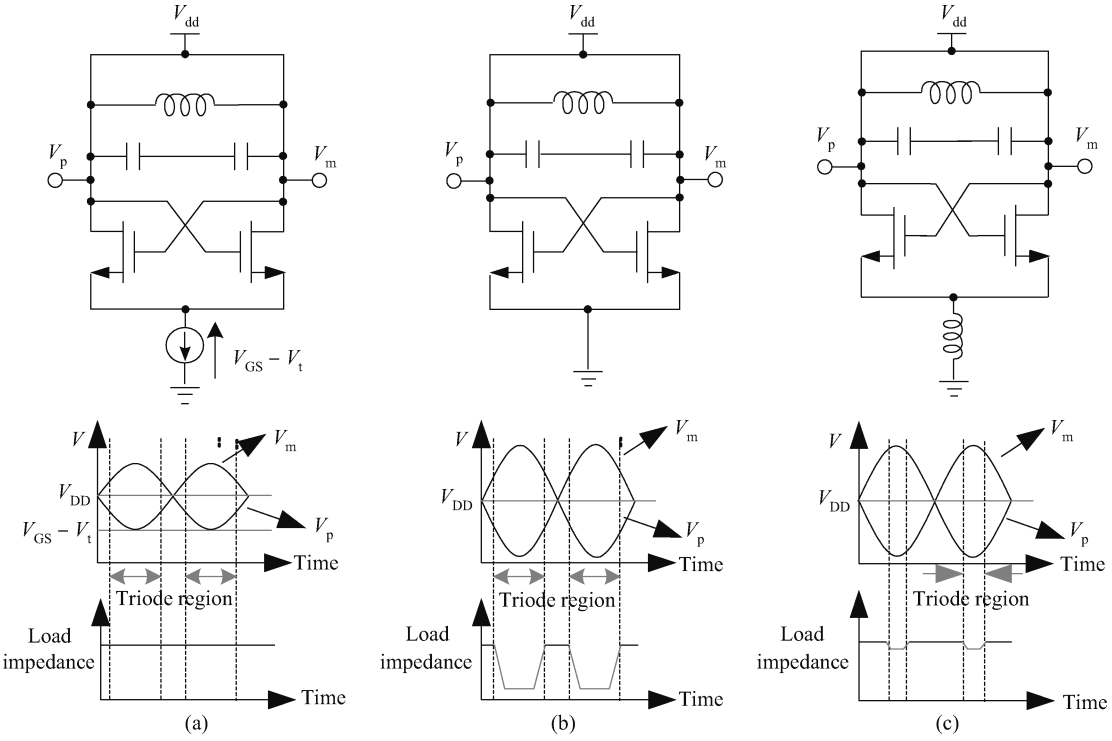


Fig. 3. Schematics of the VCO.

of the switching transistors are directly connected to ground in this VCO. In a period of oscillation, when the switching transistor is operated in the triode region, the equivalent turned-on resistor of the transistor is reduced to several hundred Ohm. This low parallel load will degrade the Q-factor of the resonant tank, which will degenerate the phase noise performance.

Combining the advantages of the VCO in Figs. 3(a) and 3(b), one proposed solution is shown in Fig. 3(c). An inductor is inserted between the sources of the transistors and ground to provide a relatively high impedance to load the resonant tank, preventing the degradation of the load Q-factor of the tank when the switching transistors operate in the triode region. It is noted that in wide tuning VCOs, this inductor should have a relative low Q-factor to guarantee that it can provide high impedance that is not so sensitive to frequency around the operating frequencies range of VCO. In general, the VCO in Fig. 3(c) has the following advantages: (1) less noise source to generate phase noise; (2) high oscillation amplitude; and (3) high load Q-factor of the tank in the period of oscillation. The only cost is the increase of the die area induced by the additional inductor.

4.2. Discrete tuning and 3-bit switched capacitor

A switched capacitor array technique[7] is proposed to extend the tuning range of the VCO. In this paper, a VCO with a novel three-bit binary-weighted switched capacitor array is designed, as shown in Fig. 4. The VCO has the same topology as that in Fig. 3(c), which has been discussed above. The three-bit binary-weighted switched capacitor array controlled by digital words SW (4 : 2 : 1) is shown in Fig. 4(b). Compared with the switched capacitor in Ref. [7], this design only uses one transistor for each switched capacitor, thus the quality factor of the resonant tank is doubled, resulting in good phase noise performance.

In practice, the three-bit binary-weighted capacitor tunes the oscillator center frequency to eight discrete frequencies and then a small inversion-mode varactor is interpolated to tune the oscillator continuously around these eight discrete frequencies. Appropriate design of the sizes of the switched transistors, as well as the capacitance of C_{LSB}, will give rise to eight overlapping tuning curves to guarantee continuous frequency tuning over the entire tuning range.

The unit capacitance C_{LSB} of the switched capacitor array is also very important. The larger its value, the smaller tuning range around every discrete frequency obtained, as well as the phase noise performance becoming worse. A value of C_{LSB} must be chosen to guarantee that the overlap of the adjacent tuning curves is about 50%.

By using a three-bit binary-weighted switched capacitor array, the frequency tuning ration (FTR) in terms of the tank capacitor can be expressed as the following:

$$\mathrm{FTR} = \frac{1}{2\pi}\frac{1}{F_{\mathrm{o}}}\left(\frac{1}{\sqrt{LC_{\mathrm{min}}}} - \frac{1}{\sqrt{LC_{\mathrm{max}}}}\right), \tag{7}$$

where

$$\begin{aligned} C_{\mathrm{min}} &= C_{\mathrm{var,\,min}} + C_{\mathrm{SW,\,min}} + C_{\mathrm{par}}, \\ C_{\mathrm{max}} &= C_{\mathrm{var,\,max}} + C_{\mathrm{SW,\,max}} + C_{\mathrm{par}}. \end{aligned} \tag{8}$$

F_{o} in Eq. (7) is the center frequency of the tuned VCO, $C_{\mathrm{var,\,max}}$ and $C_{\mathrm{var,\,min}}$ are the largest and smallest capacitances during the variation of the continuous tuning varactor. $C_{\mathrm{SW,\,max}}$ and $C_{\mathrm{SW,\,min}}$ are the parasitic capacitances when the digital control words of the switched capacitance array SW(4 : 2 : 1) = 111 and SW(4 : 2 : 1) = 000, respectively, and C_{par} is the fixed parasitic capacitance from the active and passive devices and interconnects.

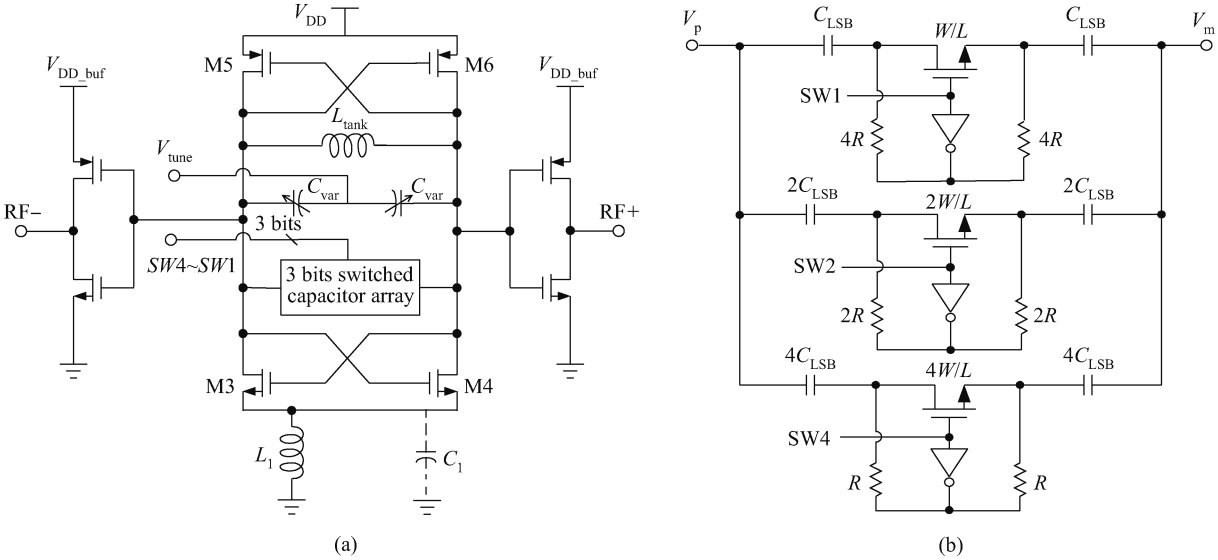


Fig. 4. (a) Designed VCO and (b) three-bit binary-weighted switched capacitor.

4.3. Amplifier

According to Ref. [8], the most important parameter for the design of the amplifier is the overdrive voltage, the $|V_{gs}-V_{th}|$ of the NMOS and PMOS transistors. The choice of $|V_{gs}-V_{th}|$ determines the output amplitude, the power consumption and the flicker-noise up-conversion. In this design, the value of $|V_{gs}-V_{th}|$ is chosen as about 0.45 V for both NMOS and PMOS transistors.

It is often stated that phase noise up-conversion can be greatly reduced by matching the transconductance of PMOS and NMOS negative cells in a complementary style VCO[9], which results in

$$\sqrt{2\mu_n C_{ox}\frac{W_n}{L_n}I_{ds}} = \sqrt{2\mu_p C_{ox}\frac{W_p}{L_p}I_{ds}}. \tag{9}$$

μ_n and μ_p are the channel mobilities for n-channel and p-channel devices, and C_{ox} is the capacitance per unit area of the gate oxide. W_n/L_n and W_p/L_p are the effective channel width–length ratios for NMOS and PMOS, respectively.

Simultaneously, to guarantee that the waveform of the oscillator is symmetric, the capacitor of PMOS and NMOS negative cells should also be matched, which can be expressed as

$$W_n L_n = W_p L_p. \tag{10}$$

Combining (9) and (10), the following equation can be obtained

$$L_n = L_p\sqrt{\frac{\mu_n}{\mu_p}}. \tag{11}$$

Equation (11) implies that the length of the NMOS transistors is about twice that of the PMOS transistors for lowering flicker-noise up-conversion.

5. Test results

The proposed LC VCO shown in Fig. 4 is fabricated in SMIC 0.18-μm RF CMOS technology. The chip micrograph is shown in Fig. 5 and the active area is about 600 × 900 μm^2.

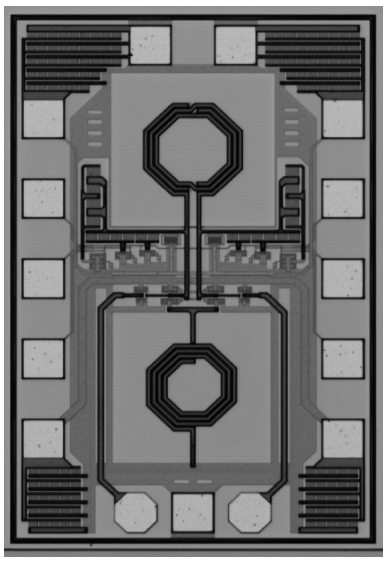


Fig. 5. Photo of the oscillator.

The oscillator is measured on an Agilent RF testing platform. The measured frequency tuning characteristic curve is shown in Fig. 6. It can be seen that the eight overlapping tuning curves cover the desired frequencies and the tuning linearity is good. The VCO achieves a tuning range of 60% from 1.92 to 3.35 GHz. Figure 7(a) shows the measured output spectrum of the designed VCO, the power of the carrier about 2.4 GHz is –0.79 dBm. The phase noise is measured using the spectrum analysis method. Figure 7(b) shows the phase noise performance near a 2.4 GHz carrier, the phase noise is about –117.82 dBc/Hz at 1 MHz offset from the carrier.

A figure-of-merit (FOM) is employed to evaluate the three performance parameters of the VCO: frequency, phase noise and power consumption[10], which is

$$\mathrm{FOM} = 10\lg\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2\frac{1}{L\{\Delta\omega\}P}\right], \tag{12}$$

where $L\{\Delta\omega\}$ is the total single-sideband phase noise spectral

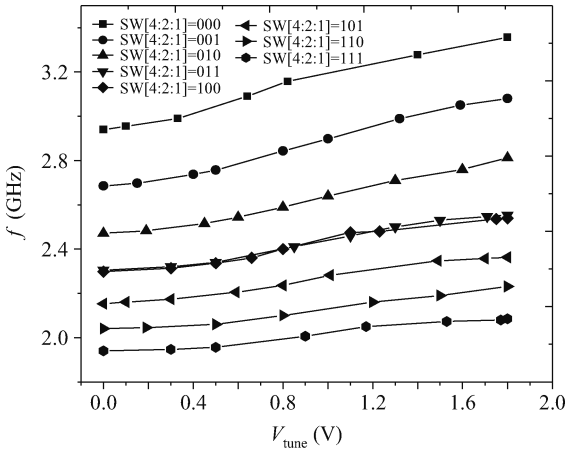
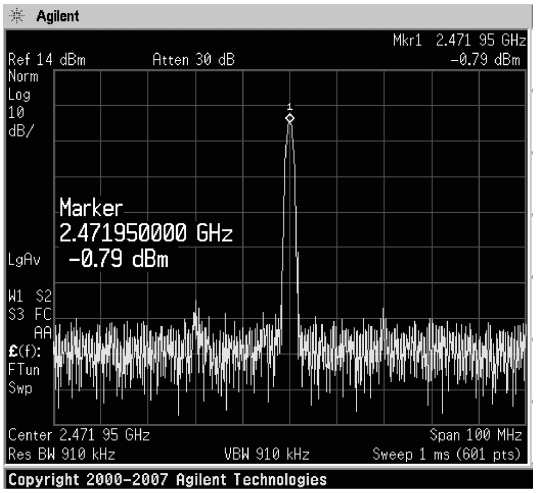
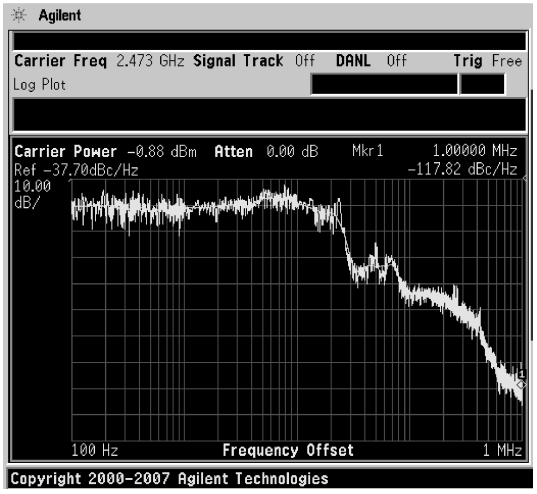


Fig. 6. Frequency tuning curves of the proposed VCO.



(a)



(b)

Fig. 7. Measured (a) output spectrum and (b) phase noise around 2.4 GHz carrier.

density at an offset frequency $\Delta\omega$ from the carrier frequency, ω_0, P valued in mW is the power dissipated by the oscillator core. The higher value of the FOM implies that the oscillator has achieved a better performance.

To evaluate VCO performance with phase noise and power consumption, as well as frequency tuning range (FTR), a new figure-of-merit ($\mathrm{FOM_T}$) is presented in Ref. [11], which can be expressed as

$$\mathrm{FOM_T} = \mathrm{FOM} + 20\lg\frac{\mathrm{FTR}}{10}, \tag{13}$$

where FTR is the frequency tuning range in percent. Similarly, a high value of $\mathrm{FOM_T}$ implies a good performance of the VCO.

Based on the discussion above, the performance of the VCO is summarized in Table 2 below together with other recent state-of-the-art VCOs.

Table 2. Comparison of VCO performance.

Parameter	Ref. [12]	Ref. [13]	Ref. [14]	This work
CMOS process (μm)	0.18	0.25	0.18	0.18
F_{O} (GHz)	2.4	2.4	2.4	2.4
FTR (%)	12.5	11.6	1.7	58.3
$L\{\Delta f\}$ (dBc/Hz)	−138	−105	−134	−117.8
Δf (MHZ)	3	0.6	1	1
P_{Diss} (mW)	5.4	17.5	4.6	10.2
FOM (dBc/Hz)	188.7	164	195	175.4
$\mathrm{FOM_T}$ (dBc/Hz)	190.6	175.1	179.6	191.42

6. Conclusion

A LC VCO is designed in SMIC 0.18-μm RF CMOS technology. The VCO achieves a tuning range of 60% from 1.92 to 3.35 GHz, and achieves a phase noise of –117.82 dBc/Hz at 1 MHz offset from the carrier frequency of 2.4 GHz, drawing 5.6 mA current from 1.8 V supply. The value of $\mathrm{FOM_T}$ for the designed VCO is 191.42 dBc/Hz.

References

[1] Leeson D B. A simple model of feedback oscillator noise spectrum. Proc IEEE, 1966, 54(2): 329
[2] Hegazi E, Sjoland H, Abidi A. A filtering technique to lower LC oscillator phase noise. IEEE J Solid-State Circuits, 2001, 36(12): 1921
[3] Kral A, Behbahani F, Abidi A. RF CMOS oscillators with switched tuning. Proc IEEE Custom Integrated Circuits Conf, 1998: 555
[4] Leroux P, Steyaert M. LNA-ESD co-designed for fully integrated CMOS wireless receivers. Dordrecht: Kluwer Academic Publishers, 2005
[5] Craninckx J, Steyaert M. Wireless CMOS frequency synthesizer design. Dordrecht: Kluwer Academic Publishers, 1998
[6] Craninckx J, Steyaert M. Low-noise VCO using enhanced LC-tanks. IEEE Trans Circuits Syst II, 1995, 42: 794
[7] Hegazi E, Rael J, Abidi A. The designer's guide to high-purity oscillators. New York: Kluwer Academic Publishers, 2005
[8] De Muer B, Borremans M, Steyaert M, et al. A 2-GHz low phase noise integrated LC-VCO set with flicker-noise upconversion minimization. IEEE J Solid-State Circuits, 2000, 35(7): 1034
[9] Kao Y H, Hsu M T. Theoretical analysis of low phase noise design of CMOS VCO. IEEE Microw Wireless Compon Lett, 2005, 15(1): 33
[10] Kinget P. Integrated GHz voltage controlled oscillators. Norwell, MA: Kluwer Academic Publishers, 1999

[11] Kim J, Plouchart J, Zamdmer N, et al. A power optimized widely-tunable 5-GHz monolithic VCO in a digital SOI CMOS technology on high resistivity substrate. Proc International Symposium on Low Power Electronics and Design, 2003

[12] Yan W H, Park C H. Filtering technique to lower phase noise for 2.4 GHz CMOS VCO. Solid-State and Integrated-Circuit Technology, 2008: 1649

[13] Li C S, Wang W Q, Chi Y. A full integrated 2.4 GHz ISM band 0.25 mm CMOS VCO with 11.6% tuning range. 4th International Conference on Microwave and Millimeter Wave Proceeding, 2004: 598

[14] Li Z, Kenneth K O. A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator. IEEE J Solid-State Circuits, 2005, 40(6): 1296