An electroplating topography model based on layout-dependent variation of copper deposition rate*

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Abstract: A layout-pattern-dependent electroplating model is developed based on the physical mechanism of the electroplating process. Our proposed electroplating model has an advantage over former ones due to a consideration of the variation of copper deposition rate with different layout parameters during the process. The simulation results compared with silicon data demonstrate the improvement in accuracy.

Key words: design for manufacturing; electroplating; modeling
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1. Introduction

Chemical-mechanical polishing (CMP) is used as a planarization technology in "dual-damascene" processes[1, 2]. In order to model post-CMP copper and oxide thickness variations, a model to predict electroplating (ECP) topography is required[3]. Some evolutionary electroplating models have been proposed. One modeling method was proposed based on computational fluid dynamics (CFD) and "curvature enhanced accelerator coverage" theory[4]. Another numerical simulation was carried out with a linked Monte–Carlo finite difference code[5]. Some other numerical methods, such as a first-order differential equation and a finite element simulation, were used in these evolutionary models[6, 7]. These kinds of model simulate the whole ECP procedure step by step and need to solve groups of formulae, which is very time-consuming. However, according to the requirements of computational resource and efficiency, a response surface model is preferred as the preparation for an ECP/CMP process simulation[8, 9].

One of the first ECP response surface models was proposed by Park[8], where the step and array heights are modeled by two separated polynomials. However, there are some potential problems in this model. One is the lack of physical insight into influencing factors[10]. Another is that a large number of calibration parameters have to be used, which may lead to overfitting. So, in Luo *et al.*'s work[11], a more accurate ECP process model was proposed, where the step and array heights are connected with a consideration of the physical mechanism. The key idea in this model is that the volume of copper deposited is proportional to the surface area. However, during the simulation using this model, some mismatches between simulated results and silicon data are found in some feature sizes after calibration. Although this model takes the physical mechanism into account, some details are neglected about the procedure, such as the deposition rate in and out of different trenches.

From industrial-based experiments, we observed that the growth rate of copper at the trench bottom is not the same as that on the surface of a field oxide and even not the same as each other of different trench widths. Because of the influence of the accumulated additives adhered on the trench sidewall and the effective trench bottom area, the growth rate of copper on the trench bottom changes as time elapses and is different from that on the surface of a field oxide. In addition, the copper width shrinkage above the feature trench varies according to different pattern characteristics such as density, wire width and pitch.

To address these two issues, we rebuild the electroplating model based on the work mentioned above[11]. Another two modified coefficients are introduced into the model separately. One is to distinguish the copper deposition rate at the trench bottom from that on the surface of the field oxide. The other is to describe the shrink of copper width in a conformal fill situation. With these two extra descriptions, the layout-pattern-dependent-electroplating process is simulated and post-ECP topography is predicted more accurately.

2. Fundamentals of the electroplating topography model for three cases

Copper has replaced aluminum as an interconnection material due to its lower bulk resistivity in deep submicron meter technology nodes. As a result, the "dual-damascene" pro-

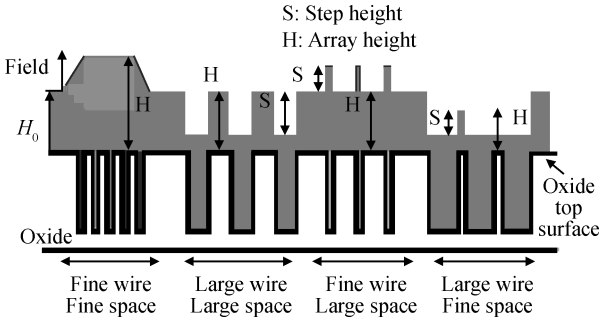

Fig. 1. Typical post-ECP topography[8].

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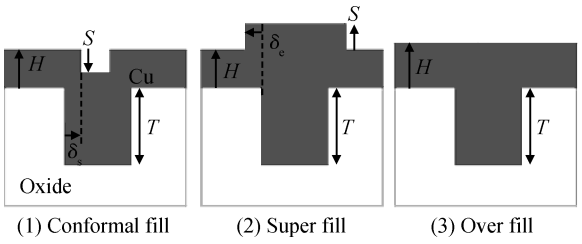

Fig. 2. Three kinds of post-ECP wire topographies [11].

cess[1, 2] was developed. Some of the steps depend on layout pattern, so a topography model is built to help designers evaluate the interconnection parameter variations for a DFM issue[3].

During the electroplating process, the wafer is immersed in chemical solutions with a large number of Cu ions. The Cu ions in the solutions react with the electrons to form Cu on the surface of the wafer where the current passes through. Figure 1 shows that the post-ECP topography strongly depends on the layout pattern. In this typical line-space pattern topography after the ECP process, the heights of the copper surface in different positions vary a great deal due to different wire widths and spaces. H_0 represents the copper thickness above the field oxide. H is the copper thickness above the oxide in array, which is called the array height. S is defined as the difference between copper height above the oxide in array and that above the trench. If the copper height above an array oxide is larger than the copper height above the trench, S is a positive value. Otherwise, it is a negative value.

For a single wire, three topographies may exist due to its wire width and different pattern environment, as Figure 2 shows. For conformal fill of case (1), the copper above the oxide is higher than that above the trench. The step height is positive, so we call this conformal fill. In this case, the copper width above the feature trench will shrink by δ_s. For the super-fill of case (2), the copper width above the feature trench expands by δ_e. For an over-fill of case (3), the copper surface is flat and the step height is 0.

The basic topography model[11] we used was a response face one. During the simulation, the layout will be divided into a large number of tiles with a size of D × D. The post-ECP topography is predicted as a function of layout pattern parameters through the evaluation of the deposited copper volume. Two aspects are considered. One is the additive physics perspective as in Eq. (1):

$$V = H_0(T_e L + D^2), \tag{1}$$

where T_e is the effective trench depth and L is the perimeter in each tile. The other is the topography geometry perspective. The array height, H, and step height, S, for the above three filling cases are formulated as follows: Case (1),

$$H = H_0(1-\rho)/(1-\rho_s), \tag{2}$$

$$S = H_0(1-\rho)/[(1-\rho_s)\rho_s] + T\rho/\rho_s - H_0 T_e L/(D^2\rho_s) - H_0/\rho_s. \tag{3}$$

Case (2),

$$H = H_0, \quad S = T\rho/\rho_e - H_0 T_e L/(D^2\rho_e). \tag{4}$$

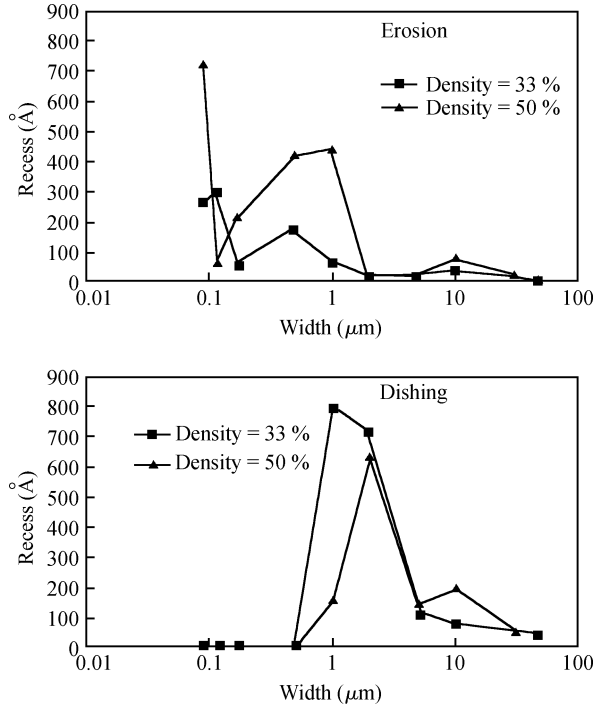

Fig. 3. Shift error between silicon data and simulated results based on the original model[11].

Case (3),

$$H = H_0 + H_0(T_e L/D^2) - T\rho, \quad S = 0. \tag{5}$$

3. Parameter calibration and simulation results

We demonstrate this electroplating model via one industrial-based experiment. Silicon data are collected under a dual-damascene 65 nm BEOL process. Based on the process parameters and in-line inspection data, the final copper thickness above the field oxide H_0 is about 7000 Å. From the-wide-line-wide-space test results of the wafer profile after ECP, the trench depth T could be estimated as about 2600 Å. From the erosion of an array whose line width is from 2 to 5 μm and Eq. (2), δ_s is calculated to be about 600 Å. Based on the data of over-fill patterns and Eq. (5), T_e is equal to about 500 Å. δ_e can be acquired as being about 7500 Å from the measurement data and procedure of fitting.

After the calibration of basic parameters, we choose two groups of data to compare the silicon data collected by an AFP (atomic force profile) tool and simulation results based on the original model for electroplating[11]. The one is the line-space array with a pattern density of 50%, and the other is that with a pattern density of 33%.

4. Limitation of the original model and improvements

In Fig. 3, the values of the data points represent the erosion or dishing difference between the test data and simulated results. From a different pattern with 50% density, the simulated erosion data varies from the test value when the line width is less than 2 μm and the simulated dishing is different from test

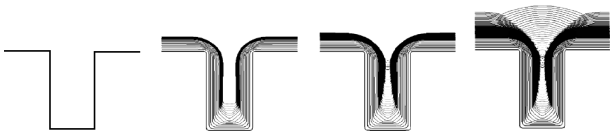

Fig. 4. Procedure of copper deposition in a trench.

data when the line width is larger than 1 μm. From the pattern group with 33% density, the simulated erosion meets the silicon data while the simulated dishing shows some error when the line width is between 1 μm and 5 μm. For the limitation of simulation accuracy, we think that the above model should be based on the electroplating procedure.

In Fig. 4, the growth of copper in a single trench is shown. According to the original ECP model[6], the growth rate of copper on the trench bottom is just the same as that on the surface of a field oxide. Whereas, because of the influence of the accumulated additives adhered to the trench sidewall and the shrinking of the effective trench bottom area, the copper deposition rate on the trench bottom changes as time goes on. It is different from that on the surface of the field oxide. Besides that, the copper width shrinkage above the feature trench varies a great deal according to different pattern variables such as density, wire width and space. So that for these two issues, an extra two modified coefficients are introduced into the model separately.

One is to distinguish the copper deposition rate on the trench bottom from that on the surface of the field oxide. During the calculation of deposited copper volume based on the additive physics in the model, Equation (1) is changed as:

$$V = H_0[T_e L + (f_1\rho + 1 - \rho)D^2], \tag{6}$$

where the coefficient f_1 describes the variation of copper growth rate at the trench bottom.

The other is to describe the shrinkage of trench width in case (1) of Fig. 2. During the calculation of deposited copper volume based on the geometry perspective in case (1), the equation is formed as:

$$V = HD^2 - SD^2 f_2\rho_s + TD^2\rho, \tag{7}$$

where the coefficient f_2 relates to the pattern-dependent shrinking trench width.

As a result, the new topography model for the three deposition cases is rebuilt. Step height and array height are obtained as follows:

Case (1):

Since the accelerator in the trench accumulates on the trench bottom and cannot flow out, the growth of the copper on oxide surface is due to the accelerator on oxide. Combining Eqs. (6) and (7), the array height and step height are formulated as:

$$H = H_0(1-\rho)/(1 - f_2\rho_s), \tag{8}$$

$$S = H_0(1-\rho)/[(1 - f_2\rho_s) f_2\rho_s] + T\rho/f_2\rho_s - H_0 T_e L/(D^2 f_2\rho_s) - H_0(f_1\rho + 1 - \rho)/f_2\rho_s. \tag{9}$$

Case (2):

In this case of super fill, the copper thickness above the oxide out of the expanding range will not be affected by the accelerator in the trench. The volume of copper is formulated as:

$$V = HD^2 - SD^2\rho_e + TD^2\rho. \tag{10}$$

As a result, the array height is equal to the copper thickness on the field oxide H_0. Therefore H is equal to H_0. So this yields the array height and the step height for case (2) after combining Eqs. (6) and (10):

$$H = H_0, \quad S = T\rho/\rho_e - H_0 T_e L/(D^2\rho_e) + H_0(1-f_1)\rho/\rho_e. \tag{11}$$

Case (3):

From a topography geometry perspective, the copper volume can be formed as:

$$V = HD^2 + TD^2\rho. \tag{12}$$

For case (3), the step height S is 0 and the topography density is 1. Therefore, the array height and the step height are formulated as:

$$H = H_0(f_1\rho + 1 - \rho) + H_0(T_e L/D^2) - T\rho, \quad S = 0. \tag{13}$$

5. Experiments and verification

An improved electroplating model including modified coefficients f_1 and f_2 has been built up in Section 4. According to the relative differences of line width and space, the situations are divided into four categories, as Figure 1 shows: fine wire fine space (FWFS), fine wire large space (FWLS), large wire fine space (LWFS) and large wire large space (LWLS). The influence of modified coefficients should be considered only in case (1), which describes LWLS and LWFS, and in case (3), which describes FLFS. As mentioned at the end of Section 4, f_1 and f_2 are calibrated separately. During the calibration, the relationship between modified coefficient f_1, f_2 and layout pattern dependent variables such as density ρ, wire width w and wire space s are acquired. So in the equations, most coefficients are constant except these three ones.

In case (1), f_1 could be calculated based on erosion data and Eq. (13). We can use some fitting method to determine the relationship between f_2 and wire space s: $f_2 = g(space) + c_1$ Then we replace f_2 with the above value in Eq. (14), a similar functional relationship between f_1 and wire width w can be acquired as: $f_1 = g(space) + c_2$

In case (3), the situation is more complicated, so we need to consider coefficient f_1 in different segments. According to the calculation of erosion in Eq. (17), the coefficient f_1 can be evaluated. For the pattern whose wire width is larger than 0.12 μm but less than 0.5 μm, f_1 can be fitted as the first-order function of pattern density and wire width. $f_1 = g(\rho, space) + c_3$

where c_1, c_2 and c_3 represent constants.

According to above fitting results and the improved electroplating model, the array and step heights are simulated in Figs. 5 and 6. These two charts represent the difference between AFP test data and simulated results based on both original and improved electroplating models. The data points connected by a real line show the improvements. With the introduction of two coefficient factors, the error between the simulation results and the silicon data declines. From the comparison

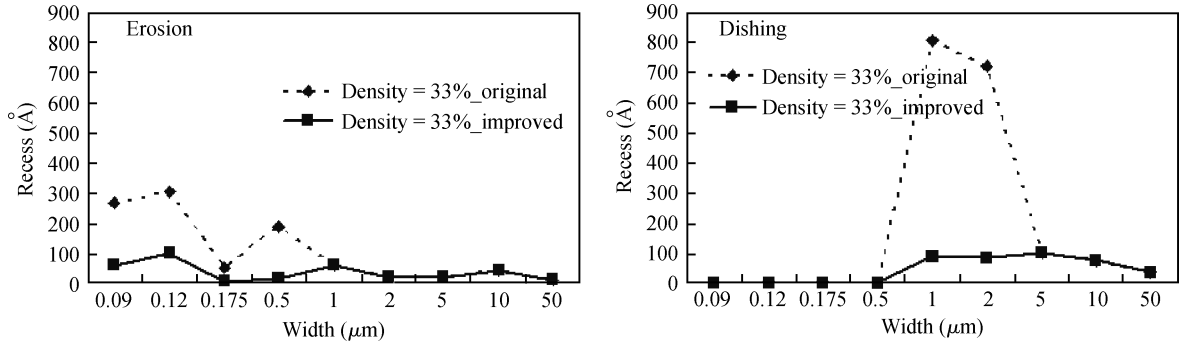

Fig. 5. Shift error between silicon data and an improved simulation for a 33% density pattern.

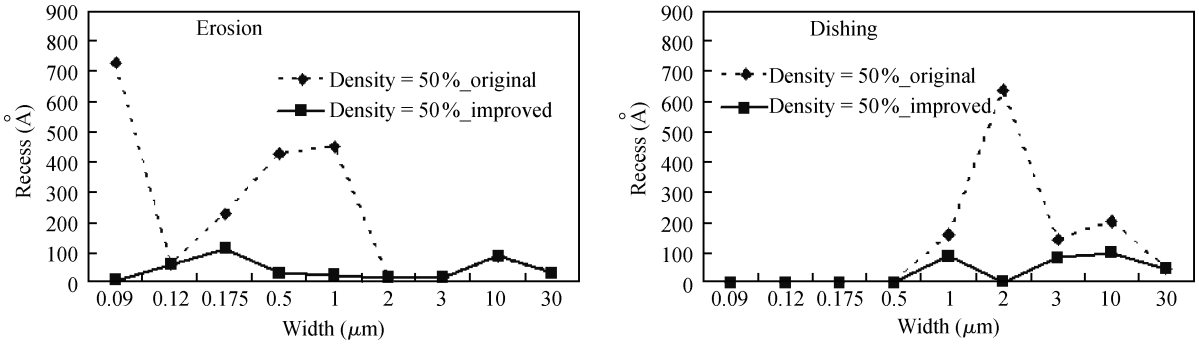

Fig. 6. Shift error between silicon data and an improved simulation for a 50% density pattern.

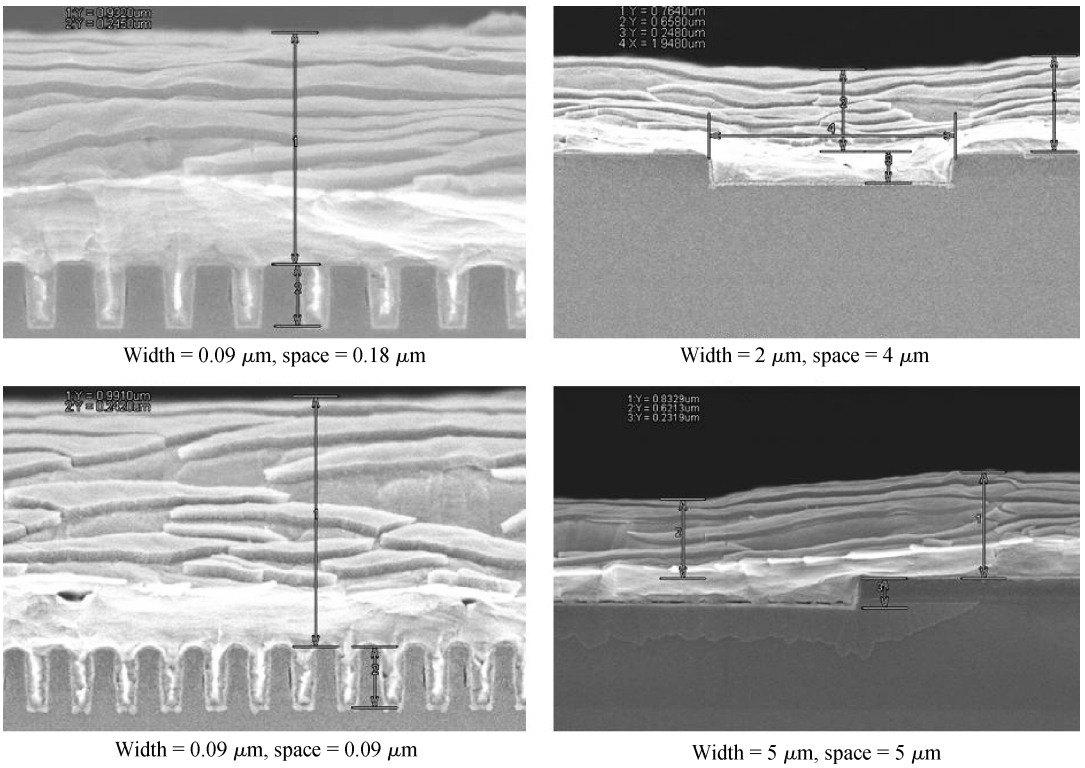

Fig. 7. Cross-section photos collected by SEM. (1) Width/space = 0.09 μm/0.18 μm. (2) Width/space = 2 μm/4 μm. (3) Width/space = 0.09 μm/0.09 μm. (4) Width/space = 5 μm/5 μm.

in the figures, the improved erosion of the fine line with width less than 1 μm reveals its accuracy. So is the simulated dishing of the wide line with width between 1 μm and 5 μm. All of the shift errors are below 100 Å.

The measurement error of the scanning electron microscope (SEM) is much larger than the AFP test and it is difficult

Table 1. Verification of simulated copper thickness by SEM measurements.

Measure Point	Width (Å)	Space (Å)	Density (%)	SEM_Thk (Å)	Simu_Thk (Å)	Error (Å)	Error (%)
1	0.09	0.18	33	11770	11503	267	2.27
2	2	4	33	9060	8790	270	2.98
3	0.09	0.09	50	12330	11954	376	3.05
4	5	5	50	8532	7692	840	9.85

to analyze the variation between different patterns accurately with SEM test data. So the surface profile is more useful to the ECP process simulation than copper thickness and the calibration is mainly based on AFP test data during the electroplating process modeling. However, we still take cross-section measurements by SEM for reference and as verification. In the experiments, SEM photos of some measured points are collected and listed in Fig. 7. The details of the related comparison are shown in Table 1. For over a 7500-Å post-ECP copper thickness, the difference between the silicon data and the simulated results is below 10%.

6. Conclusions and next steps

In this paper, an improved model for ECP based on the physical mechanism of electroplating in a dual-damascene process is presented. The copper deposition variation on the trench bottom and sidewall is involved and described after two coefficients are introduced. From a comparison of the simulation results in Section 5, it can be found that the accuracy of prediction for the electroplating process is improved. This model is not just limited to dealing with test structures. After being embedded into the process simulation tools, the full chip simulation of the electroplating process is enabled with a consideration of the interaction length.

In a next step, we will continue with our research of ECP process modeling under advanced technology nodes. At the same time, a more efficient method and simulator will be developed for the simulation of functional chip designs.

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