Digitally controlled oscillator design with a variable capacitance XOR gate

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Abstract: A digitally controlled oscillator (DCO) using a three-transistor XOR gate as the variable load has been presented. A delay cell using an inverter and a three-transistor XOR gate as the variable capacitance is also proposed. Three-, five- and seven-stage DCO circuits have been designed using the proposed delay cell. The output frequency is controlled digitally with bits applied to the delay cells. The three-bit DCO shows output frequency and power consumption variation in the range of 3.2486–4.0267 GHz and 0.6121–0.3901 mW, respectively, with a change in the control word 111–000. The five-bit DCO achieves frequency and power of 1.8553–2.3506 GHz and 1.0202–0.6501 mW, respectively, with a change in the control word 11111–00000. Moreover, the seven-bit DCO shows a frequency and power consumption variation of 1.3239–1.6817 GHz and 1.4282–0.9102 mW, respectively, with a varying control word 1111111–0000000. The power consumption and output frequency of the proposed circuits have been compared with earlier reported circuits and the present approaches show significant improvements.

Key words: digital control oscillator; delay cell; power consumption; variable capacitance; voltage controlled oscillators; XOR gate

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1. Introduction

Clock frequencies and data rates have increased with each new generation of communication and microprocessor technology. In modern high performance systems, the phase-locked loop (PLL) is the most frequently used circuit component, with wide application in frequency synthesis, clock and data recovery[1–4]. Normally, the clock is generated by analog circuits called PLLs, which contain a phase detector, a charge pump, a loop filter and a voltage controlled oscillator. Analog PLLs have shortcomings of sensitivity towards process deviation and high power consumption. With the introduction of very large scale integration (VLSI) technology, the all-digital phase-locked loop (ADPLL) has become an important building block for digital systems[3–6]. Digitally controlled PLLs are more robust, consume less power and require a smaller layout area on integrated circuits. The digitally controlled oscillator (DCO) is the central block of these ADPLL systems and replaces the voltage controlled oscillator (VCO) in analog PLLs. The propagation delay of each cell and the number of delay cells in the closed loop determines the total delay of a ring based oscillator circuit[7, 8]. Digitally controlled delay elements (DCDEs) are the elementary building blocks for any DCO circuit and their optimized design contributes to overall performance. Three foremost techniques for varying the delay of a DCDE are: driving strength fixed capacitive loading[8, 9], shunt capacitive loading[10–13] and variable resistance[14]. A conventional shunt capacitance DCDE is shown in Fig. 1. Here, C_V serves as the variable capacitive load and consequently changes the delay of the circuit from input (In) to output (Out).

Power consumption is currently an important consideration for VLSI (very large scale integration) system design[15]. The wide usage of battery operated and mobile devices has further added to research work in the field of low-power VLSI design. DCOs are a major constituent of an ADPLL system and liable for most of the power consumption. Ring based topology for DCO designs is widely used[12, 13, 16, 18–20]. This paper proposes a ring based DCO design with new delay elements using varying capacitive load. A three-transistors XOR gate[21] has been used as the variable load for delay variations. The gate capacitance of the XOR gate varies with a change in control bits, which further changes the delay of the circuit. Efforts have been made to reduce the power consumption in proposed DCO designs using optimized XOR gates.

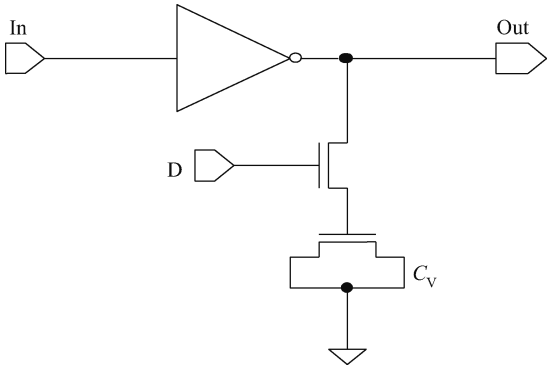

Fig. 1. Conventional delay cell with shunt capacitance.

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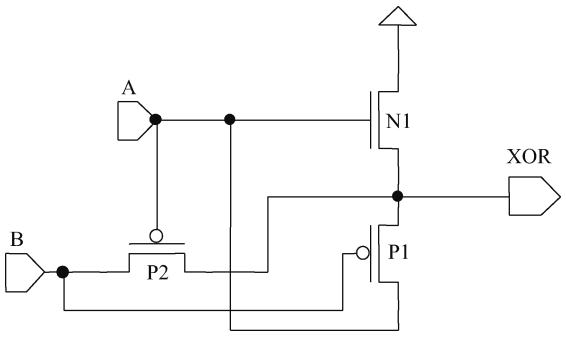

Fig. 2. 3-transistor XOR gate.

2. Circuit description

The oscillators designed here are based on single ended DCDEs used in a ring topology. Three-, five- and seven-stage DCOs have been designed with digital control bits. The proposed structure utilizes the variable capacitance loading method for ring based DCO design. A three-transistor XOR gate, as shown in Fig. 2, has been used for variable capacitive loading. In the proposed XOR, the gate lengths of all transistors have been taken as 0.18 μm. The widths (W_n) of the PMOS transistors (P1 and P2) have been taken 2.0 μm. The width (W_p) of the NMOS transistor (N1) has been taken as 0.25 μm.

A delay cell using a CMOS inverter and an XOR gate is shown in Fig. 3(a). The inverter part width of the PMOS transistor (P3) is taken as 1.25 μm, whereas the width of the NMOS transistor (N2) is taken as 0.5 μm. The CMOS inverter delay cell has been improved with the addition of digitally controlled variable capacitive loading. The gate-to-channel capacitance of the MOS transistor contributes to the overall gate capacitance, which further contributes to the total output capacitance (C_L) of the delay cell. This capacitance varies with the application of control bits, which are responsible for modulating the propagation delay of individual stages.

Here, in Fig. 3(a) the total gate to source/drain capacitance of transistors N1, P1 and P2 show variation with applied digital control bit D. The total capacitance at node C_L depends on the gate capacitance of N1 and P2, which further depends on the value of control bit D. An equivalent circuit of the proposed delay cell is shown in Fig. 3(b). C_I is the capacitance before the application of control bit D and ΔC is the change in capacitance with the application of control bit D. Values of capacitance are dependent on the external bias voltage applied across the pn junction in MOS transistors. Equivalent capacitance (C_{eq}) is related to voltage differences, as shown in Eq. (1), where C_j is the junction capacitance.

$$C_{eq} = \frac{\Delta Q}{\Delta V} = \frac{1}{V_2 - V_1} \int C_j dV. \quad (1)$$

With the application of a low (0) control bit (D), the transistor P1 is the ON condition and the V_{ds} of N1 transistor is increased, due to which the voltage difference between the gate and drain/source voltage of N1 is reduced. This reduced voltage difference increases the gate capacitance of N1. The gate capacitance of transistor P2 decreases as the voltage difference between the gate and source/drain terminal of P2 is increased with low D input. C_{eq} of transistor P2 decreases, which further

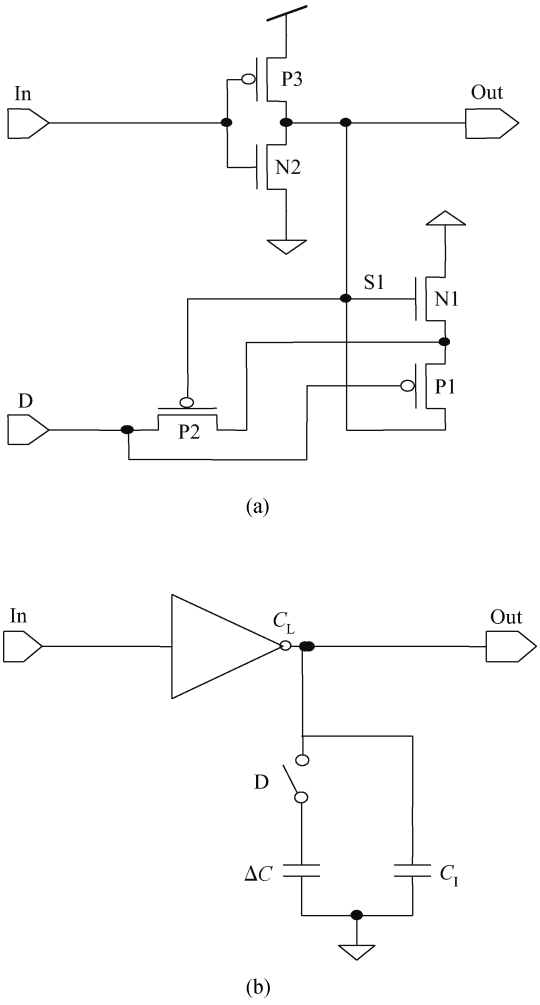

Fig. 3. (a) Delay cell with XOR gate variable capacitance. (b) Equivalent circuit.

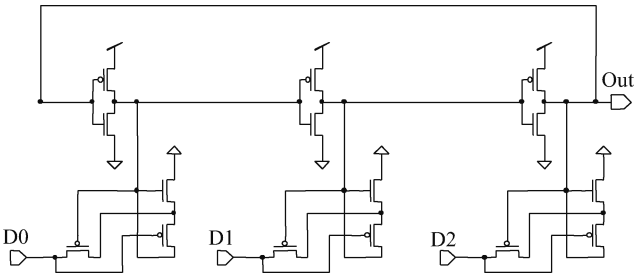

Fig. 4. 3-stage DCO.

affects the total load capacitance (C_L). Moreover, for transistor P1 the gate capacitance also decreases with low (0) applied control bit (D). The widths of the transistors (P1 and P2) are large, so these transistors contribute more to the total load capacitance and the net effect is a decrease in the load capacitance of the delay cell with low (0) control bit. With a decrease in capacitance the delay of the DCDE is reduced and the output frequency rises.

In another case when control bit (D) is high, the transistor P1 is in the OFF condition and the voltage difference between the gate and drain/source voltage of N1 increases. This large voltage difference decreases the gate capacitance of N1.

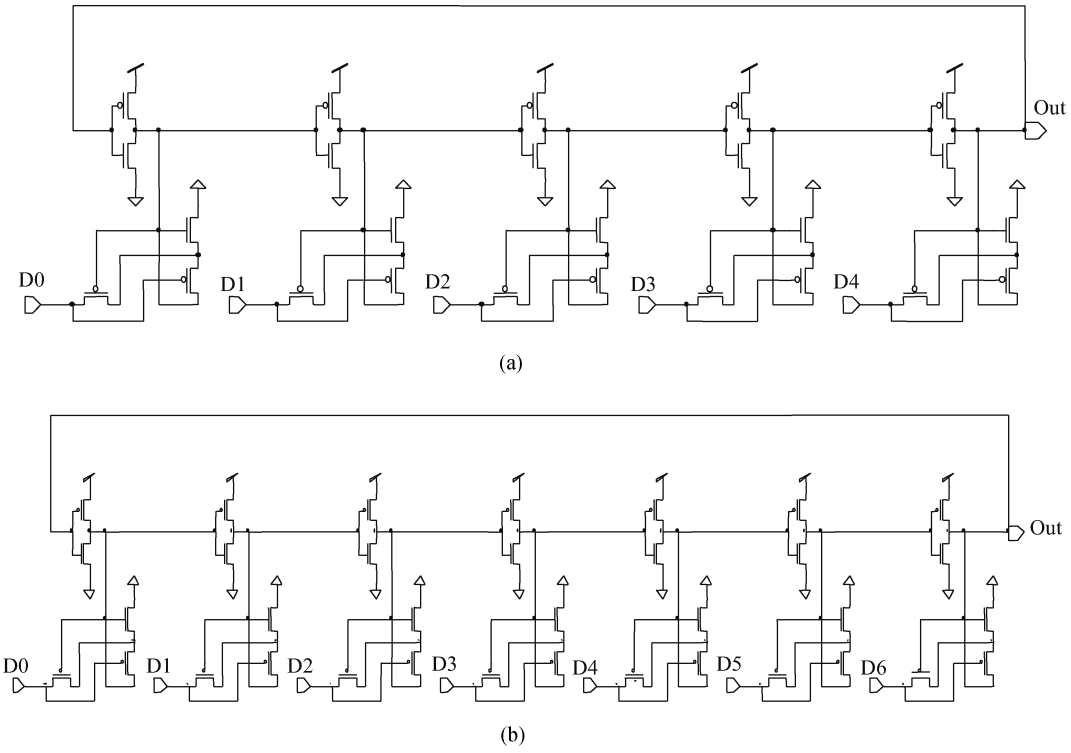

Fig. 5. (a) 5-stage DCO. (b) 7-stage DCO.

Gate capacitance of transistor P2 shows increment as the voltage difference between the gate and source/drain terminal of P2 is reduced with a high D input. Moreover, for transistor P1 the gate capacitance also increases with a high (1) applied control bit (D) because the difference of the gate and source/drain voltage decreases. As the widths of the transistors (P1 and P2) are large, these transistors contribute more to the total load capacitance and contribute to an increase in the load capacitance of the delay cell with a low (0) control bit. With an increase in capacitance, the DCDE delay is increased and subsequently the output frequency decreases. Power consumption shows an upward trend with the application of high control bits, as more current is drawn from the power supply to ground. The total power consumption in any CMOS circuit is given as in Eq. (2).

$$P_{\text{total}} = \alpha C_{\text{L}} V_{\text{dd}}^2 f + I_{\text{sc}} V_{\text{dd}} + I_{\text{sub}} V_{\text{dd}} + I_{\text{gatelleakage}} V_{\text{dd}}. \quad (2)$$

In Eq. (2), α is the switching activity, C_{L} is the capacitance of the load, f is the clock frequency and V_{dd} is the supply voltage. The first two components constitute the dynamic power consumption and the remaining two components give the static power consumption.

The three-transistor XOR gate has no direct connection to a power supply so it provides a power efficient variable capacitance load as compared to conventional four-transistor NAND or NOR gates. This XOR gate is based on pass transistor logics, which have reduced internal capacitance and are suitable for power efficient implementations[15]. When the value of the control bit is 1, transistor P1 is off and provides a large resistance and capacitance, which subsequently increases power consumption. In the second case, when the value of the control bit is 0, the gate capacitive and resistance effects of P1 and P2 are decreased, which subsequently reduces power consumption. Furthermore, during transition of the output signal at node S1, the transistor N1 and P2 goes in ON and OFF conditions accordingly and the subthreshold and gate leakage also contribute to total power dissipation. The leakage power can be attributed mainly to reverse biased p–n junctions, the sub threshold leakage current and the gate leakage components. The leakage current results from substrate injection and sub threshold effects[22]. The reverse biased p–n junction current is the static dissipation due to reverse biased diode leakage between the diffusion regions, wells and substrate. Even when a transistor is in the OFF condition, a weak inversion current still exists. This is known as the subthreshold leakage and is given by:

$$I_{\text{sub}} = \mu_{\text{o}} C_{\text{ox}} \frac{W}{L} V_{\text{T}}^2 \exp \frac{V_{\text{gs}} - V_{\text{th}}}{n V_{\text{T}}} \left(1 - \exp \frac{-V_{\text{ds}}}{V_{\text{T}}}\right), \quad (3)$$

where μ_{o} is mobility, C_{ox} is gate oxide capacitance per unit area, L is the channel length, W is the gate width, V_{gs} and V_{ds} are the gate to source and drain to source voltage, respectively. V_{th} is the threshold voltage, $V_{\text{T}} = \frac{KT}{q}$ is the thermal voltage and n is a technology parameter. Ideally, no current flows through a CMOS transistor when it is in the OFF condition. However, in practice, if there is a potential difference between the source and the drain terminals, a small leakage current flows through the transistor when it is in the OFF condition. The power supply and potential difference in the circuits have the most effect on power consumptions. In the proposed design direct connection to V_{dd} is eliminated in the XOR gate and the design is power efficient as compared to the variable load implemented by conventional gates.

A three-stage DCO based on ring topology using XOR

Table 1. Frequency and power consumption variations for the 3-bit DCO with an XOR delay cell.

Control bits ($D_0D_1D_2$)	Output frequency (GHz)	Power consumption (mW)
000	4.0267	0.3901
100	3.6794	0.4753
110	3.3558	0.5376
111	3.2486	0.6121

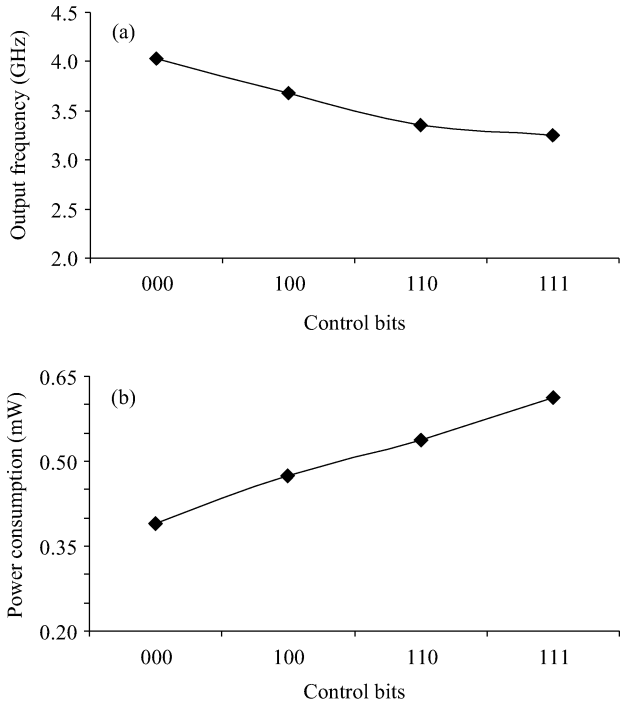

Fig. 6. (a) Output frequency and (b) power consumption for the 3-bit DCO.

gate capacitive loading has been implemented and shown in Fig. 4. Control bits D0–D2 are varied to achieve different output frequency components. Five- and seven-stage DCOs with proposed delay cells have been shown in Figs. 5(a) and 5(b). Five- and seven-bit control words are applied to these DCO circuits to obtain the different frequency components.

3. Results and discussions

Simulations have been carried out using SPICE based on TSMC 0.18 μm technology with a supply voltage of 1.8 V. Table 1 shows the output frequency and power consumption results for 3-bit DCO realized with an XOR delay cell. D_0, D_1 and D_2 bits control the first, second and third stage of the proposed 3 bit controlled DCO. With applied control word '000' all three stage show a change in load capacitance (C_L), as explained in the previous section. The total capacitance of the XOR section decreases, which further affects the total load capacitance (C_L) and the propagation delay also decreases. The output frequency increases with the application of more low control bits, as revealed in Table 1. With a change in control word from 000 to 100 the capacitance of the first delay stage is increased and output frequency shows a falling trend. By

Table 2. Frequency and power consumption variations for the 5-bit DCO with an XOR delay cell.

Control bits ($D_0D_1D_2D_3D_4$)	Output frequency (GHz)	Power consumption (mW)
00000	2.3506	0.6501
10000	2.1691	0.7378
11000	2.0808	0.7979
11100	1.9848	0.8786
11110	1.8795	0.9475
11111	1.8553	1.0202

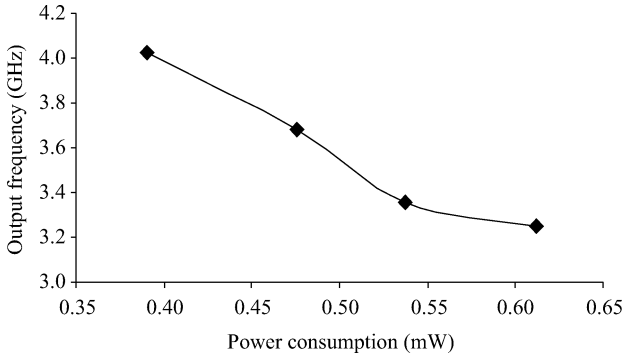

Fig. 7. Power consumption versus output frequency for the 3-bit DCO.

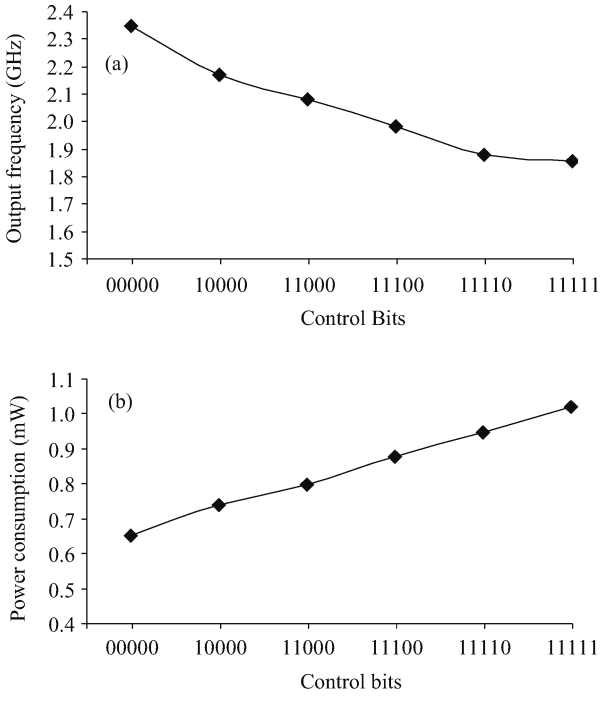

Fig. 8. (a) Output frequency and (b) power consumption for the 5-bit DCO.

having more ones in the control word, the capacitance further increases, which subsequently decreases the output frequency. Due to change in parallel capacitance (ΔC), the delay of a particular stage changes, and this further changes the output frequency as shown in Fig. 6(a). With a change in control word 000–111, power consumption shows the variations as depicted in Fig. 6(b). With the application of more ones (high control

Table 3. Frequency and power consumption variations for the 7-bit DCO with an XOR delay cell.

Control bits ($D_0D_1D_2D_3D_4D_5D_6$)	Output frequency (GHz)	Power consumption (mW)
0000000	1.6817	0.9102
1000000	1.5779	0.9984
1100000	1.5372	1.0583
1110000	1.4792	1.1389
1111000	1.4297	1.2077
1111100	1.3876	1.2851
1111110	1.3367	1.3567
1111111	1.3239	1.4282

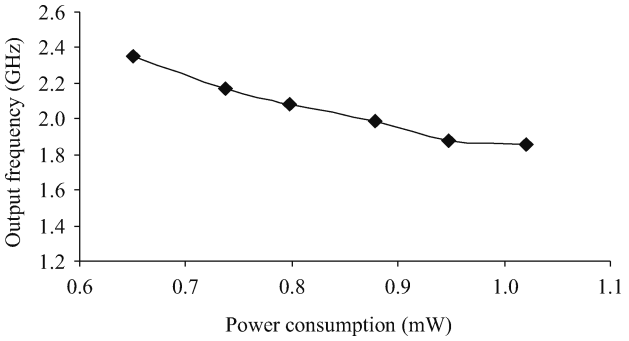

Fig. 9. Power consumption versus output frequency variation for the 5-bit DCO.

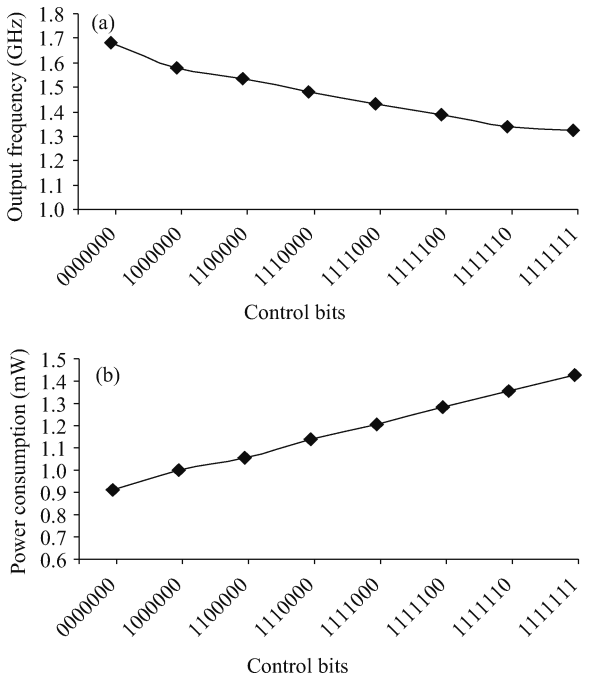

Fig. 10. (a) Output frequency and (b) power consumption for the 7-bit DCO.

bit), the power consumption increases as more current is provided by the supply voltage as compared with the low control (D) input. A power consumption versus output frequency graph for the three-stage DCO is shown in Fig. 7.

Table 2 shows the results for a five-stage DCO designed

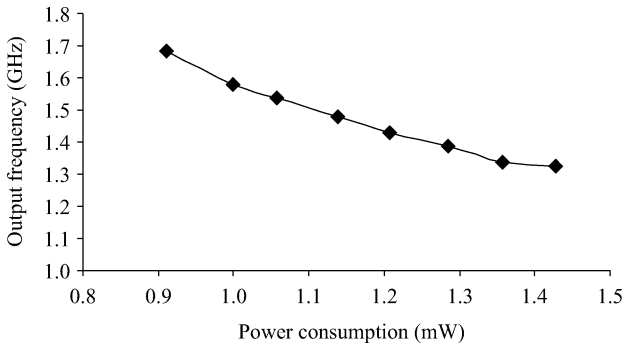

Fig. 11. Power consumption versus output frequency variation for the 7-bit DCO.

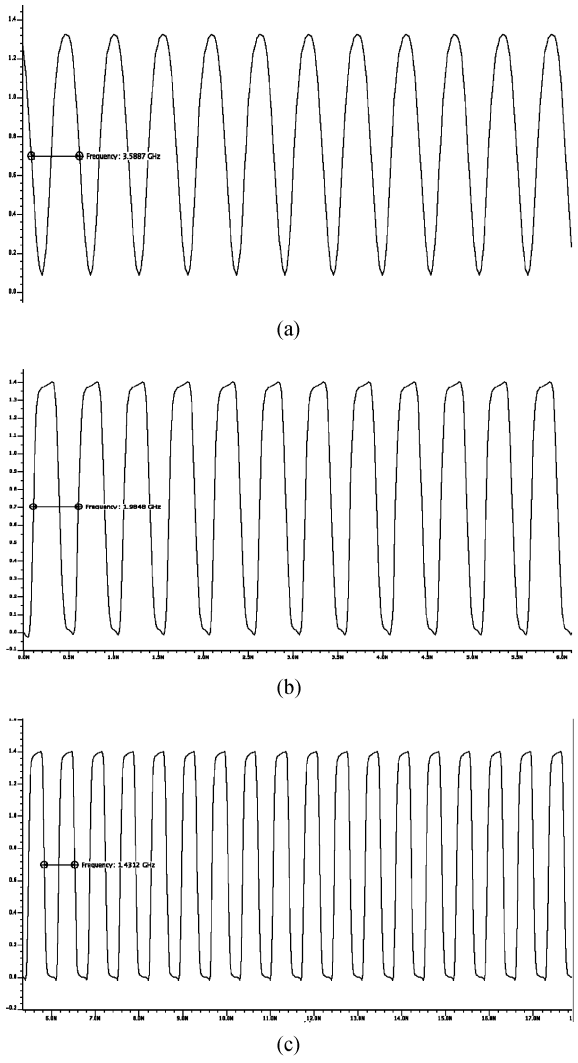

Fig. 12. DCO waveforms for (a) 3 stages with 110, (b) 5 stages with 11100, and (c) 7 stages with 1111000.

with an XOR delay cell controlled by five control bits. The output frequency shows a downward trend with a change in control word from 00000–11111. The output frequency decreases with the addition of more number ones in the control word, as shown in Fig. 8(a). Here, the delay of individual stages increases, which further decreases the output frequency. Power consumption increases with the change in control bits from

Table 4. Comparisons of circuits.

DCO structure	Power consumption (mW)	Output frequency (GHz)	Technology (μm)
Ref. [5]	2.3	0.57–0.85	32 nm
Ref. [7]	2.2	0.57–0.8	32 nm
Ref. [8]	—	1.350–4.550	0.18
Ref. [16]	5.4	0.087–0.25	0.18
Ref. [17]	63.4	0.333–1.472	0.35
Ref. [18]	—	0.750–1.6	0.5
Present work [3 stage 3 bit DCO]	0.6121–0.3901	3.2486–4.0267	0.18
Present work [5 stage 5 bit DCO]	1.0202–0.6501	1.8553– 2.3506	0.18
Present work [7 stage 7 bit DCO]	1.4282– 0.9102	1.3239–1.6817	0.18

00000–11111 as shown in Fig. 8(b). The power consumption versus output frequency graph for a five-stage DCO is shown in Fig. 9.

Table 3 shows the simulation results for a seven-stage DCO controlled with 7 bits. Output frequency and power consumption variations are shown in Figs. 10(a) and 10(b). Power consumption variation with output frequency is shown in Fig. 11.

Output waveforms for 3-, 5- and 7-stage DCOs with control words 110, 11100 and 1111000 are shown in Figs. 12(a), 12(b) and 12(c), respectively.

Table 4 shows a comparison with the simulated results of earlier reported and proposed circuits in terms of power consumption and output frequency. The presented circuits show a better range of output frequency with reduced power consumption. The design reported here is better than the reported design with NAND and NOR based variable capacitive loads as two input gates require four transistors, whereas the present approach requires only three transistors for the XOR gate.

4. Conclusions

Digitally controlled oscillators with two input XOR gates used for variable capacitive loading have been reported. Three-, five- and seven-bit controlled DCO circuits using the proposed delay cell have been simulated with the SPICE simulator. The 3-bit DCO shows an output frequency in the range 3.2486–4.0267 GHz and power consumption 0.6121–0.3901 mW with changing control bits 000–111. The 5-bit DCO provides an output frequency in the range of 1.8553–2.3506 GHz and power consumption in the range of 1.0202–0.6501 mW with varying control bits 00000–11111. Further, the 7-bit DCO gives an output frequency in the range of 1.3239–1.6817 GHz and power consumption in the range of 1.4282–0.9102 mW with changing control bits 0000000–1111111. The reported circuit has a low power consumption and a sufficient output frequency range has been obtained with a reduced transistor count. Output frequency and power consumption results have been compared with earlier reported circuits and the proposed circuit shows significant improvements over prior circuits.

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