# A 3.125-Gb/s inductorless transimpedance amplifier for optical communication in 0.35 $\mu$m CMOS*

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**Abstract:** A 3.125-Gb/s transimpedance amplifier (TIA) for an optical communication system is realized in 0.35 $\mu$m CMOS technology. The proposed TIA employs a regulated cascode configuration as the input stage, and adopts DC-cancellation techniques to stabilize the DC operating point. In addition, noise optimization is processed. The on-wafer measurement results show the transimpedance gain of 54.2 dBΩ and –3 dB bandwidth of 2.31 GHz. The measured average input referred noise current spectral density is about 18.8 pA/$\sqrt{\text{Hz}}$. The measured eye diagram is clear and symmetrical for 2.5-Gb/s and 3.125-Gb/s PRBS. Under a single 3.3-V supply voltage, the TIA consumes only 58.08 mW, including 20 mW from the output buffer. The whole die area is 465 × 435 $\mu$m$^2$.

**Key words:** pre-amplifier; CMOS technology; RGC input stage; DC-cancellation; low power dissipation
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## 1. Introduction

The growing popularity of multimedia applications demands high speed communication systems. The cable communication technology using optical fibers plays a significantly influencing role in modern communication networks. Therefore, the development of high-speed integrated circuits that possess independent IP is of great significance in information construction. The optical receiver is an important part of the optical communication system, and the front-end TIA is a critical element in the optical receiver, affecting the total system performance.

Recently, a number of advanced circuit structures of TIAs have been reported. The work on the TIA presents two trends: resolving the bottleneck of the bandwidth, such as shunt peaking[1], a three-dimensional inductor converter[2], the zero-pole cancellation[3] and active inductor peaking[4]; and optimizing the sensitivity and dynamic range, such as automatic gain control (AGC) technology[5, 6]. A regulated cascode (RGC) stage has been employed to alleviate bandwidth reduction of the TIA due to parasitic capacitance of the photodetector[7]. The RGC stage could extend the bandwidth without a passive inductor, and thus the chip area can be saved well. In this paper, we design a 3.125-Gb/s inductorless transimpedance amplifier, based on low cost 0.35 $\mu$m CMOS technology, utilizing the RGC input stage. In addition, the current generated from the photodetector has an average weight. When the received photocurrent is large, a DC cancellation circuit is also needed to stabilize the DC operating point, improving the dynamic range of the received photocurrent.

## 2. System structure

The transimpedance amplifier converts the received photocurrent to an output voltage, preparing for the further processing of the follow-up circuit. The performance of the optical receiver mainly depends on the TIA's gain, bandwidth, sensitivity and dynamic range. These parameters tend to trade-off with each other, so an optimized design is required. Figure 1 depicts the block diagram of the TIA; the proposed circuit is composed by: RGC_TIA; DC_Cancellation; RC low-pass filter; single to double converter (S2D); and output buffer (BUF). The OTA is an error amplifier. The output buffer provides an output PCML level, and it achieves a good drive to the pads and load.

## 3. Circuit design

### 3.1. RGC transimpedance amplifier

The advanced circuit techniques should be adopted due to the difficulty of designing an ultra-high speed circuit up to 3.125-Gb/s with current 0.35 $\mu$m CMOS technology whose $f_{\text{T}}$ is only 13.5 GHz. Figure 2 shows a schematic of the regulated cascode transimpedance amplifier (RGC_TIA) consisting of a RGC input stage, a gain stage and a buffer.

To optimize the transimpedance gain and bandwidth of the TIA, open the feedback loop of RGC_TIA. Figure 3 is the equivalent small signal circuit, assuming $r_{\text{o2}} \gg R_2$, $r_{\text{o3}} \gg R_3$, $C_1$ is the equivalent capacitance for node 3 to ground. Here, $R'_{\text{f}} = R_1 // \frac{R_{\text{f}}}{1+\alpha_2 g_{\text{m3}} R_3}$, $\alpha_2 = \frac{g_{\text{m2}} R_2}{1+g_{\text{m2}} R_2}$, $C_{\text{T}} = C_{\text{pd}} + C_{\text{gsB}} + C_{\text{sb1}}$, $C_{\text{Z}} = C_{\text{gs1}} + C_{\text{gdB}}$.

As the circuit is more complex, we separate the circuit from point A. Firstly the transfer function $I_{\text{eq}}$ to $I_{\text{in}}$ can be derived as Eq. (1), where $I_{\text{eq}}$ is the short circuit current at point A.

$$\frac{I_{\text{eq}}}{I_{\text{in}}}(s) \approx \frac{1+\dfrac{sC_{\text{B}}}{g_{\text{mB}}}}{\left[1+\dfrac{sC_{\text{T}}}{(1+g_{\text{mB}}R_{\text{BB}})\,g_{\text{m1}}}\right][1+sR_{\text{BB}}(C_{\text{B}}+C_{\text{Z}})]}. \quad (1)$$

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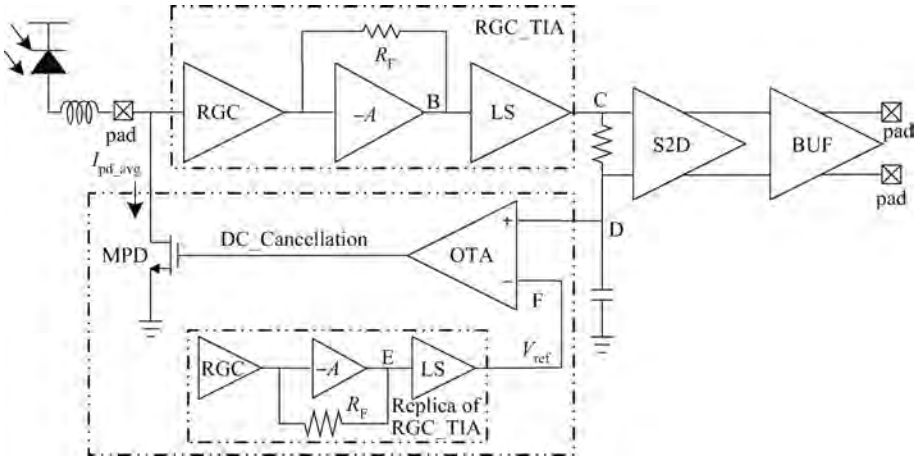


Fig. 1. Block diagram of the transimpedance amplifier.

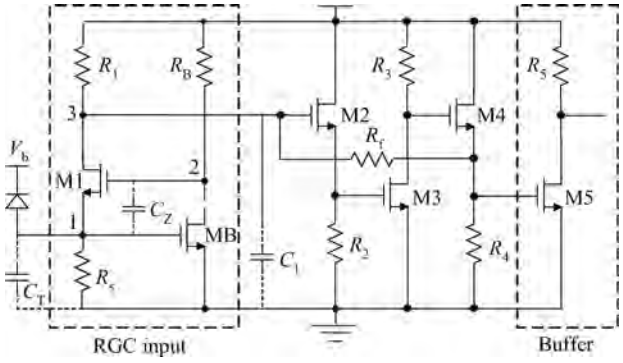


Fig. 2. Schematic of an RGC transimpedance amplifier.

Then we can calculate the transfer function from output voltage $V_{out}$ to $I_{eq}$,

$$\frac{V_{out}}{I_{eq}}(s) \approx \frac{g_{m2}g_{m3}R_2R_3R_f'}{1+g_{m2}R_2}\left(1+\frac{sC_{gs2}}{g_{m2}}\right) \times\left[1+\frac{s(R_f'C_{gs2}+g_{m2}R_2R_f'C_1)}{1+g_{m2}R_2}\right]^{-1} \times\left[1+\frac{s(C_{gs2}+C_{gs3})}{g_{m2}}\right]^{-1}. \quad (2)$$

Multiply Eqs. (1) and (2), and the transfer function of pre-amplifier can be derived as

$$\frac{V_{out}}{I_{in}}(s) = \frac{g_{m2}g_{m3}R_2R_3R_f'}{1+g_{m2}R_2}\left(1+\frac{sC_{gs2}}{g_{m2}}\right)\left(1+\frac{sC_B}{g_{mB}}\right) \times\left\{\left[1+\frac{sC_T}{(1+g_{mB}R_{BB})\,g_{m1}}\right][1+sR_{BB}\,(C_B+C_Z)] \times\left[1+\frac{s(R_f'C_{gs2}+g_{m2}R_2R_f'C_1)}{1+g_{m2}R_2}\right](1+sR_2C_{gs3})\right\}^{-1}. \quad (3)$$

From Eq. (3), we can obtain the transimpedance gain of the RGC_TIA as

$$Z_T(0) = \frac{V_{out}}{I_{in}}(0) = \frac{g_{m2}g_{m3}R_2R_3}{1+g_{m2}R_2}\left(R_1 // \frac{R_f}{1+\alpha_2 g_{m3}R_3}\right). \quad (4)$$

Meanwhile, the main pole of the RGC_TIA can be expressed as

$$\begin{aligned} p_1 &= \frac{1+g_{m2}R_2}{2\pi R_f'(C_{gs2}+g_{m2}R_2C_1)} \\ &= \frac{1}{2\pi R_f'\left(\dfrac{C_{gs2}}{1+g_{m2}R_2}+\alpha_2 C_1\right)} \\ &\approx \frac{1}{2\pi\left(R_1 // \dfrac{R_f}{1+\alpha_2 g_{m3}R_3}\right)(C_{db1}+C_{g2})}. \end{aligned} \quad (5)$$

According to Eqs. (4) and (5), increasing the value of $R_1$ and $R_f$ can effectively improve the transimpedance gain, but large $R_1$ and $R_f$ will cause a low dominant pole, which will reduce the –3 dB bandwidth. If we increase the gain of middle stage $g_{m3}R_3$, the transimpedance gain and –3 dB bandwidth can be increased together, but because the deep sub-micron CMOS technology limits the gain of the single-stage amplifier, so the increasing of $g_{m3}R_3$ is limited. Hence, the compromise among various constraints is necessary to optimize the parameters in the circuit design. Additionally, the RGC stage reduces the input resistance of the TIA, so the input is no longer the main pole, effectively isolating the parasitic capacitance of the photodetector in the bandwidth.

### 3.2. Noise analysis and optimization

Referring to the noise analysis in Ref. [8], neglecting the flicker noise, only considering the resistor and channel thermal noise, the equivalent input noise current spectral density of the TIA is given by

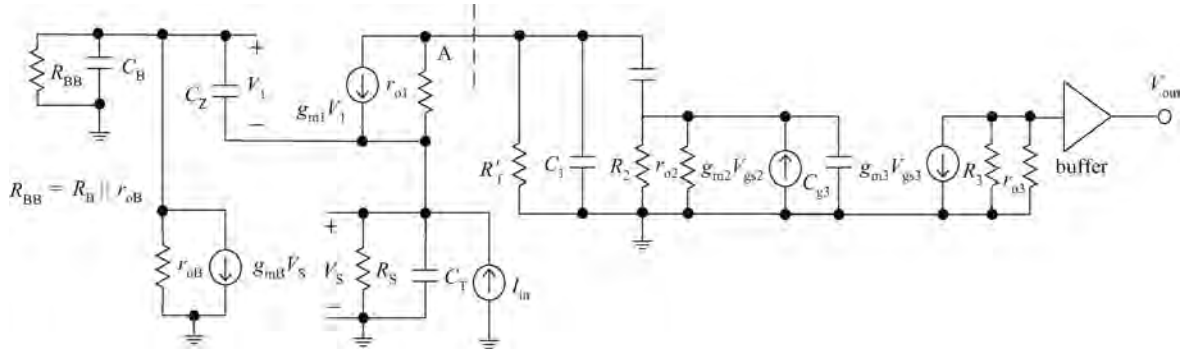


Fig. 3. Equivalent small signal circuit of RGC_TIA.

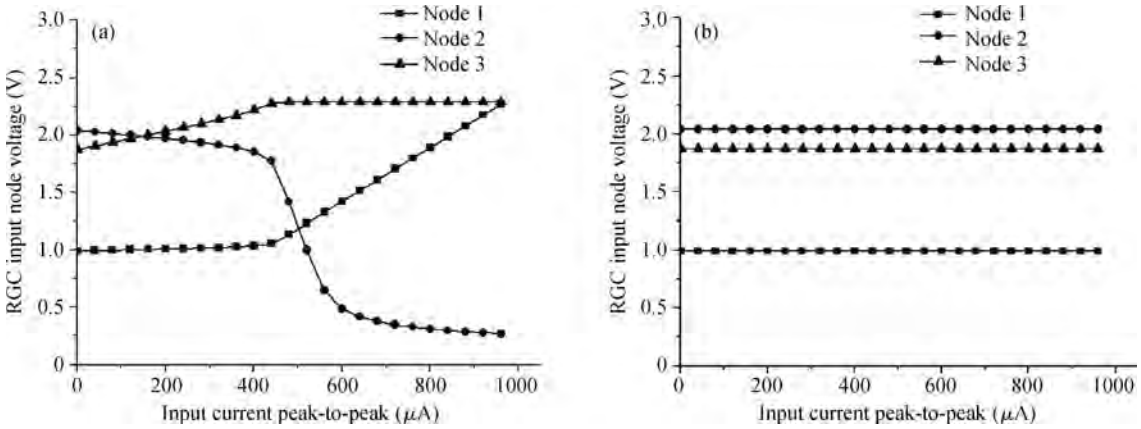


Fig. 4. Node voltage of input stage changes with the photocurrent. (a) Without DC cancellation. (b) With DC cancellation.

$$
\begin{aligned}
I_{\mathrm{n,eq}}^2 \approx\ & I_{\mathrm{S}}^2 + I_{\mathrm{Rf}}^2 + I_{\mathrm{R1}}^2 + \left(\frac{sC_1}{g_{\mathrm{m3}}}\right)^2 (I_{\mathrm{d3}}^2 + I_{\mathrm{R3}}^2) \\
& + \left[\frac{R_{\mathrm{B}}(1+sC_{\mathrm{T}})}{(1+g_{\mathrm{mB}}R_{\mathrm{B}})R_{\mathrm{S}}}\right]^2 I_{\mathrm{B}}^2 \\
& + \left(\frac{sC_{\mathrm{Z}}}{g_{\mathrm{m1}}}\right)^2 (I_{\mathrm{d1}}^2 + I_{\mathrm{Rf}}^2 + I_{\mathrm{R1}}^2) \\
\approx\ & 4kT\left(\frac{1}{R_{\mathrm{S}}} + \frac{1}{R_{\mathrm{f}}} + \frac{1}{R_1}\right) \\
& + \frac{4kT\omega^2(C_{\mathrm{db1}} + C_{\mathrm{gs2}})^2}{g_{\mathrm{m3}}^2}\left(\gamma + \frac{1}{R_3}\right) \\
& + \frac{4kT\omega^2(C_{\mathrm{gs1}} + C_{\mathrm{gdB}})^2}{g_{\mathrm{m1}}^2}\left(\gamma + \frac{1}{R_{\mathrm{f}}} + \frac{1}{R_1}\right) \\
& + \frac{4kTR_{\mathrm{B}}^2\left[1+\omega^2(C_{\mathrm{pd}} + C_{\mathrm{gsB}} + C_{\mathrm{sb1}})^2\right]}{(1+g_{\mathrm{mB}}R_{\mathrm{B}})^2 R_{\mathrm{S}}^2}\left(\gamma + \frac{1}{R_{\mathrm{B}}}\right).
\end{aligned} \tag{6}
$$

To reduce the noise current, $R_{\mathrm{s}}$, $R_{\mathrm{f}}$, $R_1$, $g_{\mathrm{m1}}$ and $g_{\mathrm{m3}}$ should be increased as large as possible, and the size of transistors M1, MB and M2 should be as small as possible to reduce the parasitic capacitance. From Eq. (5), great $R_{\mathrm{f}}$ and $R_1$ will result in bandwidth degeneration. A large value of $g_{\mathrm{m1}}$ and $g_{\mathrm{m3}}$ means that the $W/L$ ratio and current of transistors M1 and M3 should be increased. Hence, a choice of proper $W/L$ and bias current is necessary to optimize the noise performance.

### 3.3. DC-cancellation circuit

When the received photocurrent is large enough, it is possible to change the operating status of the active device on the signal path, so the output waveform experiences pulse width distortion. The DC cancellation circuit will separate the average components from the input current, and reduce the average current injected into the amplifier to zero, thus stabilizing the DC operating point.

We analyze the RGC_TIA in Fig. 2. Without the DC cancellation circuit, the node voltage of the RGC stage changes with the amplitude of the input photocurrent, as shown in Fig. 4(a). When the magnitude of the photocurrent is small, due to the negative feedback, node 1 remains approximately unchanged. The voltage of nodes 2 and 3 changes linearly with increasing photocurrent, so the $V_{\mathrm{ds}}$ of transistor M1 and the $V_{\mathrm{gs}}$ of transistor MB decrease. When the photocurrent increases to a certain extent, the voltage in node 2 causes the transistor M1 cut-off and the transistor MB into the linear region, so the DC voltage of the RGC input stage experiences a large offset, resulting in no output waveform. From Fig. 4(b) we can see that with the DC cancellation circuit, the DC operating point is effectively stable, extending the dynamic range of the input photocurrent.

As shown in Fig. 1, RGC_TIA, Replica_RGC_TIA, OTA and transistor MPD compose a negative feedback loop. The voltage of point F is a DC reference voltage that is independent of the photocurrent, equal to the voltage of the C/D point when there is no photocurrent input. To meet all PVT cases,

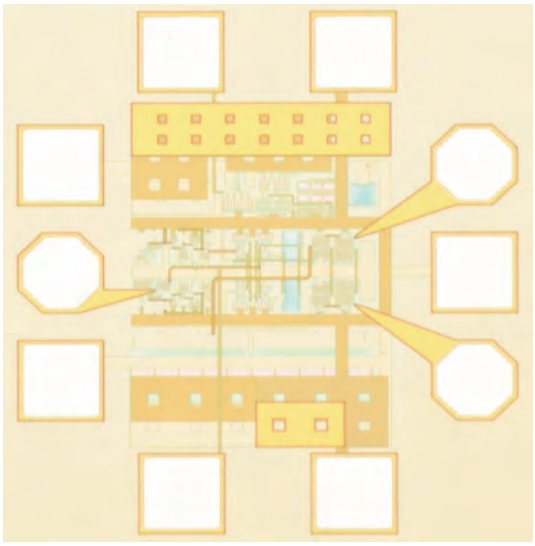

Fig. 5. Chip micrograph of the TIA (0.465 × 0.435 mm$^2$).

Replica_RGC_TIA needs to maintain the same topology with RGC_TIA, as Replica_RGC_TIA only provides a DC reference voltage, and its size could be reduced proportionally to reduce the power consumption.

## 4. Measured results

The TIA is designed and implemented by 0.35 $\mu$m CMOS technology. Figure 5 shows the chip microphotograph of the TIA. The chip with pads occupies an area of 0.465 × 0.435 mm$^2$.

In order to assess the performance of the TIA, on-wafer measurement is carried out. Under a 3.3 V single power supply, the circuit consumes a current of 17.6 mA.

The measured results of eye diagrams are shown in Fig. 6. The peak-to-peak input voltage signal is 10 mV and the signal speed is 2.5 Gb/s and 3.125 Gb/s, respectively. The required $2^{31}$–1 pseudo-random bit sequence (PRBS) is provided by a ROHDE & SCHWARE signal generator and an ADVANTEST D3186 pulse pattern generator. From Fig. 6, under the 2.5 Gb/s and 3.125 Gb/s, the TIA takes on good eye-opening, thinner eyelids and smaller jitter, and the whole eye diagram is clear and symmetrical.

Using an Agilent 8363B network analyzer, we measured the chip without a photodiode on the Cascade 11000 probe station. Figure 7 illustrates the measured $S$-parameters with an input signal power of –55 dBm, and the differential output transimpedance gain of amplitude-frequency characteristic handling of Eq. (7). Figure 7(b) indicates that the differential output transimpedance gain is 54.2 dBΩ, –3 dB bandwidth of 2.31 GHz. The measured results almost coincide with the simulation,

$$Z_{\mathrm{T}} = \frac{2 \times 50 \times S_{21}}{1 - S_{11}}. \tag{7}$$

Figure 8 shows the measured noise figure curve from the Agilent 346C noise source and the Agilent N8975A noise figure analyzer and the handled equivalent input noise current spectral density according to Eq. (8), where $k$ is the Boltzmann

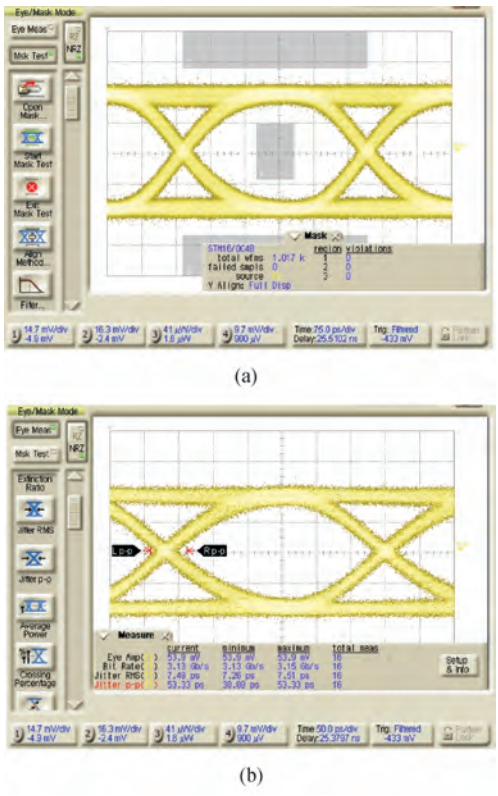

Fig. 6. Measured eye diagrams of the TIA. (a) 2.5 Gb/s, 10 mV PRBS input. (b) 3.125 Gb/s, 10 mV PRBS input.

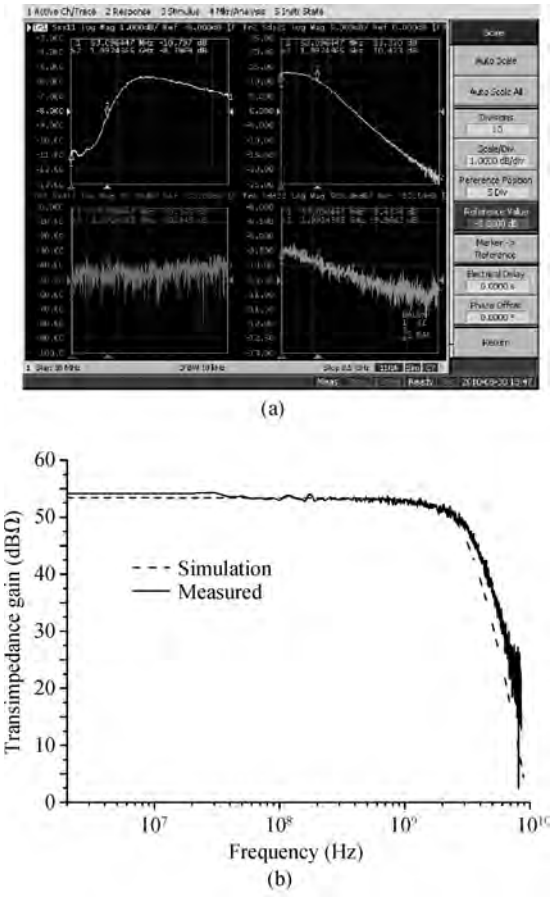


Fig. 7. Frequency characteristic of the TIA. (a) Measured $S$ parameters. (b) Amplitude–frequency characteristic.

Table 1. Summary and performance comparison.

| Parameter | This work | Ref. [9] | Ref. [10] | Ref. [11] | Ref. [12]* | Ref. [13] |
|---|---|---|---|---|---|---|
| Process ($\mu$m) | 0.35 CMOS | 0.35 CMOS | 0.35 CMOS | 0.35 CMOS | 0.18 CMOS | 0.18 CMOS |
| Bandwidth (GHz) | 2.31 | 2 | 1.25 | 2.2 | 2.1 | 4 |
| Speed (Gb/s) | 3.125 | 1 | 1.25 | 2.5 | 3.125 | 5 |
| Gain (dBΩ) | 54.2 | 50 | 55 | 54.5 | 64 | 66d |
| Input-referred noise (pA/$\sqrt{\text{Hz}}$) | 17.0 @ 2.31 GHz | N/A | 16.0 @ 1.25 GHz | N/A | 32.0 | N/A |
| Sensitivity (dBm) | N/A | –11 | –21.0 | –21.2 | –18.0 | –19.0 |
| Power (mW) | 58 | 54 | 260 | 99 | 50 | 24** |
| Voltage (V) | 3.3 | 3.3 | 3.3 | 3.3 | 1.8 | 1.8 |
| $C_{\text{pd}}$ (pF) | 0.5 | N/A | 0.7 | 0.3 | 1.5 | 0.5 |
| Chip area (mm$^2$) | 0.202 | 0.286 | 2.08 | 2.475 | 0.64 | N/A |
| FOM*** | 7.44 | 3.01 | 0.096 | 0.35 | 2.12 | N/A |
| Year | 2010 | 2010 | 2004 | 2006 | 2007 | 2010 |

* Simulation results. ** Not including the output buffer. *** FOM $= \frac{\text{Gain}\times\text{Bandwidth}}{f_{\text{T}}\times\text{Power}\times\text{Area}}$.

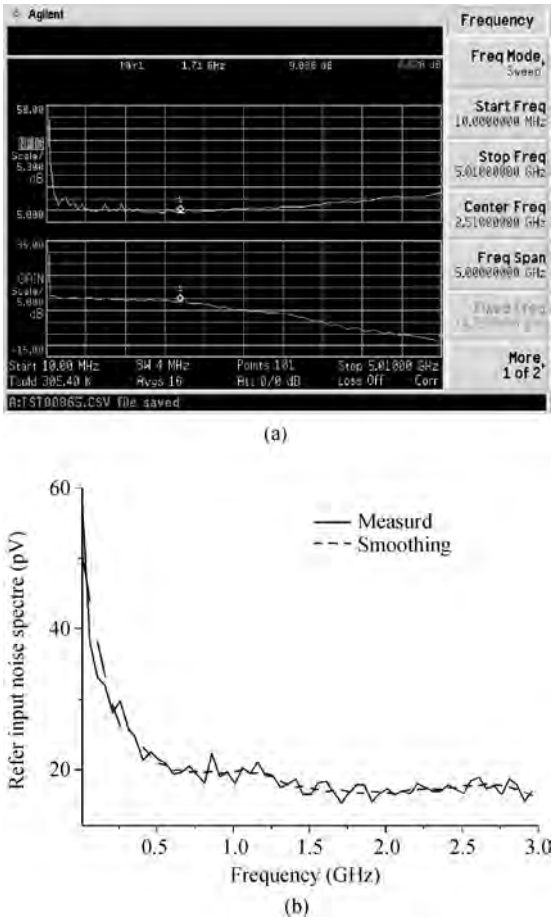


Fig. 8. Noise characteristic of TIA. (a) Measured noise figure. (b) Equivalent input noise current spectral.

constant, $T$ is absolute temperature (assuming room temperature is 300 K), and NF is the noise figure (dB). Figure 8 indicates that the equivalent input noise current spectral density at –3 dB bandwidth is 17.0 pA/$\sqrt{\text{Hz}}$, and the average equivalent input noise current spectral is 18.8 pA/$\sqrt{\text{Hz}}$.

$$\overline{i_{\text{n, eq}}} = \sqrt{4kT \times 50 \left(\frac{1-S_{11}}{100}\right)^2 \left(10^{\text{NF}/10}-1\right)}. \quad (8)$$

## 5. Conclusion

A 3.125-Gb/s inductorless transimpedance amplifier for an optical communication system has been implemented by 0.35 $\mu$m CMOS technology. The RGC input stage effectively extends the bandwidth of the amplifier, and the DC-cancellation circuit offers a stable operating point. The proposed TIA achieves a transimpedance gain of 54.2-dBΩ, a 3-dB bandwidth of 2.31-GHz and an average equivalent input noise current spectral density of 18.8 pA/$\sqrt{\text{Hz}}$. The measured eye diagrams show good characteristics at a 3.125-Gb/s input signal, and total power consumption of 58 mW. The measured results of the optical receiver TIA are compared with those recently published in standard CMOS technology in Table 1. Among the references mentioned in Table 1, using the same 0.35 $\mu$m CMOS technology, the speed rate of the proposed TIA is higher than that of Refs. [9–11]. As the inductorless design, the chip area is less than in Refs. [9–12]. In Table 1, the figure of merit (FOM) is calculated for the state of the optical receiver TIA in CMOS.

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