Characterization of on-chip balun with patterned floating shield in 65 nm CMOS

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Abstract: A simple method of balun synthesis is proposed to estimate the balun structure in the operating frequency band. Then, a careful optimization is implemented to evaluate the estimated structure by a series of EM simulations. In order to investigate the impact of the patterned floating shield (PFS), the optimized baluns with and without PFS are fabricated in a 65 nm 1P6M CMOS process. The measurement results demonstrate that the PFS obviously improves the insertion loss (IL) in the frequency range and a linear improving trend appears smoothly. It is also found that the PFS gradually improves the phase balance as the frequency increases, while it has a very slight influence on the magnitude balance. To characterize the device's intrinsic power transfer ability, we propose a method to obtain the baluns' maximum available gain directly from the measured 3-port S-parameters and find that IL-comparison may not be very objective when evaluating the shielding effect. We also use the resistive coupling efficiency to characterize the shielding effect, and an imbalanced shielding efficiency is found though the PFS is perfectly symmetric in the measurement. It can be demonstrated that this phenomenon comes from the intrinsic imbalance of our balun layout.

Key words: Balun; on-chip; patterned floating shield; passive devices; RFIC; silicon

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1. Introduction

A balun is a component that transforms balanced differential signals to a single-ended signal or vice versa. It has been used extensively in many applications for radio frequency integrated circuits (RFICs), such as double balanced mixers, push-pull amplifiers and frequency doublers.

In our experiment, a center-tapped spiral transformer structure is chosen for the balun design. Like the standard on-chip spiral inductors, our balun suffers from losses in the metal coils as well as in the conductive silicon substrate. The metal loss is mainly caused by the current crowding phenomenon resulting from the skin effect and proximity effect, and its impact can be alleviated by using a thick top metal layer. The lossy silicon substrate dissipates energy in terms of two loss mechanisms, i.e., the eddy current and displacement current losses resulting from the magnetic and electric field, respectively.

To reduce the substrate losses, several techniques have been adopted, such as the high-resistive silicon substrate, micromachining technique and silicon-on-insulator (SOI) structure[1−3]. However, most techniques require additional process steps or special materials. On the other hand, a patterned ground shield (PGS) is introduced between the spiral coil and the silicon to limit the electromagnetic field penetration into the conductive substrate[4]. However, the large parasitic capacitance between PGS and the spiral coil leads to a much lower resonant frequency. Thus, the high frequency application of the device is limited. Meanwhile, it is difficult to implement an on-chip ground reference without any voltage swing. When the shield suffers some voltage variation, energy is again lost to the conductive substrate[5]. In addition, PGS must be designed very carefully, otherwise it may deteriorate the device performance or change the characteristics of the device[6, 7].

Recently, floating shields have been proposed to improve the performance of passive devices, such as on-chip transmission lines, inductors and transformers[5, 6, 8−12]. Most of the research reported in the literature has made an effort to investigate the improvements in transmission lines and inductors[5, 8−11]. To the best of our knowledge, only a few research groups have analyzed the impact of the floating shield on monolithic transformers[6, 12], while investigations into the baluns with floating shields are scarce. Reference [6] showed that the use of floating shields allows a slight improvement without degrading other characteristics of the transformer. In Ref. [12], a resistive coupling efficiency was introduced to serve as the criterion for evaluating substrate shielding. Although our balun design uses the transformer structure, it is more than a simple transformer. Compared with transformers, some figures-of-merit in the balun design are very sensitive (e.g. amplitude imbalance, phase imbalance) and a slight modification of the structure may change them significantly. Therefore, it is important to carry out some investigations into the impact of floating shields on the monolithic balun.

In this paper, a parameterized balun structure is presented and its structure parameters are estimated by a simple method of balun synthesis. Based on the electromagnetic simulations, the estimated balun is optimized carefully for the operating frequency band of 3–8 GHz. Then the optimized baluns with and without PFS are implemented in a 65 nm 1P6M CMOS process. After the parasitic de-embedding procedure, we compare the measured performance in terms of some important figures-of-merit, such as insertion loss, amplitude imbalance and phase imbalance. In order to assess the impact of the floating shield,

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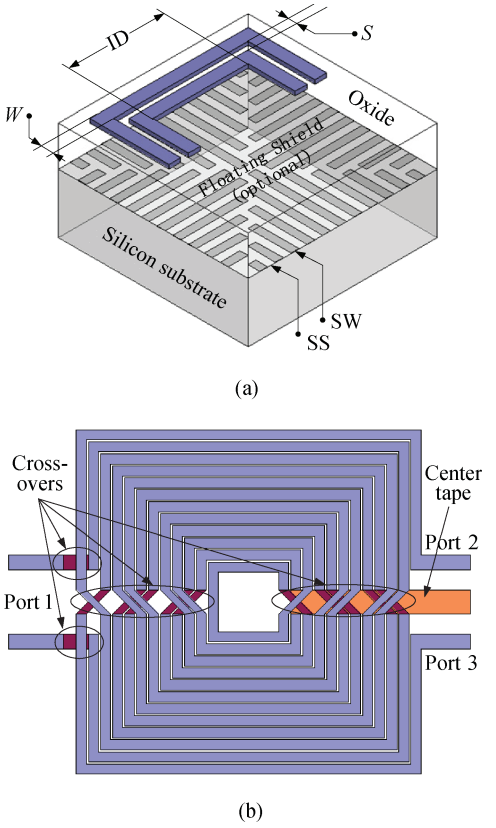


Fig. 1. Balun structure. (a) Cross-sectional view. (b) Top view.

two methods are provided from different aspects.

2. Balun design considerations

2.1. Parameterized balun layout

According to our knowledge, three types of on-chip planar transformer structures can be used to implement the transformer balun, i.e., taped, stacked and interleaved structures[13]. In a taped structure, there is a spatial separation between the primary and secondary coils, leading to the lowest mutual coupling coefficient. Though the stacked configuration can achieve the highest mutual coupling, it suffers from high terminal-to-terminal capacitance or equivalently has a low self-resonant frequency. Moreover, one spiral coil in the stacked structure cannot use the thick top metal, and the use of other thin metal layers will lead to additional losses. Thus, the interleaved configuration with the highest resonant frequency and moderate coupling is employed in our design.

In our balun design (Fig. 1(b)), the thick top metal (M6) is used to implement the primary and secondary coils, while the combination of M5 and M6 forms several X-shaped crossovers. In addition, M4 makes the center tape pass through the crossovers smoothly.

The balun structure, illustrated in Fig. 1(a), is determined by several parameters, including turn ratio (N:N), line spacing (S), line width (W), internal diameter (ID), shield spacing (SS) and shield width (SW). The mutual inductance and capacitance between the primary and secondary coils are proportional to the peripheral length of each winding[14], so the mutual inductance is promoted at the expense of increased coupling capacitance when the number of turns increases. Relatively small spacing between adjacent lines will enhance the magnetic coupling between two coils, but the induced larger capacitance will decrease the self-resonant frequency. Also, there is a trade-off between metal loss and magnetic coupling when selecting the line width: the wider the line width, the smaller the metal loss is, but the weaker the magnetic coupling becomes. In addition, increasing the internal diameter will improve the magnetic coupling because of increased magnetic flux, but a greater chip area will be consumed and the coupling capacitance will also increase.

2.2. Figure-of-merit

There are several figures-of-merit to characterize the balun's electrical performance, e.g. amplitude imbalance, phase imbalance and insertion loss.

According to Ref. [14], the transformers in different configurations (i.e. inverting and non-inverting connections) show different high-frequency responses due to the effect of the inter-winding capacitance. Actually, our balun is the integration of two transformers in different configurations: the primary and one-half of the secondary coils form one transformer, and these two transformers share the same primary part. In addition, the balun layout still shows some slight asymmetry due to the use of multiple crossovers. Therefore, the balun will certainly show some imbalanced behaviors, and we often use the amplitude imbalance (ζ) and phase imbalance (θ) to characterize this phenomenon.

$$\zeta = -20\lg\left|\frac{S_{21}}{S_{31}}\right|, \tag{1}$$

$$\theta = 180 - \left|\arctan\frac{\text{imag}(S_{21})}{\text{real}(S_{21})} - \arctan\frac{\text{imag}(S_{31})}{\text{real}(S_{31})}\right|. \tag{2}$$

When the signal passes through the balun, the device itself dissipates and stores energy. In addition, the phase imbalance at the balanced ports also causes an energy loss. Thus, the insertion loss definition considering both pass loss and phase imbalance loss is given as[15]

$$\begin{aligned}\text{IL} = &-10\lg(|S_{21}|^2 + |S_{31}|^2)\\ &-10\lg\frac{|S_{21}|^2 + |S_{31}|^2 + 2|S_{21}||S_{31}|\cos\theta}{|S_{21}|^2 + |S_{31}|^2 + 2|S_{21}||S_{31}|}.\end{aligned} \tag{3}$$

When the phase imbalance is small, we can get

$$\text{IL} = -10\lg(|S_{21}|^2 + |S_{31}|^2). \tag{4}$$

2.3. EM simulation setup

The electromagnetic (EM) simulation results in our balun design are based on the numerical solver, IE3D. The solver is a full-wave, method-of-moments (MOM) based EM simulator for analyzing and optimizing planar and 3D structures with multilayer dielectrics.

Before EM simulation, a multilayer dielectric environment must be created. However, there are more than 30 dielectric

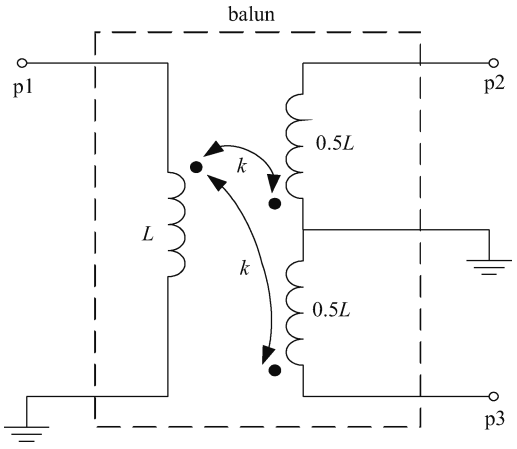


Fig. 2. Simple model for balun.

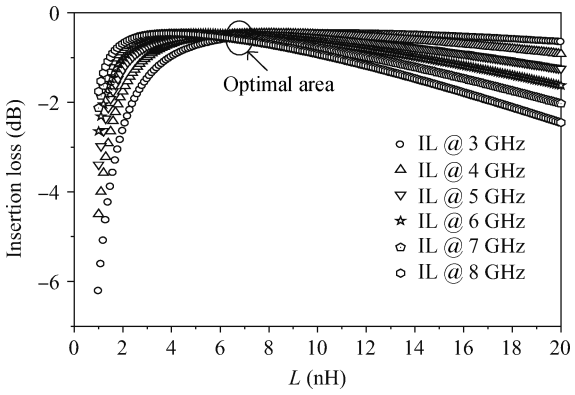


Fig. 3. Insertion loss under different simulation conditions.

layers in the 65 nm 1P6M CMOS process, and setting all layers will slow down the simulation. Thus, we choose to merge the dielectric layers for the simulation efficiency. The merging method is as follows,

$$\varepsilon_{\text{eff}} = \frac{t_1 + t_2 + t_3 \cdots}{t_1/\varepsilon_1 + t_2/\varepsilon_2 + t_3/\varepsilon_3 \cdots}, \tag{5}$$

$$t_{\text{eff}} = t_1 + t_2 + t_3 \cdots , \tag{6}$$

where t_i and ε_i (i=1, 2, 3…) denote the thickness and relative dielectric constant of the i-th layer, respectively. The effective thickness and relative dielectric constant of the merged layer are denoted by t_{eff} and ε_{eff}, respectively.

2.4. Synthesis and optimization of the balun

In the simple balun model illustrated in Fig. 2, we fix the mutual coupling coefficient k as 0.75 for the interleaved balun from our experience. By sweeping the inductance L from 1 to 20 nH in the frequency band 3–8 GHz, we get the insertion loss responses under different simulation conditions in Fig. 3. The narrowest part, which is denoted by "optimal area" in this figure, demonstrates that the inductance in this area will provide the optimal IL response in the operating frequency band. Thus, we estimate that the inductance of the primary or secondary coil is about 7 nH.

In Ref. [16], the planar spiral inductance can be estimated by the monomial expression in the structure parameters. According to the fact that adjacent turns of one coil is isolated by the other coil, the expression in Ref. [16] should be transformed as

$$\begin{aligned} L = {} & \beta\{\text{ID} + 2[W + (N-1)(2W + 2S)]\}^{\alpha_1} W^{\alpha_2} \\ & \times [\text{ID} + W + (N-1)(2W + 2S)]^{\alpha_3} \\ & \times N^{\alpha_4} (W + 2S)^{\alpha_5}, \end{aligned} \tag{7}$$

where β, α_1, α_2, α_3, α_4 and α_5 are the coefficients listed in Ref. [16].

In order to obtain the maximum magnetic coupling, we fix the spacing between adjacent lines to 2 μm (i.e., $S = 2$ μm), which is the minimum spacing of the top metal. Also, the number of turns (N) is set as 6 to obtain the appropriate mutual inductance. In addition, the line width (W) is set as 10 μm to balance the trade-off between the metal loss and the magnetic coupling. Thus, there is only one variable (i.e., ID) in Eq. (7). By solving the equation, we find that the value of ID is about 60 μm.

In order to evaluate the balun synthesis, we implement a series of EM simulations for baluns with different parameters. The results have been summarized in the following table. As shown in Table 1, the estimated design with $N = 6$, $W = 10$ μm, ID = 60 μm and $S = 2$ μm is demonstrated to be the optimal structure for the operating frequencies from 3 to 8 GHz.

2.5. Considerations for PFS

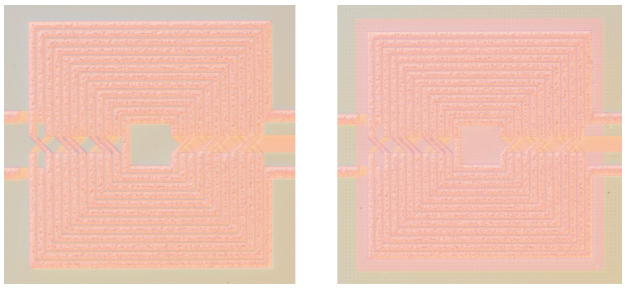
Without requiring an explicit on-chip ground connection, the PFS using M1 is inserted between the spiral coils and the silicon substrate. Since M1 is a good conductor, the shield can be viewed as an electric wall approximately and the tangential component of the electric field is "shorted out" at the surface of the shield. Meanwhile, the normal component of the electric field at the shield surface is determined by the net charge on the shield, while the charge on the shield is induced by the charge of the above balun. Because there is no net charge on the balun, the net charge on the shield will not exist and the normal component of the electric field will vanish at the shield surface. Therefore, the PFS can effectively shield the electric field from penetrating the silicon and reduce the substrate losses.

As illustrated in Fig. 1(a), slots of the shield are designed to cut off the path of the eddy currents, which is induced by the magnetic field. The widths of the strip and slot (i.e. SW and SS in Fig. 1(a), respectively) are designed to be narrow enough to shield the vertical electric field from entering the conductive substrate. In our experiment, we set the parameters as SW = 2 μm, SS = 1 μm.

The addition of PFS with the complex geometry will generate tremendous cells in the meshing step of the EM simulation. And the simulation of the balun with PFS will exhaust the computer resources and be terminated by the solver itself. On the other hand, the main purpose of this paper is to apply PFS to a carefully chosen balun and then do some investigations into the impact of PFS. Therefore, based on the optimized balun structure determined in Section 2.4, a carefully refined PFS is added directly during fabrication.

Table 1. Balun optimization.

N	W (μm)	ID (μm)	IL_{min} (dB @ GHz)	IL_{max} (dB @ GHz)	ζ_{max} (dB @ GHz)	θ_{max} (degree @ GHz)
6	8	60	1.823 @ 3.97	2.252 @ 8	0.086 @ 8	0.27 @ 8
6	10	60	1.536 @ 3.55	2.354 @ 8	0.138 @ 8	0.384 @ 8
6	12	60	1.682 @ 3.22	3.386 @ 8	0.247 @ 8	0.614 @ 8
6	10	50	1.549 @ 3.8	2.149 @ 8	0.118 @ 8	0.378 @ 8
6	10	60	1.536 @ 3.55	2.354 @ 8	0.138 @ 8	0.384 @ 8
6	10	70	1.527 @ 3.34	2.62 @ 8	0.161 @ 8	0.402 @ 8
5	10	60	1.814 @ 5.33	2.162 @ 3	0.049 @ 8	0.113 @ 8
6	10	60	1.536 @ 3.55	2.354 @ 8	0.138 @ 8	0.384 @ 8
7	10	60	1.534 @ 3	8.086 @ 8	0.073 @ 8	0.522 @ 8



(a) (b)

Fig. 4. Micrograph of the balun (a) without PFS and (b) with PFS.

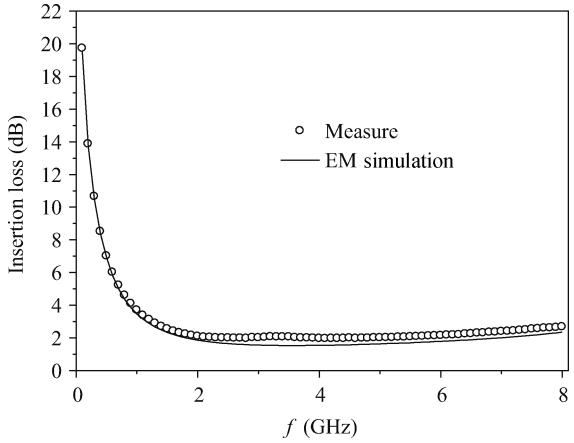


Fig. 5. IL comparison between measurement and simulation.

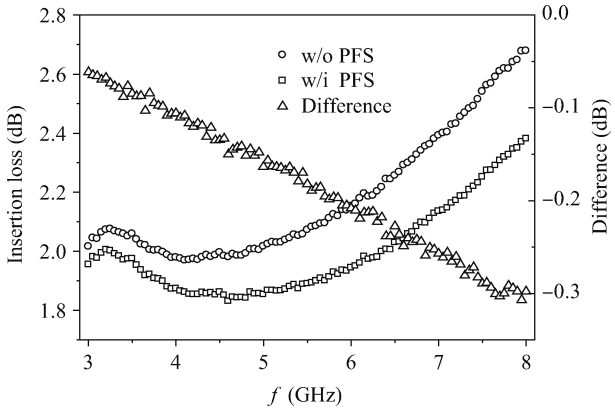


Fig. 6. Insertion loss comparison.

3. Measurement results

The optimized baluns with and without PFS have been fabricated in a 65 nm 1P6M CMOS process with a substrate resistivity of about 10 Ω·cm and a top metal thickness of 3.4 μm. The micrographs of the implemented baluns are shown in Fig. 4, and the 3-port S-parameters were measured using an Agilent E5071B vector network analyzer and RF probes. To characterize the intrinsic balun, the pad parasitics were de-embedded from the measurement using the open and short pad structures.

3.1. Comparison between measurement and EM simulation

In Fig. 5, we compare the measured and simulated insertion loss for the balun without PFS. As demonstrated in this figure, the EM simulation matches the measurement at low frequencies, but deviates from the measurement when the frequency becomes high. This may be due to the fact that the electric and magnetic polarizations in the dielectric and substrate layers are not estimated accurately in the simulation. Because the corresponding loss of polarizations becomes apparent at high frequencies, the simulated and measured IL responses separate when the frequency increases. In the frequency band 3–8 GHz, the IL deviation falls into the range of 0.3–0.5 dB and this can be set as the reference for compensation in the balun design using EM simulations.

As for other figures-of-merit (i.e., amplitude imbalance (ζ) and phase imbalance (θ)), the EM simulation is difficult to estimate their responses accurately. In the frequency band 3–8 GHz, EM simulation shows that $\zeta_{max} = 0.138$ dB and $\theta_{max} = 0.384$ degree, while the measurement shows that $\zeta_{max} = 0.6$ dB and $\theta_{max} = 6.5$ degree. The reason is that these figures-of-merit are very sensitive and a slight imbalance in fabrication or measurement will change them significantly.

3.2. Comparison between baluns with and without PFS in measurement

As demonstrated in Fig. 6, the PFS obviously improves the insertion loss in the operating frequency range. The difference value between the insertion losses with and without the shield is also illustrated in this figure, and shows a linear improving trend as the frequency increases. This is expected due to the fact that the electric and magnetic field leakage to substrate is effectively shielded, particularly at high frequencies. Figure 7 shows that the PFS has a very slight influence on the magnitude balance in the operating frequency band. In Fig. 8, it is

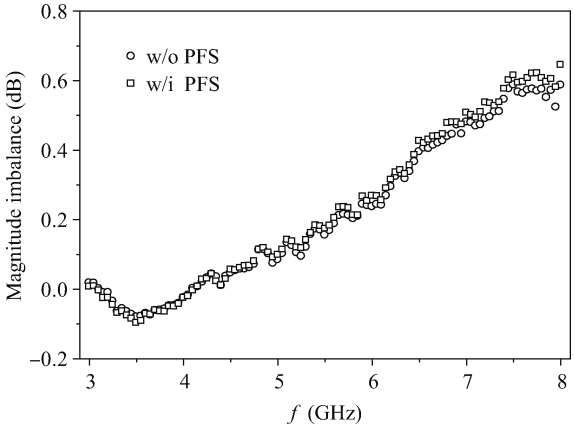


Fig. 7. Magnitude imbalance comparison.

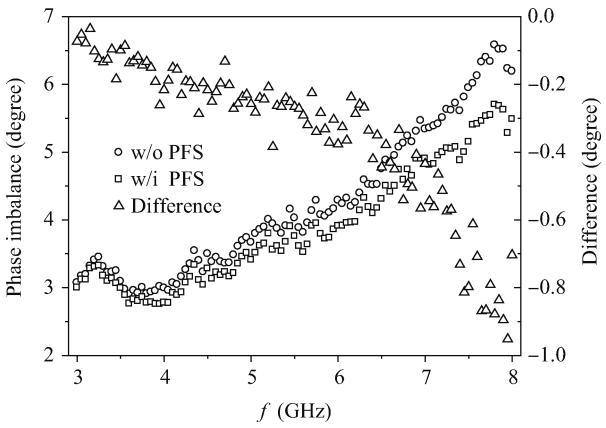


Fig. 8. Phase imbalance comparison.

found that the shield can gradually improve the phase balance as the frequency increases, and the maximum improvement in the frequency band is 1 degree.

4. Two methods to evaluate shielding efficiency

4.1. Maximum available gain

One of the most important figures-of-merit for baluns in circuit applications is the ability of power transfer. The ability is determined not only by the balun itself but also by the source and load impedance, including the corresponding matching network. In other words, the power transfer ability (defined by IL) cannot represent the pure characteristics of the balun device, and this will lead to unfair comparisons between different baluns.

In Ref. [17], the maximum available gain ($G_{\max}$) was introduced to characterize 2-port transformers as

$$G_{\max} = \left|\frac{S_{21}}{S_{12}}\right| (k - \sqrt{k^2 - 1}), \tag{8}$$

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|}, \tag{9}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{10}$$

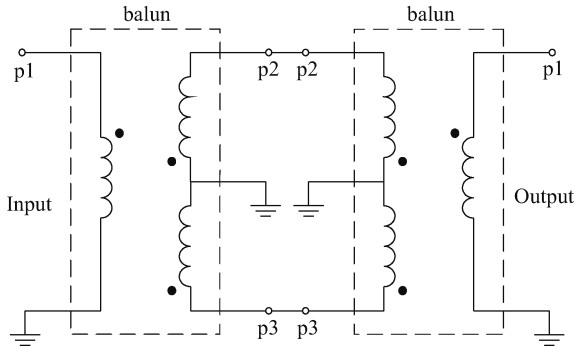


Fig. 9. Back-to-back configuration of two baluns.

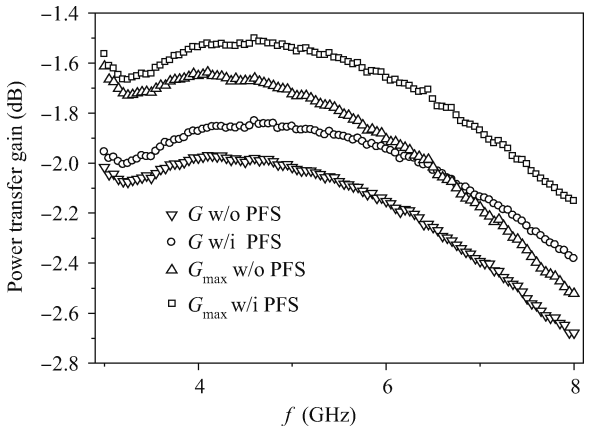


Fig. 10. Power transfer gain.

Although the $G_{\max}$ calculation in terms of measured S-parameters is very convenient, it is only limited to 2-port configurations. Unfortunately, our balun has three ports, so we'd better do some modifications to utilize the 2-port $G_{\max}$. One method is to treat the balun as a transformer by suspending the center tape and connecting the load impedance to balanced terminals. However, this method changes the original balun device itself, and may lead to some behavioral deviations. In addition, the fabricated baluns have already grounded the center tape, so it is impossible to suspend it unless a new structure is fabricated.

As illustrated in Fig. 9, we cascade two 3-port data blocks in a back-to-back configuration, and then we fill the blocks with the same measured S-parameters of one balun. In this configuration, the first balun transforms a single-ended signal to differential signals, while the second one transforms the differential signals back to a single-ended signal again. Thus, the combination of two baluns forms a two-port network and can be used to calculate $G_{\max}$ using Eqs. (8)–(10). In addition, because the signal transfers through the identical balun twice, a factor of 0.5 must be added to $G_{\max}$ (in dB) to assess one balun performance.

To compare the power transfer gain under the measured condition (i.e. $G = 1/\mathrm{IL}$) and ideally matched condition (i.e. $G_{\max}$), we illustrate them in Figs. 10 and 11. As shown in Fig. 10, G or $G_{\max}$ of the balun with PFS is obviously larger than that without PFS. It is also illustrated in this figure that $G_{\max}$ is larger than G by approximately 0.2–0.4 dB, which is

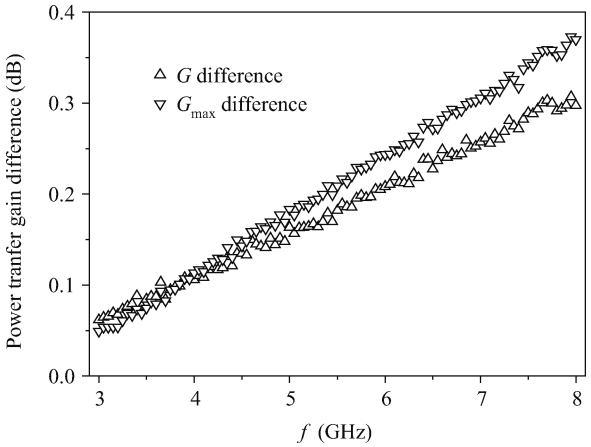


Fig. 11. Power transfer gain difference.

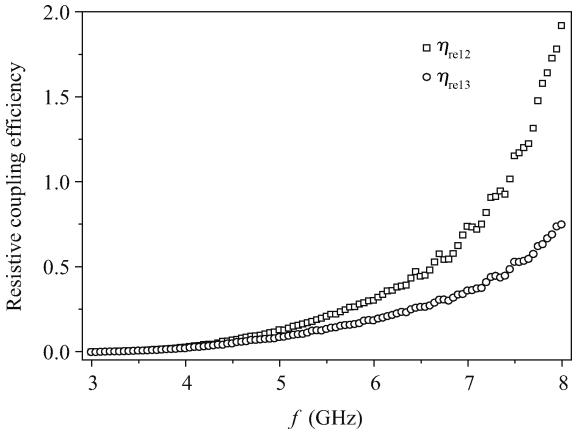


Fig. 12. Resistive coupling efficiency.

due to the fact that the balun is ideally matched for G_{max}. Figure 11 shows the G- or G_{max}-difference between baluns with and without PFS. By setting G_{max}-difference as a reference, we can conclude that G or IL will underestimate the shielding effect from 3.9 to 8 GHz and overestimate the effect from 3 to 3.9 GHz.

4.2. Resistive coupling efficiency

In order to give a clear insight into the effectiveness of the shielding for transformers, Reference [12] introduced the resistive coupling efficiency η_{re} as

$$\eta_{re} = \frac{k_{re} - k_{re(shield)}}{k_{re}} \times 100\%, \tag{11}$$

$$k_{re} = \frac{\mathrm{Re}(Z_{12})}{\sqrt{\mathrm{Re}(Z_{11})\mathrm{Re}(Z_{22})}}. \tag{12}$$

As reported in Ref. [12], k_{re} accounts for hybrid effects of parasitic capacitances and eddy currents in the substrate. The lower the k_{re}, the less substrate effect the transformer has. The relative variation of k_{re} between transformers with and without shields (i.e. η_{re}) can indicate the shielding performance. $\eta_{re} > 0$ indicates the improved shielding effect, while $\eta_{re} < 0$ indicates the degraded shielding effect. Since the balun can be viewed as the integration of two transformers in different configurations (i.e. inverting and non-inverting connections), we get the resistive coupling efficiencies η_{re1j} for both transformers ($j = 2$, 3) as

$$\eta_{re1j} = \frac{k_{re1j} - k_{re1j(shield)}}{k_{re1j}} \times 100\%, \tag{13}$$

$$k_{re1j} = \frac{(-1)^{j+1}\mathrm{Re}(Z_{1j})}{\sqrt{\mathrm{Re}(Z_{11})\mathrm{Re}(Z_{jj})}}. \tag{14}$$

As shown in Fig. 12, the value of η_{re12} and η_{re13} increases as the frequency increases. This indicates an improved shielding effect at high frequencies. It is due to the fact that the skin depth of the shield decreases as the frequency increases, thus less electric and magnetic field can penetrate the shield into the lossy substrate. In addition, we note that η_{re12} is gradually larger than η_{re13} as the frequency increases, which means that

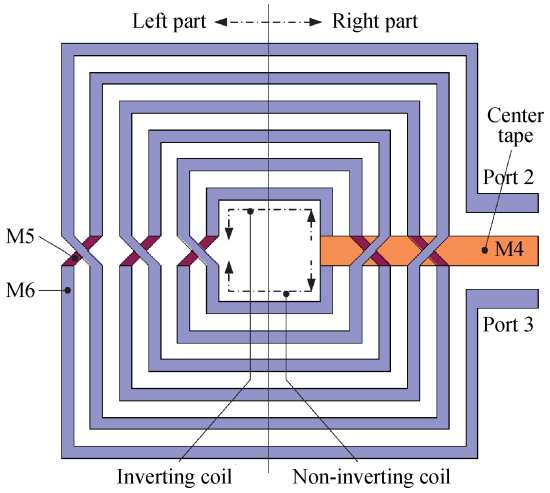


Fig. 13. Secondary coil of balun.

the shielding effect is more efficient for the inverting configuration than for the non-inverting configuration. This imbalanced shielding efficiency may actually compensate the imbalanced behavior of the balun, and this compensation is more apparent in the phase balance improvement, which has already been demonstrated in the measurement results.

Actually, this imbalanced shielding phenomenon comes from the intrinsic imbalance of our balun layout. In Fig. 13, the secondary coil of the balun is shown to evaluate the balun's imbalance and the primary coil is hidden for clearness. As demonstrated in this figure, the main spirals of the inverting and non-inverting coils are designed to be absolutely symmetric, so the imbalance can only be attributed to the crossovers. The crossovers in the right part are naturally shielded from the substrate by the center tape connecting to ground. In the left part, 3 crossovers consisting of 6 connecting bridges are exposed above the substrate. Among them, 3 higher bridges (M6) belong to the inverting coil and 3 lower ones (M5) belong to the non-inverting coil. When the frequency is low, the corresponding wavelength of the electromagnetic wave is much larger than the distances between the bridges and PFS, and the shielding effect is very weak for both inverting and non-inverting configurations. Consequently, η_{re12} and η_{re13} in Fig. 12 are almost the same at low frequencies. When the frequency

increases, the wavelength is gradually comparable to the distances and the imbalance becomes apparent. The lower bridge with smaller distance from PFS will show a weaker shielding effect, because more power will penetrate PFS through the slots of the shield. Therefore, the inverting configuration with 3 exposed higher bridges will have a higher shielding efficiency at high frequencies, which is demonstrated in Fig. 12.

5. Conclusion

A simple method of balun synthesis is proposed to estimate the balun structure. Based on EM simulations, the estimated balun is optimized in the operating frequency range. The optimized baluns with and without PFS are fabricated in a 65 nm 1P6M CMOS process. The measurement results demonstrate that the PFS gradually improves the insertion loss and the phase balance as the frequency increases, while it has a very slight influence on the magnitude balance. In addition, two methods are provided from different aspects to evaluate the impact of PFS.

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