A high-performance MUX-direct digital frequency synthesizer with quarter ROMs

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Abstract: This paper presents a detailed description of a high-performance direct digital frequency synthesizer (DDFS) using optimized quarter ROMs. To improve the working frequency and spectral purity, an original quarter ROMs structure in 0.13 μm CMOS is brought forward and implemented. The working frequency is increased by 40% compared with Yuan Ling's method[1] of implementing a segmented DAC based DDFS. It has been implemented in 0.13 μm CMOS technology. The DDFS has a resolution of 10 bits with a measured SFDR 54 dBc. Its maximum operating frequency is 1.2 GHz by using six pipelining stages. Analytical investigation of improving spectral performances by using dual-slope approximation and pipeline is also presented.

Key words: MUX-direct digital frequency synthesizers; quarter ROMs; dual-slope approximation
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1. Introduction

Direct digital frequency synthesizers (DDFS) are able to generate single-phase or modulated sinusoids with frequency resolution in the sub-hertz range, good spectral purity, very fast frequency switching and phase continuity on switching[2]. Owing to their unique characteristics, DDFS technology plays an important role in modern communication systems (including spread spectrum and frequency hopping systems), in measurement instrumentation, in radar and in electronic warfare systems. The basic DDFS architecture was firstly introduced by Tierney in 1971[3].

The parameter which properly characterizes the DDFS spectral purity is the spurious-free dynamic range (SFDR), defined as the ratio of the amplitude of the desired frequency component to that of the largest undesired frequency component. The most critical block in a DDFS is the sine/cosine generator, which limits operating frequency and is the main source of power dissipation. A number of techniques for phase to sine/cosine amplitude conversion have been published[4−6]. These techniques can be subdivided in three categories: (1) look-up table-based approaches[4]; (2) angle-rotation algorithms[5]; (3) polynomial interpolation techniques[6].

In this paper, a new high-performance MUX-DDFS using quarter-ROMs is proposed. The MUX-DDFS means that a MUX block is used to select coarse amplitude and fine amplitude as the outputs of the DDFS structure.

2. DDFS architecture

Figure 1 shows a simplified schematic of a DDFS. The phase accumulator is an overflowing f-bit accumulator that produces a digital sweep with a slope imposed by the frequency control word (FCW). The most significant bits are input of the sine/cosine generator, which computes sine and cosine functions with high speed and accuracy. Analog outputs, when required, are generated by DACs. The frequency of output sine wave signals is proportional to the frequency control word.

$$F_{\text{out}} = \frac{\text{FCW}}{2^f} f_{\text{clk}}, \quad 0 \leqslant \text{FCW} \leqslant 2^{f-1}, \tag{1}$$

where f_{clk} is the clock frequency.

Figure 2 shows the structure of a MUX-DDFS system based on the quarter ROMs: on one hand, to reduce the complexity of high-frequency circuit, a quarter ROMs structure is implemented; on the other hand, to obtain 1.2 GHz operating frequency, a modified pipeline structure using new switching schemes was developed. The goal of this work is to obtain good harmonic performance even at high frequencies. With correct synchronization, quarter ROMs would be a good method to improve the working frequency. Therefore the traditional look up table is divided into ROMs and a selector.

As we know, the sine/cosine generator section has a most complexity in the system, its limitation of working frequency should be the size of the quarter ROMs, system-level analysis led the customer to request 10-bit resolution and excellent INL and DNL. Secondary specification parameters were the chip die area and total power consumption.

A wide-bits phase accumulator is often used in DDFS for the fine frequency resolution at high clock frequency, and the wide-bits accumulator cannot finish one adding operation in a short single clock period because of the delay caused by the carry bits propagating through the adder. Every new frequency input word is moved into the pipeline circuit. The circuit con-

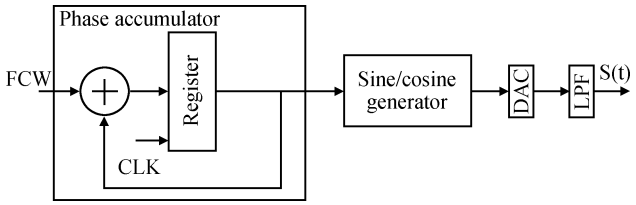

Fig. 1. Schematic of a traditional DDFS system.

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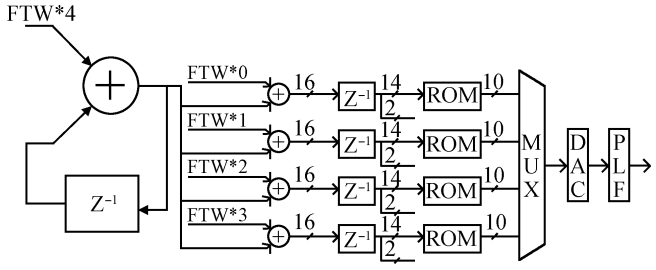


Fig. 2. DDFS system with quarter ROMs.

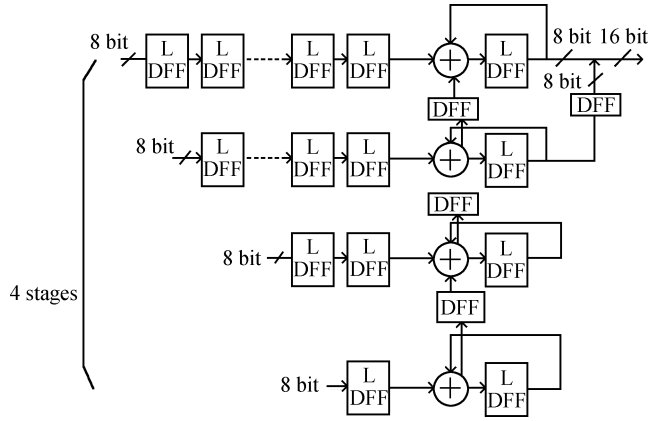


Fig. 3. Architecture of the pipelined accumulator in this work.

sists of D-flip-flops (DFFs) and delay elements. The speed of the accumulator based on this architecture can be increased up to m times, where m is the number of stages of the accumulator pipelined. The accumulator in this work is set as 4 stages of 8 bits each, as shown in Fig. 3. Compared with Yuan Ling's method of implementing a segmented nonlinear DAC, it may improve the working frequency distinctly.

3. Quarter ROMs schemes

The 4 : 1 integrated MUX of the MUX-DDFS offers the users the capability to apply an input data rate 4 times lower than the effective sampling frequency provided by:

$$\text{Data\_rate} = f_{\text{CLK\_SYNC}}/4 = f_{\text{CLK}}, \tag{2}$$

where f_{CLK} is the frequency of data ready clock, since this input MUX is not programmable, all 4 ports have to be used for proper operation of the DAC. Figure 4 shows the internal structure of the sine block. In order to ensure the validity of the digital system, a group of integrated ROMs are set into it. The full-period sine wave can be reconstructed with only a quarter of the sine information by exploiting the quarter-wave symmetry of the sine function. The first step toward the reduction of sine/cosine generator complexity consists in truncating the least significant bits (LSBs) from the phase accumulator. This introduces spurious noise into the DDFS outputs. This noise should be careful taken into account in the design phase. Other conventional approaches always used to simplify the sine/cosine generator are the quadrant symmetry of trigonometric functions and trigonometric identities.

For MUX-DDFSs, sine calculation for phase angles belonging to the first quadrant is required. To reduce the ROM

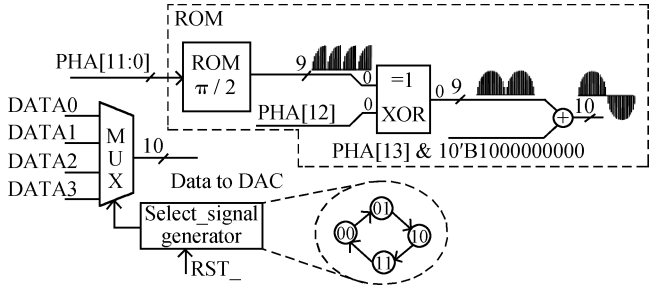


Fig. 4. Quarter ROM structure.

size, the Sunderland technique based on simple trigonometric identities is used in this work. As shown in Fig. 4, although this introduces the 1/2 least significant bit (LSB) offsets to the output. ROM size can be reduced significantly. The phase of a quarter of a sine wave is decomposed to the most significant bits (MSBs), the middle bits, and the least significant bits (LSBs). The sine function can be expressed as follows:

$$\sin(\alpha + \beta + \gamma) = \sin(\alpha + \beta)\cos\gamma + \cos(\alpha + \beta)\sin\gamma + \cos\alpha\sin\gamma. \tag{3}$$

The most significant two phase bits are used to decode the quadrant, while the remaining 14 bits are used for the one-quadrant phase to sin amplitude converter. They are divided into three bit slices: α, β, and γ, having 4, 6, and 4 bits, respectively. Now Equation (3) can be rewritten as follows:

$$A_{\text{mpc}} = \sin(\alpha + \beta) = \sum \text{si}(\alpha)\text{ci}(\beta), \tag{4}$$

$$A_{\text{mpf}} = \cos\alpha\sin\gamma \approx \sum \text{si}(\alpha)\text{fi}(\gamma). \tag{5}$$

α is used to generate signals si(α) and control two blocks: input latch and MUX. The block of Input Latch is used as power gating block to hold or pass the data of β, γ, and 2 MSBs to one of eight phase to amplitude generator logic blocks. In every clock cycle, β, γ, and 2 MSBs are used as inputs of one phase to amplitude converter logic block only, and the inputs of other phase to amplitude converter logic blocks are unchanged and no dynamic power is consumed. Yang *et al.*[7] proposed that minimizing the mean-square error provides the lowest total spur energy and minimizing the maximum absolute error tends to reduce the value of the greatest spurs. To improve the SFDR performance, 2 MSBs are introduced to the one-quadrant phase to sine amplitude converter to reduce the error resulting from 1's complement approximation, which is used to determine whether the sine amplitude is increasing or decreasing. Equation (5) is rewritten as

$$A_{\text{mpf}} = \cos\alpha\sin\gamma \approx \text{si}(\alpha)\text{fi}(\gamma, 2\,\text{MSB}), \quad i = 1, 2, \cdots, 8, \tag{6}$$

where fi(γ, 2MSB) is 2 MSBs and γ together generate fine amplitude. Sine-phase difference algorithm has been introduced to compress the amplitude of the coarse ROM table by storing difference ($\sin\frac{\pi\varphi}{2} - \varphi$) instead of the sine term. But, this method requires an additional adder. The ROM $\pi/2$ is also decreased by QLA (quad line approximation) technique and pipelined. With such structure, we have limited the scale of high speed circuits as much as possible.

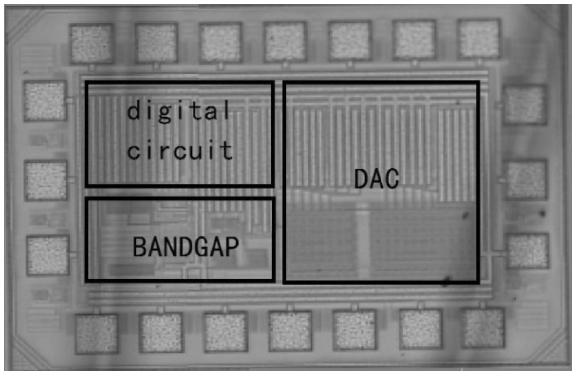


Fig. 5. Micro-photo of the MUX-DDFS chip.

The QLA waveform is used to approximate the sine-phase difference, which is calculated with following four expressions.

$$\mathrm{qla}(\alpha+\beta)=\frac{\alpha+\beta}{2^{j-1}},\quad 0<\frac{\alpha+\beta}{2^{j-1}}<\frac{1}{8}, \tag{7}$$

$$\mathrm{qla}(\alpha+\beta)=\frac{1}{16}+\frac{\alpha+\beta}{2^{j}},\quad \frac{1}{8}<\frac{\alpha+\beta}{2^{j-1}}<\frac{1}{4}, \tag{8}$$

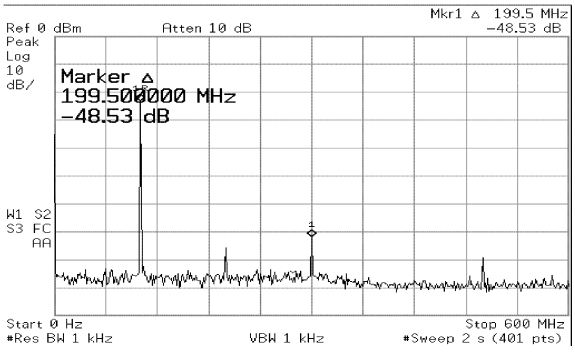
$$\mathrm{qla}(\alpha+\beta)=\frac{1}{4}+\frac{1}{16}+\frac{\alpha+\beta}{2^{j}},\quad \frac{1}{4}<\frac{\alpha+\beta}{2^{j}}<\frac{3}{8}, \tag{9}$$

$$\mathrm{qla}(\alpha+\beta)=\frac{1}{2}-\frac{1}{16}+\frac{\alpha+\beta}{2^{j-1}},\quad \frac{3}{8}<\frac{\alpha+\beta}{2^{j}}<\frac{1}{2}. \tag{10}$$

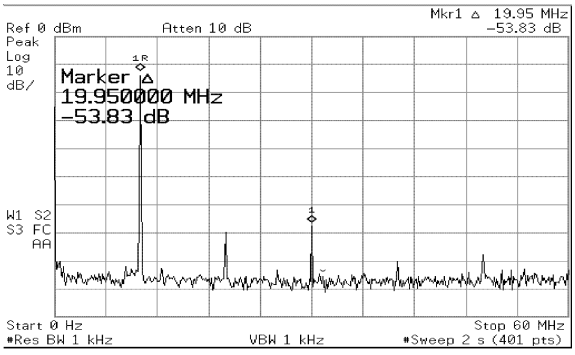
The data for $0<\frac{\alpha+\beta}{2^{j-1}}<\frac{1}{8}$ are generated through shifting down the phase $(\alpha+\beta)/2^{j-2}$ by 1 bit. The data for $\frac{1}{8}<\frac{\alpha+\beta}{2^{j-1}}<\frac{1}{4}$ are generated through shifting down the phase $(\alpha+\beta)/2^{j-1}$ by 2 bits and by changing the first and second MSBs of the phase to "10". The data for $0<\frac{\alpha+\beta}{2^{j-1}}<1/2$ are symmetric[8]. A complementor is needed to reconstruct the symmetric waveform. Two bits of word length can be saved.

$$\mathrm{cr}(\alpha+\beta)=y(\alpha+\beta)-\mathrm{qla}(\alpha+\beta), \tag{11}$$

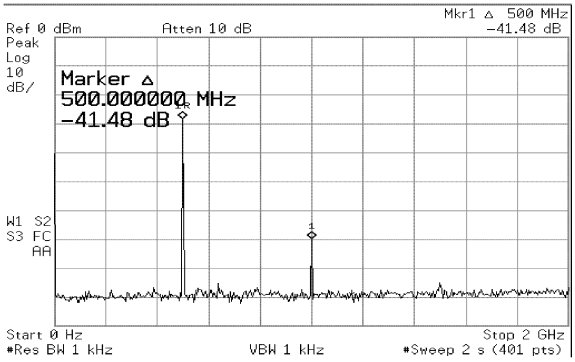
$$\max[\mathrm{cr}(\alpha+\beta)]\approx 0.26\max[y(\alpha+\beta)]. \tag{12}$$



(a)



(b)



(c)

Fig. 6. Output spectra. (a) $f_{\mathrm{out}}=199.5$ MHz @ 1.2 GHz. (b) $f_{\mathrm{out}}=19.95$ MHz @ 1.2 GHz. (c) $f_{\mathrm{out}}=500$ MHz @ 1.2 GHz.

4. Implementation

The chip is implemented in a 1-poly, 8-metal 130 nm CMOS technology, and occupies an active area of 0.33 × 0.66 mm^2 (core area). The micro-photo of the chip is shown in Fig. 5. It includes 3 blocks including digital circuit, BANDGAP and DAC blocks. The DAC core is placed in a separate array to avoid coupling from the digital signals to the current sources. A clock driver is used between the input differential clock pads. The system clock is amplified by the clock driver in the chip. With modern EDA tools, the clock-tree is carefully built to ensure an acceptable clock skew, the maximal delay of the metal wire in chip is about 50 ps.

5. Measurement result

The MUX-DDFS has been measured at a single power supply of 1.2 V and the maximum output current for a pair of 100 Ω termination resister is 5 mA to obtain the maximum single-ended analog output voltage of 0.5 V. The power consumption for the DDFS is about 34 mW. The supply voltage can vary from 0.9 to 1.5 V. Its operating frequency is 1.2 GHz. Figure 6(a) shows the measured spectrum at 199.5 MHz output frequency, while the input clock frequency is 1.2 GHz. The measured spectrum at 19.95 MHz and 500 MHz output frequencies are presented in Figs. 6(b) and 6(c). It can be seen that the wideband spurious free dynamic range (SFDR) of the DDFS is 54 dB, and the narrowband SFDR is about 75 dB.

Table 1 shows the parameters and the performances of optimized MUX-DDFS circuits implemented using the techniques presented in previous sections. Timing and power dissipation performances have been obtained by simulations with the inclusion of parasitic. A Monte Carlo approach with random tuning word and accurate switch-level simulation was used to evaluate power dissipation.

Table 1. Comparison between different reported DDFSs.

Parameter	Ref. [1]	Ref. [8]	Ref. [9]	This work
Power voltage (V)	3.3	3.3	1.2	1.2
Technology	CMOS 350 nm	CMOS 350 nm	CMOS 130 nm	CMOS 130 nm
Active area (mm^2)	5	1.6	0.008	0.22
SFDR (dBc)	50	55	50	54
Max clock freq (MHz)	850	NA	50	1200
Phase resolution (bit)	32	16	NA	32
Amp resolution (bit)	10	10	9	10
Power efficiency (mW/GHz)	470	NA	8	33

6. Conclusion

The paper presents the design of a 1.2 V 10-bit 1.2 GHz CMOS MUX-direct digital frequency synthesizer. In order to improve the working frequency and spectral purity of the synthesizer, an original quarter ROMs structure was brought forward. The maximum operating frequency is 1.2 GHz at room temperature and 1.4 GHz at 0 ℃. Its wideband and narrowband SFDR is about 54 dBc and 75 dBc. The synthesizer implemented in TSMC 0.13 μm CMOS technology was fabricated. The chip die area was 0.218 mm^2, and the total power consumption was about less than 50 mW with 1.2 V power supply. As Table 1 summarized, comparing with other reported DDFSs, this work shows better spectral purity and higher working frequency with controllable active area and power consumption.

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