A passive UHF RFID tag chip with a dual-resolution temperature sensor in a 0.18 μm standard CMOS process*

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Abstract: This paper presents a passive EPC Gen-2 UHF RFID tag chip with a dual-resolution temperature sensor. The chip tag integrates a temperature sensor, an RF/analog front-end circuit, an NVM memory and a digital baseband in a standard CMOS process. The sensor with a low power sigma–delta ($\Sigma\Delta$) ADC is designed to operate in low and high resolution modes. It can not only achieve the target accuracy but also reduce the power consumption and the sensing time. A CMOS-only RF rectifier and a single-poly non-volatile memory (NVM) are designed to realize a low cost tag chip. The 192-bit-NVM tag chip with an area of 1 mm^2 is implemented in a 0.18-μm standard CMOS process. The sensitivity of the tag is –10.7 dBm/–8.4 dBm when the sensor is disabled/enabled. It achieves a maximum reading/sensing distance of 4 m/3.1 m at 2 W EIRP. The inaccuracy of the sensor is –0.6 ℃/0.5 ℃ (–1.0 ℃/1.2 ℃) in the operating range from 5 to 15 ℃ in high resolution mode (–30 to 50 ℃ in low resolution mode). The resolution of the sensor achieves 0.02 ℃ (0.18 ℃) in high (low) resolution mode.

Key words: RFID; temperature sensor; passive; UHF; tag
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1. Introduction

The radio-frequency identification (RFID) system offers many advantages, such as faster reading speed, greater operating distance and larger memory space over the traditional barcode system[1]. Passive UHF RFID tags have been widely applied in supply chain management, logistics, public transportation, and so on. If some sensors are embedded into the tag chip, the application area of the tag can be much extended. The tag with a temperature sensor function has recently become very attractive for remotely monitoring the temperature of perishable food, animals and humans[2, 3].

The typical temperature sensors embedded in passive RFID tag were implemented by a time-readout scheme[2, 4, 5]. These sensors adopted a two-point calibration technique to achieve the target accuracy so that the total cost of the tag increases greatly. An improved temperature sensor has been proposed that is also based on the time-readout scheme[6]. The sensor used the same band-gap reference and quantization clock generator to generate bias currents for the temperature-to-pulse converter and to compensate for the process variations, respectively, so that it only requires one-point calibration. However, the temperature-dependent pulse width is still affected by variation of the capacitors and the supply voltages. Furthermore, the sensor needs to average 128 samples for the target accuracy so that the sensing time increases to 40 ms.

The RF rectifier is one of the key components in the passive UHF RFID tag chip because the communication distance between the tag and the reader depends on its rectifying efficiency. Although there are various rectifier structures, only two kinds of rectifier are practical for UHF RFID tags[7]. One is the gate cross-connected bridge structure, which does not utilize diode or diode-connected MOS transistors. Its power efficiency is high because it does not suffer from threshold voltage problems. However, the voltage gain is not as high as that of the charge pump structure. The other one is the Dickson charge pump structure, which is based on the diode or diode-connected MOS transistors. The diode threshold voltage loss usually reduces the power efficiency of the rectifier. Although a Schottky diode with low threshold voltage can be used to improve the efficiency, it requires extra mask layers and process steps.

A small amount of non-volatile memory (NVM) should be embedded in the RFID tag to store information. The conventional EEPROM/FLASH memory requires additional mask layers and process steps, which are not suitable for low cost RFID tags. Recently, several NVM memories in standard CMOS processes have been reported[8, 9]. A single poly EEPROM cell has been proposed, in which the FN tunneling effect is employed to program the memory cell[8]. However, the NMOS tunneling device reduces its retention and endurance performance. Another embedded memory has been reported[9]. However, each bit cell has a high voltage switch and an SRAM data-latch so that the memory has a large area and power consumption.

This paper proposes a passive EPC Gen-2 UHF RFID tag chip with a dual-resolution temperature sensor. The chip consists of a dual-resolution low power temperature sensor, a high efficiency rectifier, analog frontend circuits, a digital baseband and a single-poly low power NVM memory. The sensor can operate in low and high resolution modes. It can not only achieve the target accuracy but also reduce the power consumption and sensing time. The rectifier is a CMOS-only rectifier with high

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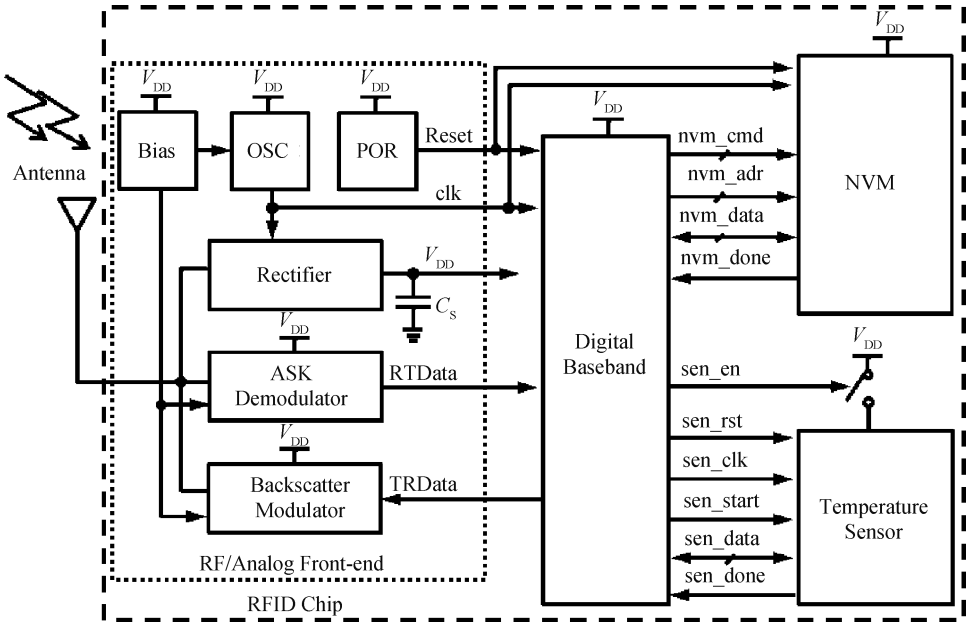

Fig. 1. Architecture of the tag chip.

power efficiency. The memory is an ultra low power NVM memory based on a single-poly standard CMOS process. The tag chip features dual-resolution, one-point calibration, high sensitivity, a CMOS-only circuit and compact size. This paper is organized as follows. First, the system architecture of the tag chip is introduced. Then the circuit design of critical building blocks is discussed. After that, the implementation and measurement results are presented, and the conclusions are finally presented.

2. Architecture of tag chip

The architecture of the tag chip is shown in Fig. 1. The chip consists of four main blocks: a temperature sensor, an RF/analog front-end circuit, an NVM memory and a digital baseband. The RF/analog front-end circuit block converts the energy of the incoming RF signal into a DC power supply for the active circuits on the chip and demodulates (modulates) the received (transmitted) signal. It generates the clock/reset signal also. A CMOS-only rectifier is used as a UHF RF rectifier.

The temperature sensor monitors the temperature and outputs the temperature signal in digital format. The digital baseband block processes the tag baseband signal based on the EPC Gen-2 protocol and controls the operation of the sensor. The NVM memory is used to store the EPC code and the temperature sensor signal.

Although the temperature sensor with ADC has better and more reliable performance, it is considered to be unsuitable for passive RFID tags because it consumes a large amount of power. In practice, the NVM memory during write operation consumes tens of microwatts that are provided by the RF rectifier for tens of milliseconds. If we can reduce the power consumption of the temperature sensor with ADC to some tens of micro watts, and let NVM memory and the temperature sensor be enabled alternately, the tag chip with the ADC-type temperature sensor can operate effectively. A low power sigma–delta ($\Sigma\Delta$) ADC is integrated into the temperature sensor in the tag.

In many application cases, the temperature sensor usually focuses on a small specific temperature range to measure the temperature at higher resolution, but for a wider temperature range the measuring resolution may be relaxed. Actually, if the sensor is calibrated at a suitable temperature point for the small temperature range, the non-linear error of the sensor is very small near the calibrated point and the measuring error can be controlled. Here we design a temperature sensor with dual-resolution operation modes: a high-resolution mode with a small temperature sensing range and a low-resolution mode with a wide sensing range. Thus the sensor can not only meet the demands of practical applications but also reduce the resolution requirement of the ADC so that the circuit structure is simplified, and the power consumption and conversion time are reduced.

To realize a highly sensitive tag chip with a high resolution temperature sensor at low cost, a dual-resolution temperature sensor is proposed with one point calibration. Then a CMOS-only rectifier is used to replace the Schottky diode rectifier and is biased by a switched-capacitor bias to improve its power efficiency. Furthermore, an ultra low power NVM is designed based on a single-poly standard CMOS process. The tag chip can be integrated into a standard CMOS process without extra mask layers and process steps. The detailed operation principles of these circuits will be discussed in the next section.

3. Design of circuit blocks

3.1. Temperature sensor with dual resolution

The block diagram of the temperature sensor is shown in Fig. 2. It consists of a bipolar sensing core, a second-order $\Sigma\Delta$ ADC, a dynamic element match (DEM) control module and a bias circuit. The $\Sigma\Delta$ ADC includes a $\Sigma\Delta$ modulator, a decimation filter and a clock generator. The bipolar sensing core is used as the sensing element because the bipolar transis-

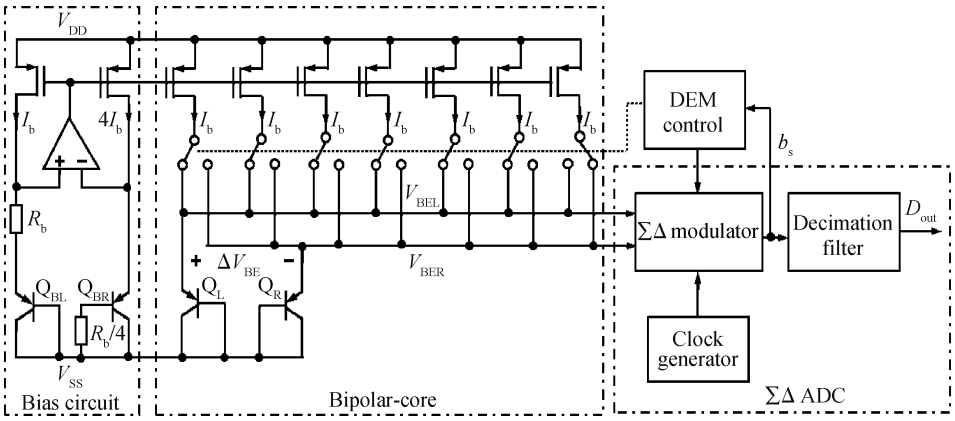

Fig. 2. Block diagram of the temperature sensor.

tor is particularly suitable for generating a linear temperature-dependant voltage signal[10]. The second-order ΣΔ ADC is used to digitize the output of the bipolar sensing core. The DEM module uses a DEM control technique to reduce the mismatch effect among the current sources in the bipolar core and the mismatch effect among the sampling capacitors in the ΣΔ modulator. The bias circuit generates a bias current I_b to make the base–emitter voltages insensitive to the spread of the current gain[10].

In the bipolar core, two diode-connected substrate PNP transistors output two temperature-dependent base–emitter voltage signals V_{BEL} and V_{BER}. The two voltage signals are then used to produce one voltage signal ΔV_{BE}, which is proportional to absolute temperature (PTAT) and one temperature-independent reference voltage signal V_{REF}.

The relationship between the temperature T and the above two voltages (V_{BER} and ΔV_{BE}) can be expressed as[11]

$$T = A\frac{\alpha}{\alpha + X}, \tag{1}$$

where A is a constant of about 600, $X = V_{BER}/\Delta V_{BE}$ and α is the gain factor, which is chosen to make a band-gap reference voltage $V_{REF} = V_{BER} + \alpha\Delta V_{BE}$. If $\alpha/(\alpha + X)$ is digitized, to achieve a resolution of 0.01 ℃ (0.1 ℃), the ADC with a resolution of 16 bit (13 bit) is required because the temperature sensing range is about 600 ℃. This is not acceptable for passive RFID tags. So another method is used to relax the resolution requirement of the ADC.

Supposing X changes from X_L to X_H ($X_H > X_L$) when the temperature ranges from T_H to T_L($T_H > T_L$), X can be transformed to

$$\eta = \frac{X - X_L}{X_H - X_L}. \tag{2}$$

Therefore η changes from 0 to 1 for the temperature range from T_H to T_L. If η is digitized and $T_H - T_L \ll 600$ ℃, the resolution requirement of the ADC can be much reduced.

The temperature sensor has two operating modes: a high-resolution mode with a small sensing temperature range and a low-resolution mode with a wide sensing range. The two operating modes are switched by the ΣΔ modulator, as shown in Fig. 3. The modulator consists of a loop filter and a clocked comparator. For simplicity, only a first-order loop filter is shown. In the actual implementation, a second-order filter is used to reduce the sampling time. The comparator produces one bit of the bit stream in each clock cycle

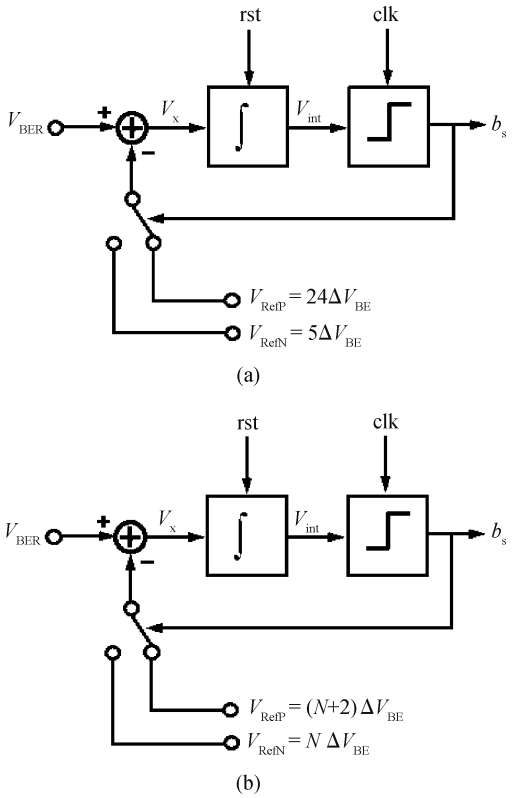

Fig. 3. ΣΔ modulator for dual operation modes. (a) Low resolution mode. (b) High resolution mode.

In low resolution mode, supposing $5\Delta V_{BE} < X < 24\Delta V_{BE}$, if the output of the ΣΔ modulator is one, $-24\Delta V_{BE}$ is added into the input of the integrator in the next cycle; otherwise, $-5\Delta V_{BE}$ is added into the input. Thus the total input V_x of the integrator is adjusted to near zero. If the average value of the bit stream is denoted as η, the following expression can be obtained,

$$(24\Delta V_{BE} - V_{BER})\eta = (V_{BER} - 5\Delta V_{BE})(1 - \eta). \tag{3}$$

Solving for η gives

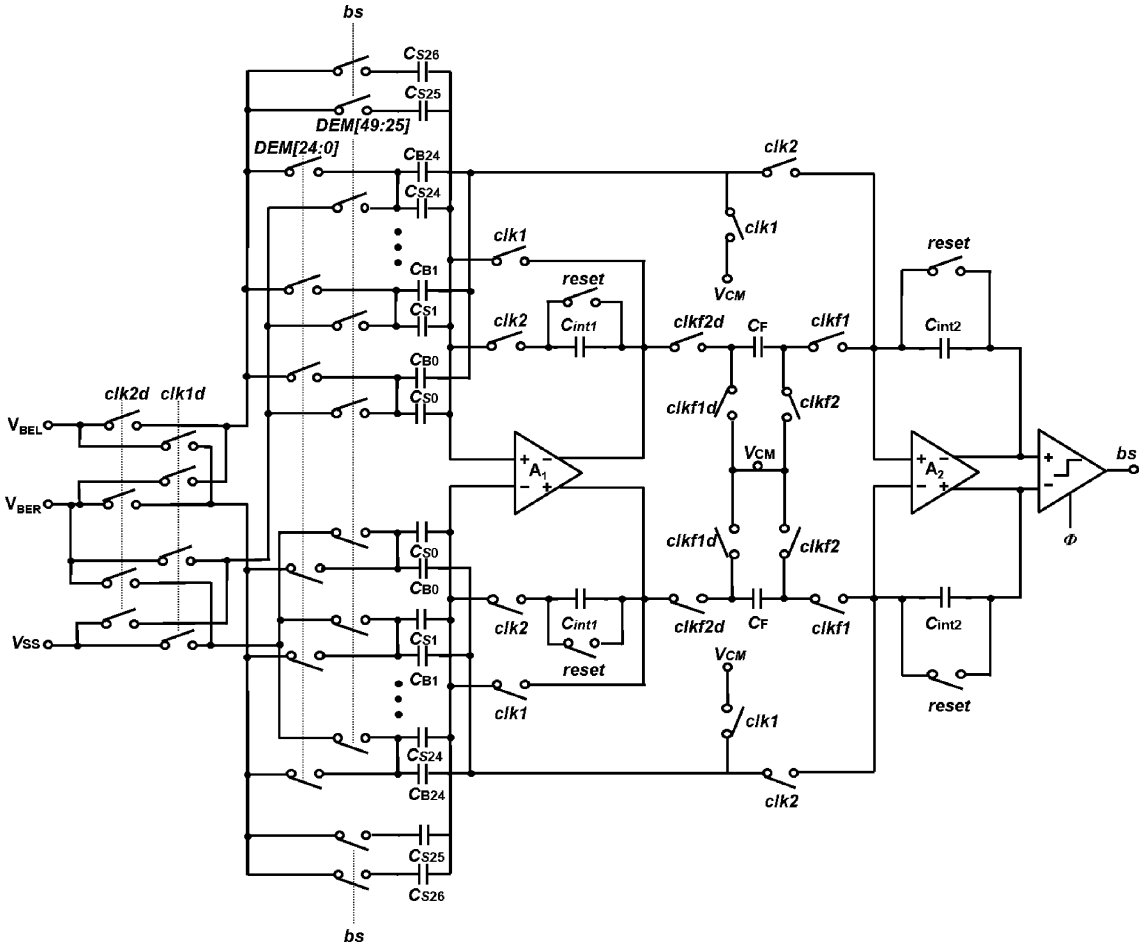

Fig. 4. Circuit diagram of the second-order ΣΔ modulator.

$$\eta = \frac{V_{\mathrm{BER}} - 5\Delta V_{\mathrm{BE}}}{19\Delta V_{\mathrm{BE}}} = \frac{X-5}{19}. \tag{4}$$

In high resolution mode, supposing $N\Delta V_{\mathrm{BE}} < X < (N+2)\Delta V_{\mathrm{BE}}$, if the output of the ΣΔ modulator is one (zero), $-(N+2)\Delta V_{\mathrm{BE}}$ ($-N\Delta V_{\mathrm{BE}}$) is added into the input of the integrator in the next cycle. Solving for η in the same way gives

$$\eta = \frac{V_{\mathrm{BER}} - N\Delta V_{\mathrm{BE}}}{2\Delta V_{\mathrm{BE}}} = \frac{X-N}{2}. \tag{5}$$

From Eqs. (4) and (5), X can be obtained, and then the temperature can be solved from Eq. (1). Furthermore, for the high resolution mode, we use the integer N to program the temperature sensing range.

Although ΔV_{BE} is insensitive to process variation, V_{BER} is sensitive to process variation because it depends on the absolute values of both the saturation current and the collector current. This process-dependent variation in V_{BER} is PTAT[10]. The variation in V_{BER} can be determined by calibration at one temperature (one-point calibration) and then corrected by a digital parameter. In the design, α is adjusted by the digital parameter stored in NVM memory to compensate for this PTAT variation in V_{BER}. The adjusting scheme is much simpler than analog trimming techniques, such as bias-current-trimming[12].

We adopt a switched-capacitor circuit to design the ΣΔ modulator. The switched-capacitor circuit is suitable for cancelling the parameter mismatch and the signal offset in the circuit. The low-resolution and high-resolution modes can be easily switched by controlling the on/off of the switches in the switched-capacitor circuit. The circuit diagram and the clock signals of the modulator are shown in Figs. 4 and 5, respectively. To shorten the temperature sensing time, a second-order ΣΔ modulator is used. Capacitors C_{s0} to C_{s26} are the sampling capacitors of the first integrator and their values are the same as

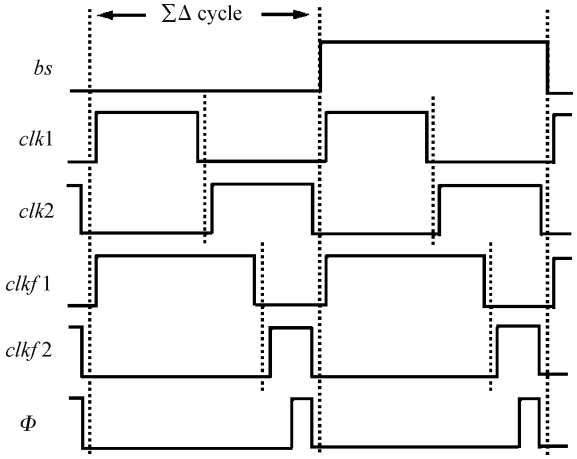

Fig. 5. Clock signals of the modulator.

each other. Capacitor C_F is the sampling capacitor of the second integrator. Capacitors C_{B0} to C_{B24} are the feed-forward capacitors, which ensure the stability of the modulator. The control signal DEM[24:0] (DEM[49:25]) determines the number of sampling capacitors for ΔV_{BE} (V_{BER}). Thus the control signal can not only switch the low and high resolution modes but also select one reference voltage from $5\Delta V_{BE}$, $24\Delta V_{BE}$, $N\Delta V_{BE}$ and $(N + 2)\Delta V_{BE}$ to subtract the input signal. Furthermore, the control signal DEM[24:0] (DEM[49:25]) can alternate the sampling capacitors to realize a dynamic element match control technique so that the parameter mismatch in the circuit can be cancelled.

In the second-order $\Sigma\Delta$ modulator, the first integrator determines the accuracy of the modulator. As the ADC's resolution requirement is relaxed, an amplifier gain of 80 dB is enough so that no gain boosting technique is required. This greatly reduces the chip area and power consumption. At the end of a $\Sigma\Delta$ cycle, the output of the first integrator is sampled on capacitors C_F and is integrated by the second integrator at the beginning of the next $\Sigma\Delta$ cycle. Since the errors are attenuated by the gain effect of the first integrator, no dynamic element matching is needed in the second integrator. The bit stream is produced by comparing the polarity of the output voltage of the second integrator with the clocked comparator. The modulator uses non-overlapping clocks (clk1 and clk2, clkf1 and clkf2) and delayed clocks (clk1d and clk2d, clkf1d and clkf2d) to reduce the errors induced by charge injection. Furthermore, the chopping technique is used in the amplifier to reduce the offset. The modulator runs for 128 cycles and produces a bit stream of 128 bits. Then the sinc^2 decimation filter processes the bit stream and outputs the temperature information.

3.2. CMOS UHF rectifier

The CMOS-only rectifier is based on a modified charge pump structure. The circuit architecture of the rectifier is shown in Fig. 6. It consists of six cascaded rectifier cells and an oscillator. RF_{in} is the input RF signal and V_{DD} is the rectified DC supply voltage. In the rectifier, Schottky diodes are not used so that the chip cost can be reduced[13, 14].

Traditionally, the cells in a charge pump circuit have either nMOS or pMOS switch transistors, in which the gate of one switch transistor is connected to the pumping capacitor and results in a large parasitic capacitance. In this rectifier cell, both nMOS and pMOS switch transistors are used, which make the gate of the switch transistor avoid connecting to the pumping capacitor. This method can reduce the parasitic capacitance of C_1. As C_1 is directly coupled to the input RF signal, reducing its parasitic capacitance can improve the power efficiency of the rectifier.

Furthermore, in the rectifier cell, two kinds of bias circuit are designed to make the nMOS and pMOS transistor switches work in the sub-threshold region, respectively. The two kinds of bias circuits are implemented with nMOS and pMOS switched-capacitor circuits, respectively. The switched-capacitor circuit is equivalent to a large resistor so that a bias is generated on C_m and NMb. The bias is equivalent to an independent supply voltage. Transistors NMb and NM1 are always in the subthreshold region. Thus the rectifier can offer high efficiency.

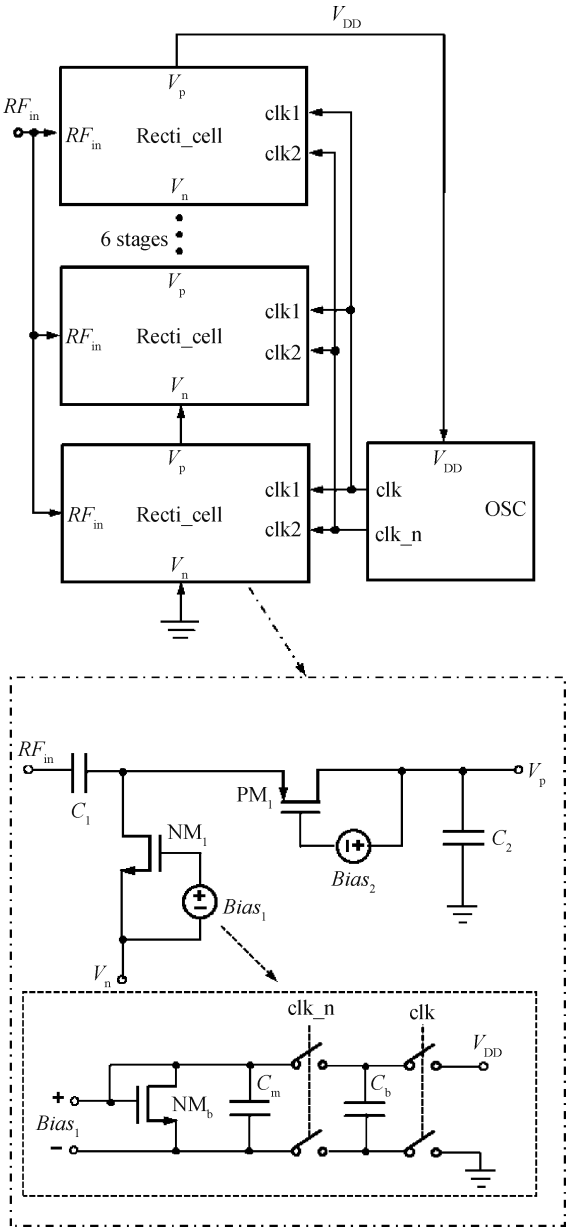

Fig. 6. Circuit architecture of the CMOS rectifier.

3.3. Single-poly NVM

NVM is required to store the EPC code and some user information. To minimize the process cost and power consumption, the memory adopts the cell based on the horizontal differential floating gate structure compatible with a standard CMOS process and bi-directional FN-tunneling to achieve reliable low power programming[15].

The block diagram of the proposed NVM is shown in Fig. 7. It includes two memory arrays with equal numbers of bits: a non-volatile array and a volatile register array. Each 16 bit word in the non-volatile array has a corresponding 16 bit word in the register array. The data in the non-volatile array are first loaded into the register array for the subsequent read operation, which is both faster and consumes much less power. The integrated charge pump circuit generates the high voltages

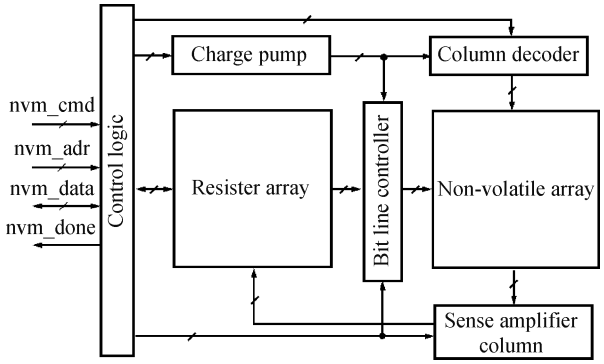

Fig. 7. Block diagram of the non-volatile memory.

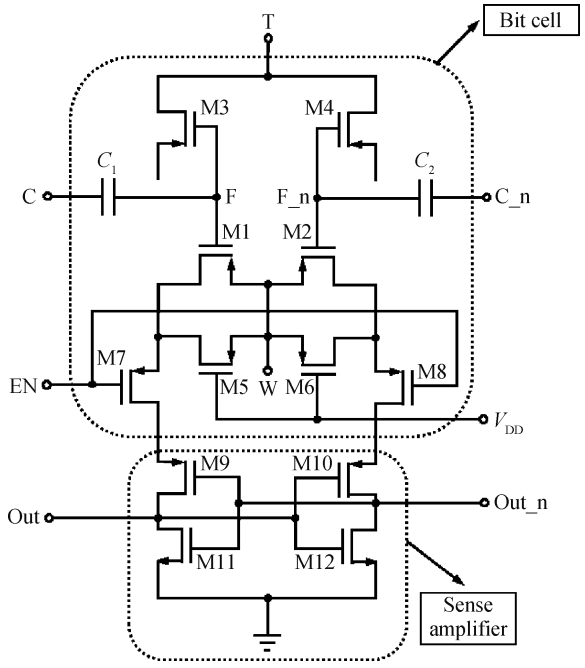

Fig. 8. Schematic of the bit cell and the sense amplifier.

for programming. The bit line controller sends high voltages to the bit line according to the input data during programming. The column decoder selects the active column and the sense amplifier column outputs the data in the active-column cells during read operation.

A schematic of the memory bit cell and the sense amplifier is shown in Fig. 8. Although the area of the bit cell is larger compared with that of flash memory, it does not require extra mask layers or process steps, so the cost is less for low capacity memories. To achieve reliable low power programming, the bi-directional FN-tunneling mechanism is utilized. The electrons can tunnel through M1 and M2 (M3 and M4) to enter into (depart from) the floating gates. Because the FN tunneling occurs at different junctions during electron injecting and erasing, the stress on the gate oxide is alleviated, which will improve the endurance and retention characteristics. As the capacitances of C_1 and C_2 are much larger than those of tunneling junctions, the voltages of the floating gates can be controlled by the voltages of nodes C and C_n, respectively. As a result, a high electric field across the junctions can be established for FN-tunneling by properly biasing the nodes C, C_n, T, W and

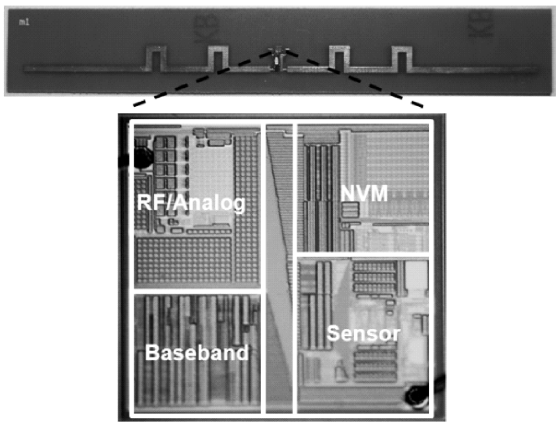

Fig. 9. Photographs of the chip and tag.

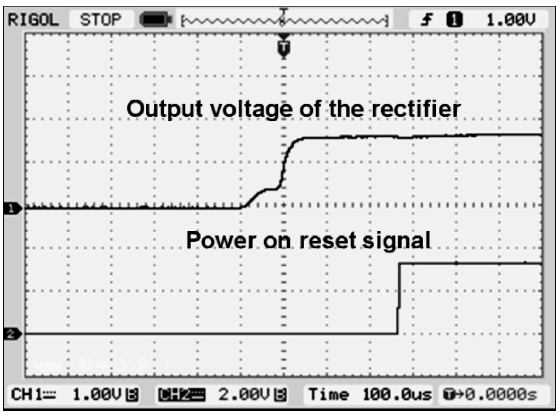

Fig. 10. Output waveform of the rectifier and the power on reset signal.

EN.

The logic state of the cell is determined by the difference in the charges stored on the two floating gates. For read operation, M1 and M2 convert the voltage difference on the floating gates into current difference, which can be detected by the sense amplifier. After the sense amplifier is latched, there is no static current flowing in the cell.

4. Implementation and measurement results

The passive UHF RFID tag chip with a dual-resolution temperature sensor and a 192-bit NVM memory was implemented in a 0.18 μm one-poly standard CMOS process. Figure 9 shows photographs of the chip and tag. The chip area is 1 mm^2. It was bonded onto a copper antenna on a PCB substrate to realize a tag. To evaluate the performance of the building circuit blocks, another tag chip with test pads was also implemented.

Figure 10 shows the output voltage waveform of the rectifier and the power on reset signal at the input power of –3 dBm and load resistor of 20 kΩ. The effect of the switched-capacitor bias is clearly shown here. The power efficiency of the rectifier was very low at the beginning because the bias circuit and the clock generator did not operate well during that time. After the output voltage increased to above 200 mV, the bias circuit and clock generator began to operate well and the power efficiency was increased greatly. The measured power efficiency of the

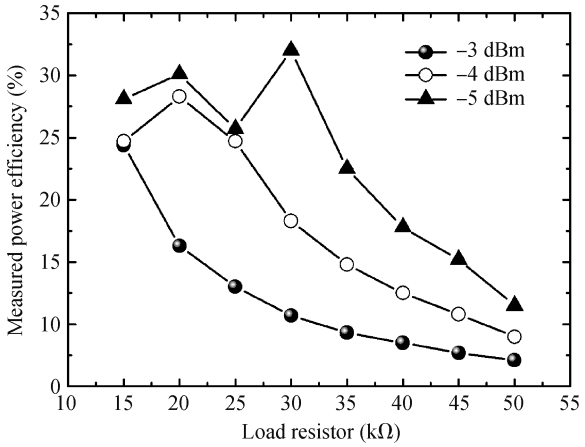

Fig. 11. Measured power efficiency of the rectifier at different input powers.

Table 1. Measured performance of the 192-bit NVM.

Parameter	Value
Technology	0.18-μm standard CMOS
Bit cell area	220 μm^2
Supply voltage	1.2 V
Clock frequency	0.78 MHz
Write non-volatile array	4.3 μW @ 0.8 kb/s
Read non-volatile array	2.2 μW @ 1.3 Mb/s
Write register array	1.1 μW @ 3.2 Mb/s
Read register array	0.12 μW @ 3.2 Mb/s
Program/erase endurance	10^5

rectifier is shown in Fig. 11. The rectifier achieved a power efficiency of about 30% at the load resistor of 20 kΩ and input power of –5 dBm. It is much larger than 20% efficiency of the conventional rectifier based on the Schottky diode[16]. This result also showed that the power efficiency increased as the load resistor was reduced. The power efficiency also increased as the input power was reduced.

The measured performance of the 192-bit NVM is shown in Table 1. The write power consumption of the NVM is only 4.3 μW @ 1.2 V supply voltage, which is acceptable in a passive RFID tag. The NVM also shows good endurance performance of more than 10^5 write/erase times. Furthermore, this memory is fully compatible with a standard CMOS process. Although the bit cell area is larger than conventional FLASH memory, the total cost is less if the size is relatively small (< 16 kb).

The temperature sensor was placed inside the temperature chamber with a temperature constancy of ±0.3 ℃ and a temperature error of ±0.5 ℃. One-point calibration was carried out. Figures 12 and 13 show the measured temperature sensing inaccuracy for low resolution mode and high resolution mode, respectively. The inaccuracy of the sensor is –0.6 ℃/0.5 ℃ (–1.0 ℃ /1.2 ℃) over the operating range from 5 to 15 ℃ (–30 to 50 ℃). The resolution of the sensor archives 0.02 ℃ (0.18 ℃) in high (low) resolution mode. This measured inaccuracy is influenced by the error of the temperature chamber. The temperature sensor consumes a power consumption of only 13 μW @ 1.2 V and a conversion time of 6 ms.

The tag was successfully measured using commercial

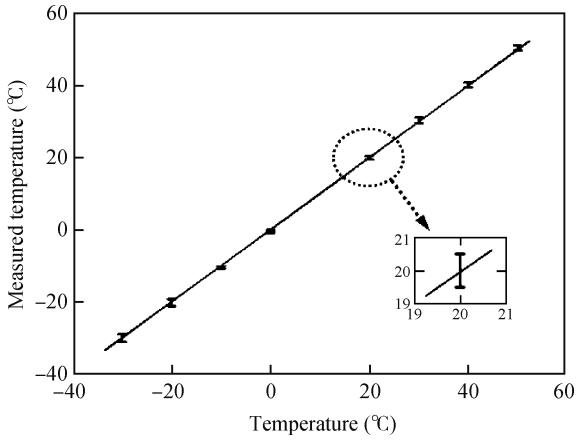

Fig. 12. Measured error of the temperature sensor (low resolution mode).

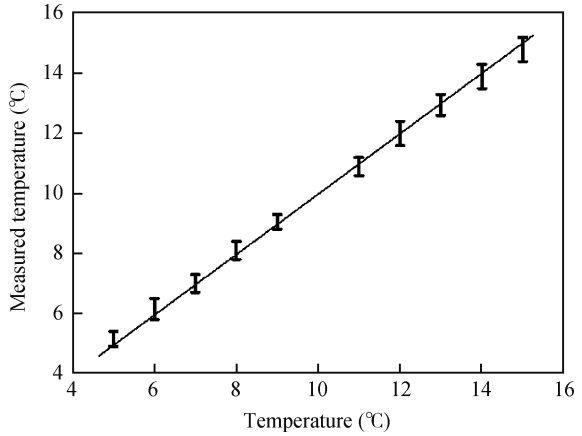

Fig. 13. Measured error of the temperature sensor (high resolution mode).

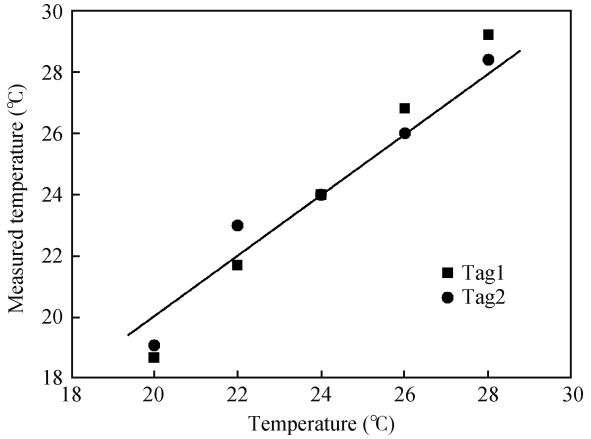

Fig. 14. Measured temperature error of the tag (low resolution).

RFID readers with 2 W EIRP. The sensitivity of the tag is –10.7 dBm/–8.4 dBm when the sensor is disabled/enabled. It achieves a maximum reading/sensing distance of 4 m/3.1 m. Figures 14 and 15 show the measured temperature sensing function of the tag in the room. Although the sensing error is limited by the reference temperature sensor and other non-ideal effects, the tag shows good performance. Table 2 summarizes

Table 2. Performance summary and comparison.

Parameter	Ref. [2]	Ref. [3]	Ref. [6]	This work
Technology (μm)	0.35 CMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS
Chip area (mm^2)	4.0	N/A	1.1	1.0
Frequency range (MHz)	860–960	860–960	860–960	860–960
Standard	EPC Gen2	EPC Gen2	EPC Gen2	EPC Gen2
Tag type	Passive	Passive	Passive	Passive
Memory	EEPROM	OTP memory	OTP memory	192-bit NVM
Sensitivity (dBm)	–4.6	0	–6	–8.4
Sensing distance (m)	2 (2 W ERP)	N/A	4 (4 W EIRP)	3.1 (2 W EIRP)
Sensing range (℃)	35–45	–10 to 30	–20 to 30	High resolution: 10 (programmable) Low resolution: –30 to 50
Sensing error (℃)	±0.1	–0.8/1	±0.8	High resolution: –0.6 /0.5 Low resolution: –1.0 /1.2
Resolution (℃)	0.035	0.18	0.35	High resolution: 0.02 Low resolution: 0.18
Conversion time (ms)	100	30	40	6
Calibration	Two-point	Two-point	One-point	One-point

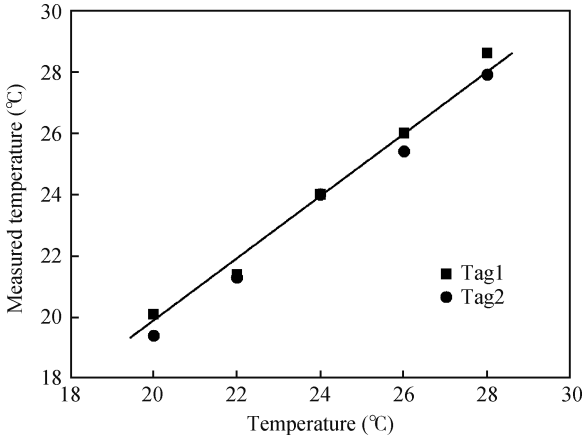

Fig. 15. Measured temperature error of the tag (high resolution).

and compares the performance of the tag with that of other tags. The results demonstrated that our tag has better tag sensitivity, temperature sensing resolution, sensing error and sensing speed than other tags. The single-poly 192-bit NVM other than OTP memory was embedded in the tag.

5. Conclusion

A passive EPC Gen-2 UHF RFID tag with a dual-resolution temperature sensor was proposed. The tag chip with an area of 1 mm^2 was implemented in a 0.18-μm standard CMOS process. The sensor with a low power sigma–delta ($\Sigma\Delta$) ADC could operate in low and high resolution modes. A CMOS-only RF rectifier and a single-poly 192-bit NVM were integrated to realize a low cost tag chip. The sensitivity of the tag was –10.7 dBm/–8.4 dBm when the sensor was disabled/enabled. It achieved a maximum reading/sensing distance of 4 m/3.1 m at 2 W EIRP. The inaccuracy of the sensor was –0.6 ℃ /0.5 ℃ (–1.0 ℃/1.2 ℃) over an operating range of 5 to 15 ℃ in high resolution mode (–30 to 50 ℃ in low resolution mode). The resolution of the sensor was 0.02 ℃ (0.18 ℃) in high (low) resolution mode.

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References

[1] Finkenzeller K. RFID handbook: fundamentals and applications in contactless smart cards, radio frequency identification and near-field communication identification. United Kingdom: John Wiley & Sons, 2010

[2] Vaz A, Ubarretxena A, Zalbide I, et al. Full passive UHF tag with a temperature sensor suitable for human body temperature monitoring. IEEE Trans Circuits Syst II, 2010, 57: 95

[3] Law M K, Bermak A, Luong H C. A sub-μW embedded CMOS temperature sensor for RFID food monitoring application. IEEE J Solid-State Circuits, 2010, 45: 1246

[4] Zhou S H, Wu N J. A novel ultra low power temperature sensor for UHF RFID tag chip. IEEE Asian Solid-State Circuits Conf, 2007: 464

[5] Lin Y S, Sylvester D, Blaauw D. An ultra low power 1 V, 220 nW temperature sensor for passive wireless applications. IEEE Custom Integrated Circuits Conf, 2006: 507

[6] Yin J, Yi J, Law M K, et al. A system-on-chip EPC Gen-2 passive UHF RFID tag with embedded temperature sensor. IEEE J Solid-State Circuits, 2010, 45: 2404

[7] Cui J, Akita J, Kitagawa A. A rectifier structure for UHF RFID transponder with high efficiency. IEICE Electronics Express, 2010, 7: 1086

[8] Ohsaki K, Asamoto N, Takagaki S. A single poly EEPROM cell structure for use in standard CMOS processes. IEEE J Solid-State Circuits, 1994, 29: 311

[9] Raszka J, Advani M, Tiwari V. Embedded flash memory for security applications in a 0.13 μm CMOS logic process. IEEE ISSCC Dig Tech Papers, 2004: 46

[10] Pertijs M A P, Makinwa K A A, Huijsing J H. A CMOS temperature sensor with a 3σ inaccuracy of ± 0.1 ℃ from –55 ℃ to 125 ℃. IEEE J Solid-State Circuits, 2005, 40: 2805

[11] Souri K, Kashmiri M, Makinwa K. A CMOS temperature sensor with an energy-efficient zoom ADC and an inaccuracy of ± 0.25 ℃ (3σ) from –40 ℃ to 125 ℃. IEEE ISSCC Dig Tech Papers,

2010: 310
[12] Pertijs M A P, Huijsing J H. Bitstream trimming of a smart temperature sensor. Proc IEEE Sensors, 2004: 904
[13] Zhang Q, Feng P, Zhou S H, et al. A novel RFID tag chip with temperature sensor in standard CMOS process. IEEE Int Symp Circuits Systems, 2010: 1109
[14] Zhou Shenghua, Wu Nanjian. CMOS UHF rectifier. Chinese Journal of Semiconductors, 2007, 28: 1471
[15] Feng P, Li Y L, Wu N J. An ultra low power non-volatile memory in standard CMOS process for passive RFID tags. IEEE Custom Integrated Circuit Conf, 2009: 713
[16] Umeda T, Yoshida H, Sekine S, et al. A 950 MHz rectifier circuit for sensor networks with 10 m-distance. IEEE ISSCC Dig Tech Papers, 2005: 256