A 0.13 μm CMOS $\Delta\Sigma$ fractional-N frequency synthesizer for WLAN transceivers

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Abstract: A fractional-N frequency synthesizer fabricated in a 0.13 μm CMOS technology is presented for the application of IEEE 802.11 b/g wireless local area network (WLAN) transceivers. A monolithic LC voltage controlled oscillator (VCO) is implemented with an on-chip symmetric inductor. The fractional-N frequency divider consists of a pulse swallow frequency divider and a 3rd-order multistage noise shaping (MASH) $\Delta\Sigma$ modulator with noise-shaped dithering techniques. Measurement results show that in all channels, phase noise of the synthesizer achieves –93 dBc/Hz and –118 dBc/Hz in band and out of band respectively with a phase-frequency detector (PFD) frequency of 20 MHz and a loop bandwidth of 100 kHz. The integrated RMS phase error is no more than 0.8°. The proposed synthesizer consumes 8.4 mW from a 1.2 V supply and occupies an area of 0.86 mm^2.

Key words: WLAN IEEE 802.11 b/g; frequency synthesizer; voltage controlled oscillator; $\Delta\Sigma$ modulator
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1. Introduction

The frequency synthesizer is one of the key building blocks in a ratio frequency (RF) communication system for its function to generate the local oscillator (LO) signal for both the receiving and transmitting paths. Frequency synthesizer design is of crucial importance to obtain good systematic performance for an RF transceiver. The recent applications of RF transceivers call for much more aggressive goals for frequency synthesizers because it must meet very stringent requirements such as proper frequency tuning range, low phase noise, fast settling time, fine frequency resolution and limited spur levels under area and power consumption constraints.

IEEE 802.11 b/g has become the most widely deployed WLAN standard recently, which occupies a frequency range from 2.412 to 2.484 GHz. In this paper, a $\Delta\Sigma$ fractional-N frequency synthesizer fabricated in a 0.13 μm CMOS technology is proposed for the application of IEEE 802.11 b/g WLAN transceivers. A block diagram of the proposed synthesizer is shown in Fig. 1.

Nowadays, the traditional charge pump based phase-locked loop (CPPLL) is still the most popular synthesizer architecture used in RF systems while high-frequency all digital phase-locked loop (ADPLL) research has become a new hot development direction with the minimum size scaling down to nanometre scale. As illustrated in Fig. 1, the proposed synthesizer in this paper is based on the CPPLL structure. It is composed of two main parts, the phase-locked loop (PLL) and LO generator. The PLL generates a RF signal ranging from 1.45 to 1.84 GHz while the LO mixer converts the signal up to a frequency band ranging from 2.17 to 2.76 GHz, which can fully meet the frequency coverage requirement of IEEE 802.11 b/g WLAN standard. The up-conversion design of the LO generator is for eliminating the frequency pulling problem caused by the power amplifier (PA) in the transmitting path. In this paper, discussion will focus on the PLL design.

As shown in Fig. 1, the PLL is composed of a crystal oscillator, a PFD, a charge pump, a VCO, a VCO buffer and a fractional-N frequency divider. A crystal oscillator provides an accurate and clean input reference signal to the frequency synthesizer. Then, the PFD compares the phase and frequency differences between the reference signal and the output signal of the fractional-N frequency divider. The following CP injects an output current proportional to the differences detected by the PFD into the loop filter to adjust the control voltage on the VCO. The 3rd-order loop filter filters out the high frequency components and extracts an average VCO voltage to improve the spectral purity of VCO output. In addition, the loop filter also plays a key role in system-level loop dynamics. The VCO is adjusted by the loop so the desired frequency can be acquired. A programmable fractional-N frequency divider is included in the feedback path in order to accomplish channel selection. This fractional-N divider consists of a pulse swallow frequency divider and a 3-rd MASH 1-1-1 $\Delta\Sigma$ modulator with noise-shaped dithering techniques which is used for low phase noise and spurs considerations. The feedback signal output by the fractional-N frequency divider is re-synchronized by the output of the VCO buffer in order to reduce the noise produced by the whole frequency divider.

The LO generator operates as follows. A high speed divider follows the VCO buffer and divides the frequency of the VCO output by 2 then sends it to the LO port of the up-conversion mixer. The output signal of the VCO becomes quadrature after a 2nd-order poly-phase filter and mixes with its half-frequency signals produced by the high speed divider in the up-conversion mixer. The up-converted signal ranging from 2.17 to 2.76 GHz is sent to an output buffer to drive both the down-conversion mixer and the up-conversion modulator in the receiving and transmitting paths.

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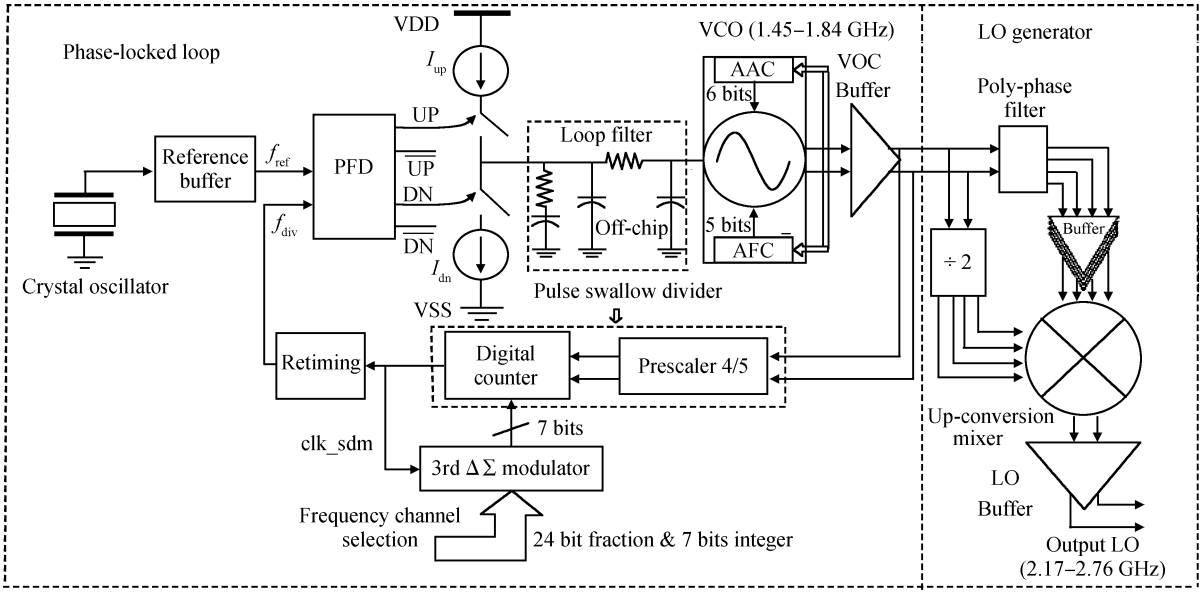

Fig. 1. Block diagram of the proposed ΔΣ fractional-N frequency synthesizer.

2. Circuit design and analysis

2.1. Voltage controlled oscillator

The voltage controlled oscillator is the most determinant building block of a frequency synthesizer. The most important characteristics of a VCO are its phase noise and its frequency tuning range. VCO design seems uncomplicated at the first glance. However, designing an optimized VCO with good performance is not an easy job for it is a question of finding the best tradeoff among many different variables which all interact with each other.

The LC tank-based VCO is the best normalized structure, which leads to low phase noise at the cost of a slightly larger area. As demonstrated in Fig. 2(a), the VCO proposed in this work is based on a current steered LC tank structure. The amplitude of the VCO output is determined by the programmable tail current. The proposed VCO can achieve optimized low phase noise performance with limited current consumption with the help of an automatic amplitude control (AAC) scheme. To obtain sustained oscillation, cross-coupled PMOS transistors M1 and M2 are adopted to provide negative resistances by forming a positive feedback loop to cancel the LC tank loss. PMOS are preferred rather than NMOS for their lower frequency flicker noise contribution to the VCO. The frequency range is coarsely tuned by a 5-bit switched capacitors bank. The switched capacitor bank is composed of 5 capacitor branches, thus there are 32 sub frequency bands in total. An automatic frequency control (AFC) scheme is introduced for fast switching among different sub-bands. Fine frequency tuning is accomplished with two PMOS varactors. These varactors are tuned by the control voltage from the loop filter. C_3 and C_4 are designed as 6 pF to suppress varactor instantaneous voltage variation. L_0 is a differential symmetric inductor with a high Q value for low phase noise considerations. Experimental results show that the achieved frequency tuning range is 1.45 to 1.84 GHz and K_{VCO} varies from 45 to 80 MHz/V. Good noise performance is attained when the AAC scheme programs the tail current at approximately 1.6 mA.

The VCO buffer is designed to isolate the VCO from on-chip noise, captive loading and frequency pulling. A schematic of the VCO buffer is shown in Fig. 2(b). The output signal of the VCO is ac coupled by two small capacitors and sent into two differential common-source NMOS transistors, M1 and M2. The gates of M1 and M2 are set to 900 mV through two resistors R_1 and R_2. A cascode topology is adopted for its high output impedance and better reverse isolation. M3 and M4 are cascode transistors whose gates are connected to the power supply 1.2 V VDD. Four capacitor switched branches working with L_1 are used to adjust the LC tank frequency of the VCO buffer according to the frequency of the VCO. The inductor load is useful for acquiring high voltage gain without decreasing output voltage headroom. The VCO buffer dissipates 1.5 mA from the power supply.

2.2. Phase-frequency detector

A schematic of PFD in this work is illustrated in Fig. 3. The PFD compares the divided-down signal with the reference signal (20 MHz) and provides an error voltage, which is ultimately fed back to control the oscillator. As shown in Fig. 3, the PFD is rising-edge sensitive. Delay is added into the feedback path to overcome the dead zone effect. It should be ensured that the time for reset is longer than the delay in the forward path, otherwise the dead zone problem can not be eliminated. However, adding further delay into the feedback path will cause both current sources to be on simultaneously, which is undesirable from a noise, spur and power-consumption point of view. Thus the delay should be very carefully designed. In this work, the delay time is defined as approximately 360 ps, which is short enough to stop the unwanted CP current from injecting into the loop filter as long as it can eliminate the dead zone.

2.3. Charge pump

A charge pump is responsible for providing an output current proportional to the phase difference detected by the PFD.

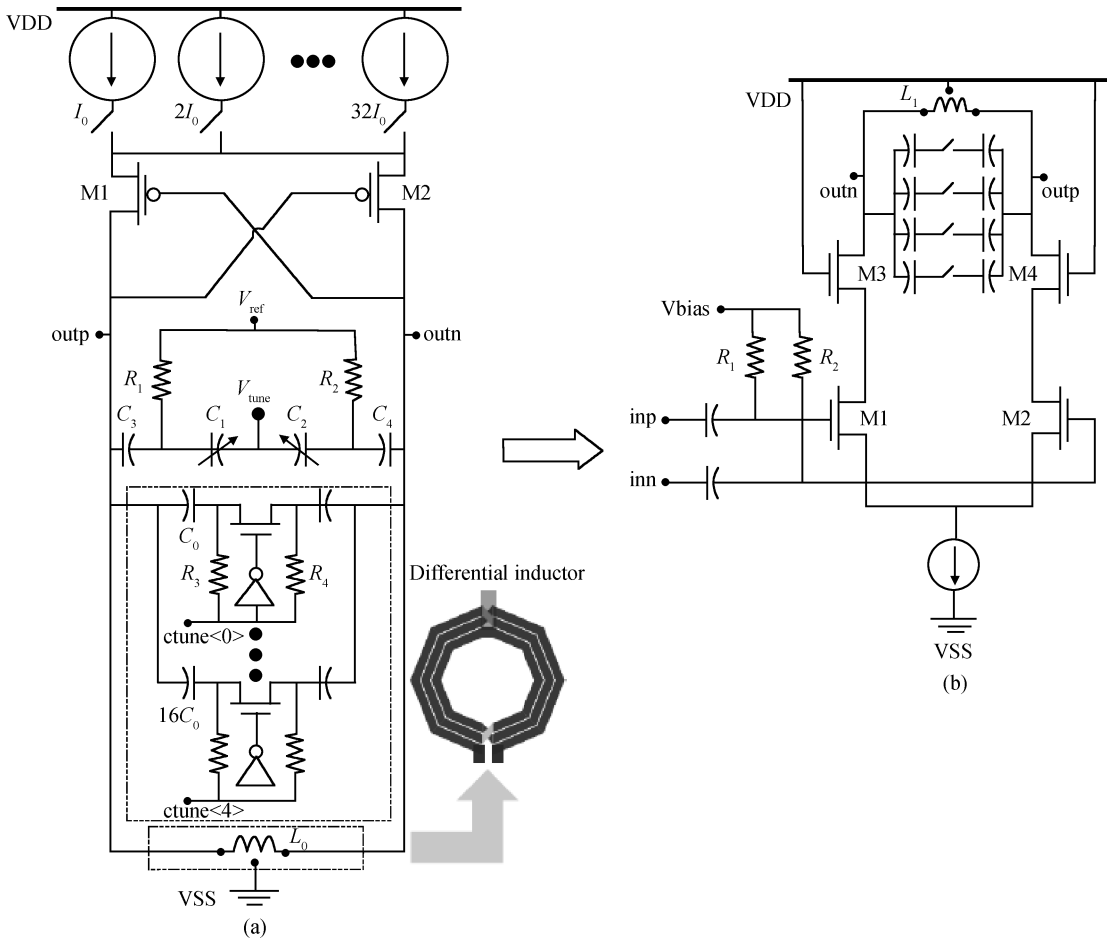

Fig. 2. (a) Schematic of the VCO. (b) Schematic of the VCO buffer.

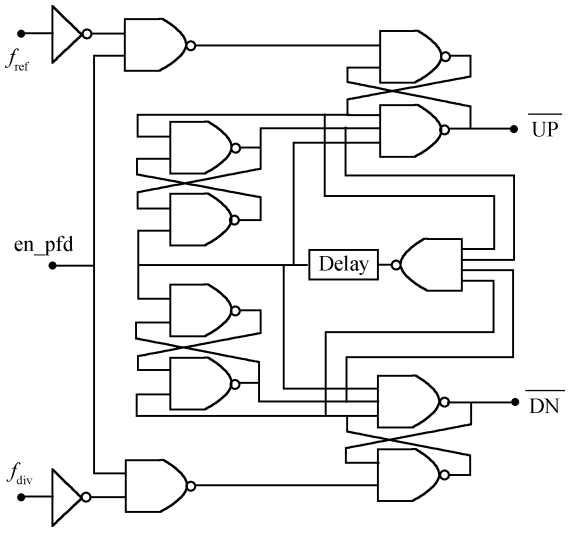

Fig. 3. Schematic of the dead-zone-free PFD.

Since CP noise can often dominate the phase noise performance in the band of the whole PLL system, it must be very carefully designed. Generally, there are several CP design issues, such as minimizing current mismatch, reducing reference feed through and leakage current, keeping low output noise and high linearity. Schematic architecture of the CP proposed in this work is illustrated in Fig. 4. The programmable current bias scheme is desirable because it permits the flexibility of being able to adjust the loop bandwidth and the optimization of charge pump current for optimum phase noise performance. As shown in Fig. 4, M2, M3, M4 and M5 are employed as current source transistors. The control voltage on the VCO can vary from 0.3 V to 0.9 V. M6, M7, M8 and M9 are used as switches connected to the gates rather than current source transistor drains. The gate connection is helpful to decrease the reference spurs. In order to improve the matching of I_{UP} and I_{DN}, the NMOS and PMOS switches need to turn on or off at the same rate. This is accomplished by setting the widths of M8 and M9 two times than M6 and M7 while keeping them the same lengths. However, the current I_{UP} and I_{DN} should be exactly equal, not only when the output happens to be VDD/2 but for any output voltage. Thus, a rail-to-rail OPAMP is introduced into the bias scheme. The OPAMP senses the output voltage and compares it with the voltage at the drains of the mirror transistors. If the voltage on the mirrors is higher than the voltage at the output, then it increases the voltage on the gate of M5 and M4. This causes the current through M5 to decrease slightly, forcing the currents through both the NMOS and PMOS transistors to be almost exactly equal, regardless of the output voltage. Special attention should be paid to the polarity of the OPAMP for maintaining stability. There is a neg-

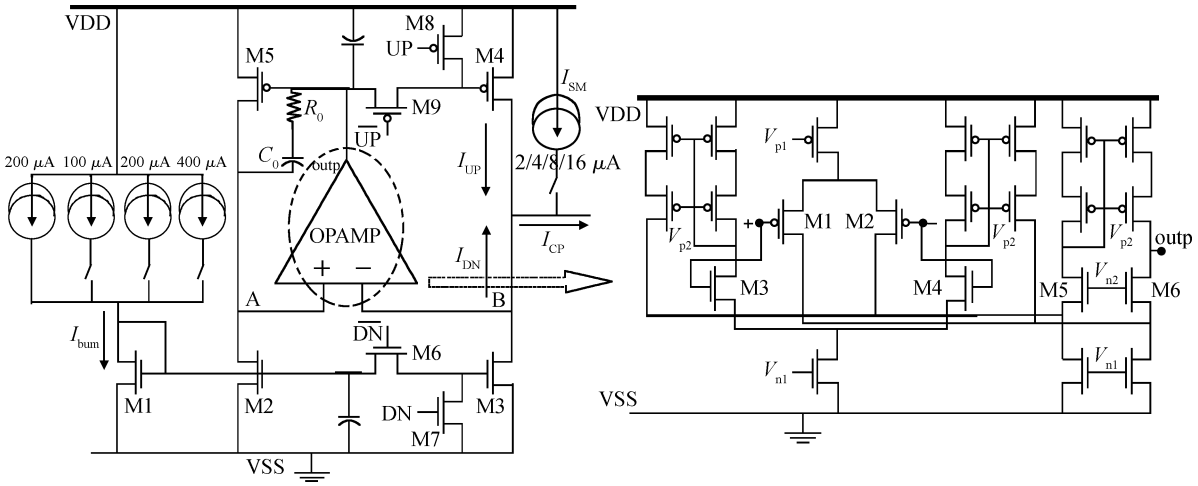

Fig. 4. Schematic architecture of the charge pump and the rail-to-rail operating amplifier.

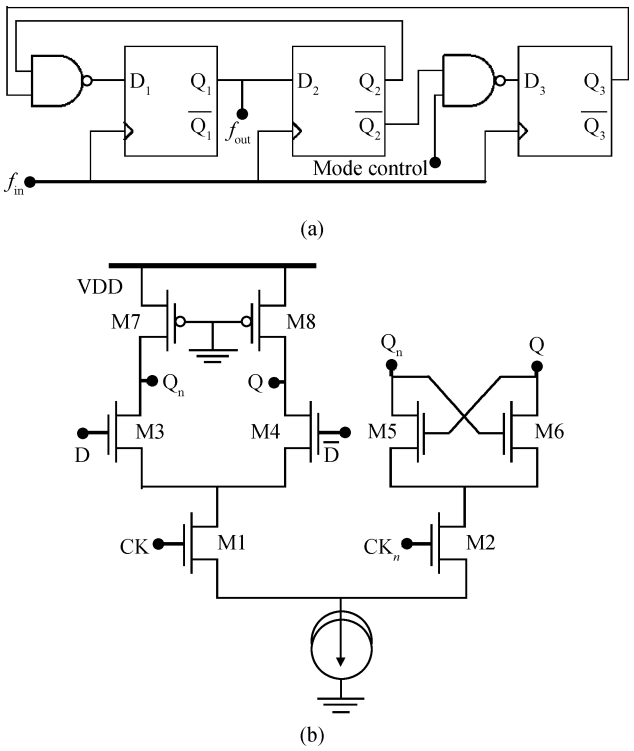

Fig. 5. (a) Schematic architecture of precaler 4/5. (b) Schematic of the proposed D latch.

ative and a positive feedback loop in this CP scheme. R_0 in series with C_0 is used to keep the feedback loop stable. I_{SM} programmed in binary steps from 2 to 16 μA is used to inject a correction current into the loop filter with the aim of improving current matching for a further step.

2.4. Fractional-*N* frequency divider

As shown in Fig. 1, the proposed fractional-*N* frequency divider consists of a high speed dual-modulus prescaler 4/5, digital counters and a 3-rd order $\Delta\Sigma$ modulator. The dual-modulus prescaler 4/5 and the 7-bit digital counters make up a pulse swallow frequency divider, which is responsible for integer dividing. The 3-rd $\Delta\Sigma$ modulator is in charge of fractional dividing.

The schematic of the dual-modulus prescaler 4/5 is shown in Fig. 5(a). It consists of three D-type flip-flops and two NAND gates. Since the prescaler 4/5 runs at the maximum frequency in the divider, it is very important to improve the operating speed of the D-type flip-flops. In this work, current mode logic (CML) is adopted because it can operate fast with low power dissipation. One D-type flip-flop is made up of two D-latches. As illustrated in Fig. 5(b), a novel D-latch is adopted in this work. Two transistors, M7 and M8, working in the linearity region are used as the load rather than a traditional resistor load[1]. The equal resistance R_{on} of M7 and M8 is given in the following equation.

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{V_{DS}}{\mu_p C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]} = \frac{1}{\mu_p C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{1}{2}V_{DS}\right)}. \quad (1)$$

When V_{DS} decreases, R_{on} becomes smaller which is desirable for Q_n or Q to turn to high logic. Hence, both high speed and low power consumption are acquired with the D-latch. The precaler 4/5 can operate at 2 GHz and dissipates 1.6 mA from a 1.2 V power supply.

In fractional-*N* synthesis, the instantaneous divisor value achieved by using different integers is always around the desired fractional value. The time-averaged divisor value is equal to the desired fractional value when the loop is in lock. However, switching between different divisor values results in undesirable phase jitter or spurs near the desired carrier frequency. Hence, randomization techniques are needed to break the correlation and repeated patterns and to spread the spur energy over the frequency band. Generally, this is accomplished by using a $\Delta\Sigma$ modulator. A noise shaping $\Delta\Sigma$ modulator, which is a high-pass noise characteristic in the frequency domain, is used to control the integer divisor of the pulse swallow divider such that the fractional spurs can be randomized and

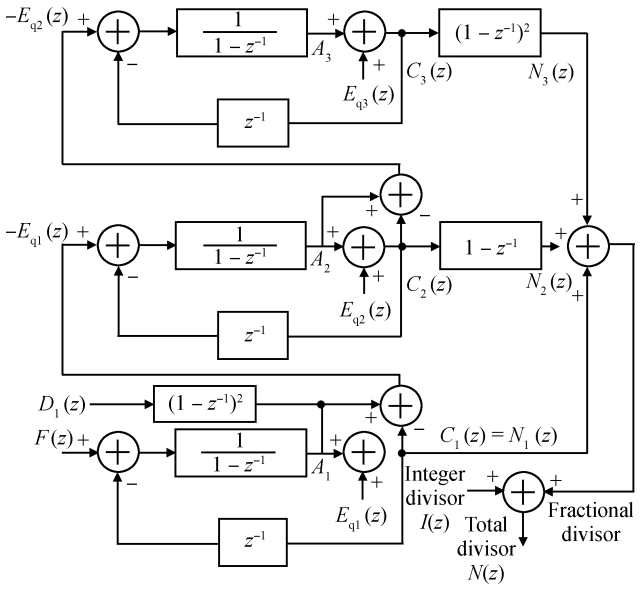

Fig. 6. Simplified architecture of the proposed 3-rd order MASH 1-1-1 $\Delta\Sigma$ modulator.

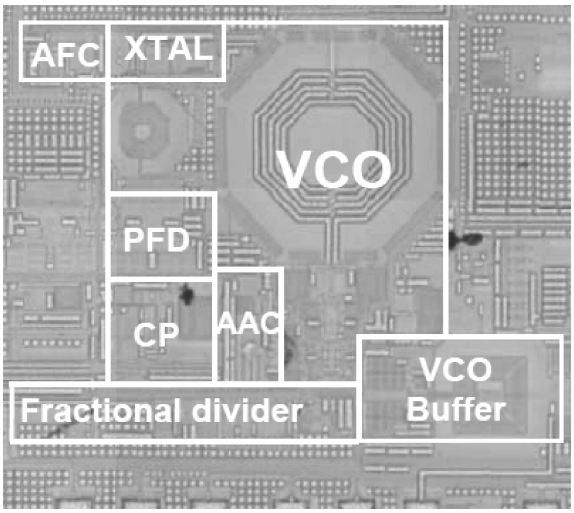

Fig. 7. Die photograph of the proposed synthesizer.

shifted to a higher frequency band where they can be easily removed by the loop filter. The MASH 1-1-1 structure is one of the most widely used topologies due to its stability, high-order in-band noise-shaping characteristic and easy implementation. In this work, a 3-rd order 24-bit MASH 1-1-1 $\Delta\Sigma$ modulator is employed. The integer divisor is expressed with a 7-bit word, while fractional divisor adopts a 24-bit word. Fine frequency resolution (< 1 Hz) is achieved by using a 24-bit fractional dividing control word, as shown in Eq. (2).

$$\text{Frequency resolution} = \frac{1}{2^{24}} f_{\text{ref}} = \frac{1}{2^{24}} \times 20\,\text{MHz} \ll 1\,\text{Hz}. \tag{2}$$

Simplified architecture of this MASH 1-1-1 $\Delta\Sigma$ modulator is shown in Fig. 6.

As demonstrated in Fig. 6, Mash 1-1-1 is a cascaded $\Delta\Sigma$ structure with three first-order loops. Each of the three loops is identical to the previous single-loop architecture. The fractional accumulator periodically generates the carry-out that toggles the loop division ratio. The integrator carries out the accumulator function and has a transfer function of $1/(1–z^{-1})$ when the delay unit is placed in the feedback path. $I(z)$ expresses the integer divisor and $.F(z)$ represents the fractional divisor. $D_1(z)$ is a 1-bit random sequence introduced into the output of the first loop. The total divisor $N(z)$ can be written as

$$\begin{aligned} N(z) &= I(z) + N_1(z) + N_2(z) + N_3(z) \\ &= I(z) + C_1(z) + (1-z^{-1})C_2(z) + (1-z^{-1})^2 C_3(z). \end{aligned} \tag{3}$$

where

$$C_1(z) = \cdot F(z) + (1-z^{-1})Eq_1(z), \tag{4}$$

and

$$C_2(z) = (1-z^{-1})^2 D_1(z) - Eq_1(z) + (1-z^{-1})Eq_2(z), \tag{5}$$

and

$$C_3(z) = -Eq_2(z) + (1-z^{-1})Eq_3(z). \tag{6}$$

So the total divisor $N(z)$ in Eq. (3) is given by

$$N(z) = I(z) + \cdot F(z) + (1-z^{-1})^3[Eq_3(z) + D_1(z)]. \tag{7}$$

As given in Eq. (7), the quantization error generated in the first and second loops are totally cancelled. The total quantization noise is equal to that of a single loop, although three loops are used. Therefore, the multi-loop $\Delta\Sigma$ architecture provides high-order noise shaping without additional quantization noise. The $\Delta\Sigma$ accumulator outputs are dithered around the desired value in the range from $I(z)$–3 to $I(z)$+4. In the frequency domain, the discrete spurs become more random, with their energy pushed towards the higher frequencies. The dithering technique is used in this modulator. As shown in Fig. 6, since the quantization errors in higher-order loops are more random, a random sequence $D_1(z)$ is introduced into the first loop only in order to de-correlate A_1 and reduce the spur energy[2]. Moreover, the feedback signal output by the fractional-N frequency divider is re-synchronized by the output of the VCO buffer in order to reduce the noise caused by the whole frequency divider for a further step.

In the programmable fractional frequency divider design, the dual-modulus precaler 4/5 and the following logic switching circuit which switches CML to CMOS rail-to-rail logic are completed by analog design, while counters of the pulse swallow divider and the 3-rd MASH 1-1-1 modulator are realized digitally with the help of verilog-HDL and synthesis tools. The overall fractional divider consumes 1.8 mA from the power supply.

3. Experimental results

The proposed synthesizer is fabricated in a 0.13 μm CMOS process and occupies an area of 0.86 mm^2. Figure 7

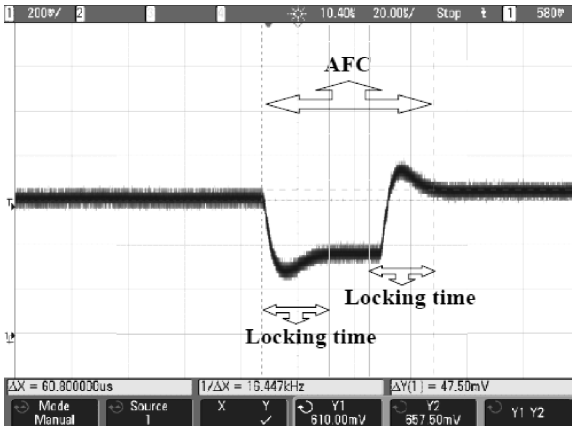

Fig. 8. Locking time and AFC settling time (from 1618 to 1634.667 MHz).

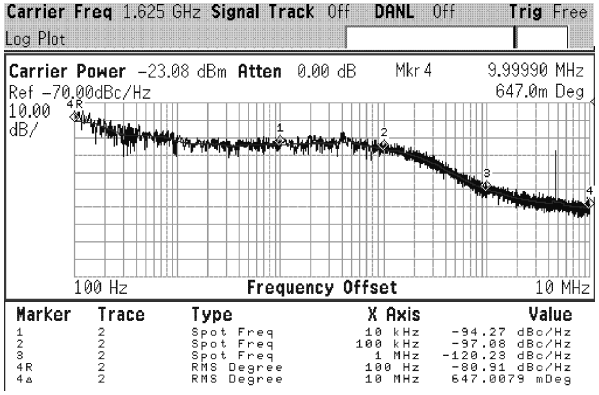

Fig. 9. Phase noise performance of 1.624667 GHz (measured at the output of VCO buffer).

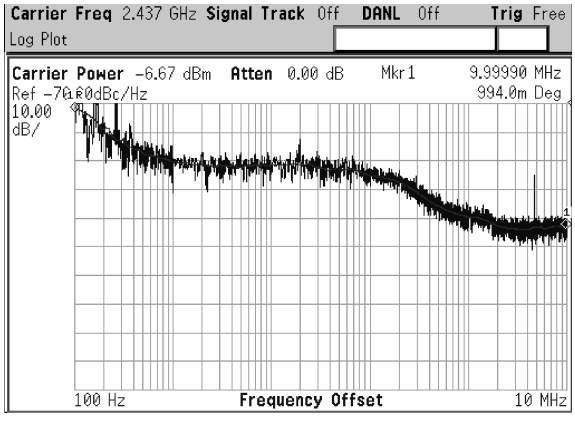

Fig. 10. Phase noise performance of 2.437 GHz (measured at the power amplifier output).

gives a die photograph of this synthesizer. The reference signal is set to be 20 MHz for low spur level and fine frequency resolution considerations, and the loop bandwidth is defined as 100 kHz for loop speed and noise considerations. The measured locking time of the proposed PLL is about 25 μs and the frequency settling time among different channels is no more than 65 μs, as shown in Fig. 8.

The proposed PLL has demonstrated good noise and spur

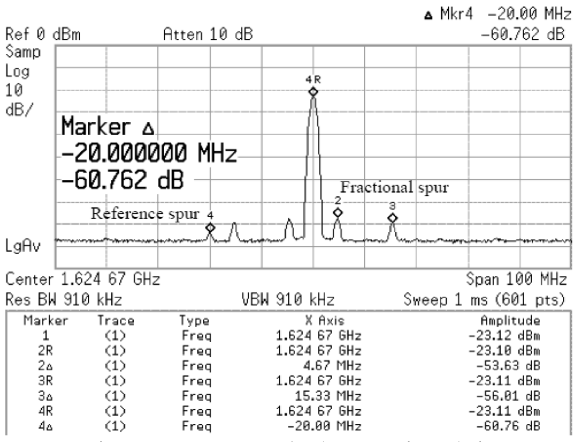

Fig. 11. Frequency spectrum of 1.624667 GHz (measured at the output of VCO buffer).

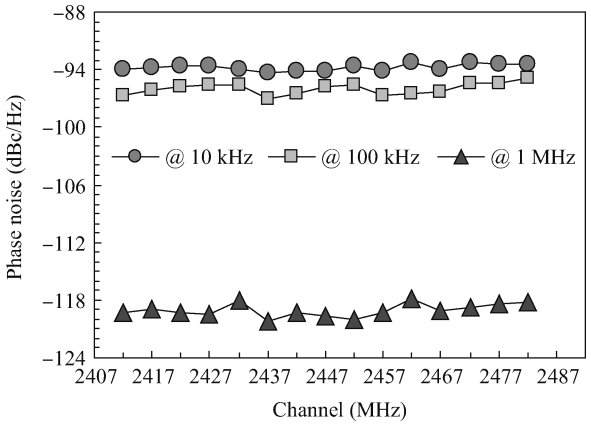

Fig. 12. Phase noise performance of all channels (measured at the output of the VCO buffer).

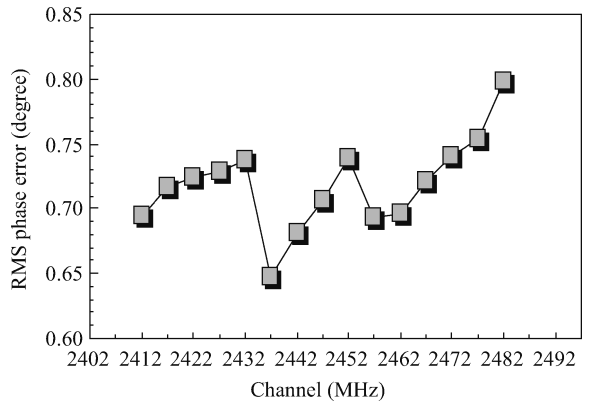

Fig. 13. RMS phase error performance of all channels (measured at the output of the VCO buffer).

performances in test. Measurement results of 1624.667 MHz (channel 2437 MHz) are shown in Fig. 9. As illustrated in Fig. 9, phase noise stays below –94 dBc/Hz in band and –120 dBc/Hz out of band at 1 MHz frequency offset. The RMS phase error integrating from 100 Hz to 10 MHz is 0.65°. In the transmitting path, the signal is up-converted to 2.437 GHz and sent into the up-conversion modulator and then the power

Table 1. Performance comparison with other related works.

Parameter	Ref. [3]	Ref. [4]	Ref. [5]	This work
Supply voltage (V)	1.8	1.2	1.8	1.2
Technology	0.18 μm CMOS	65 nm CMOS	0.18 μm CMOS	0.13 μm CMOS
Frequency range (MHz)	975–1960	90–770	3.2–4	1.45–1.84
Loop bandwidth (kHz)	92.5	100	400	100
Phase noise (dBc/Hz)	–93 @10 kHz –99 @100 kHz –126 @1 MHz	–93 @10 kHz –86 @100 kHz –119 @1 MHz	–93 @10 kHz –99 @100 kHz –111 @1 MHz	–93 @10 kHz –95 @100 kHz –118@1 MHz
RMS phase error (°)	1	1.38	0.58 (10 kHz–10 MHz)	0.8
Power dissipation (mW)	25	10.8	43	8.4

amplifier. The measurement result of the power amplifier output is shown in Fig. 10. The RMS phase error integrating from 100 Hz to 10 MHz is less than 1°. Frequency spectrum and spur performance is shown in Fig. 11. The fractional and reference spur performance both can meet the requirement of WLAN 802.11 b/g. As given in Fig. 11, the fractional spurs located at the frequency offset of the fractional divisor multiplying with a 20 MHz reference spur are less than –53 dBc. The reference spur located at 20 MHz is less than –60 dBc.

The phase noise performance of all the frequency channels in WLAN 802.11 b/g are shown in Figs. 12 and 13. The phase noise is no more than –93 dBc/Hz in band while the phase noise stays below –118 dBc/Hz at 1 MHz frequency offset. The RMS phase error integrating from 100 Hz to 10 MHz is no more than 0.8°.

4. Conclusion

In this paper, a $\Delta\Sigma$ fractional-N frequency synthesizer fabricated in a 0.13 μm CMOS technology has been proposed for the application of IEEE 802.11 b/g WLAN transceivers. The proposed synthesizer consumes 7 mA current from a 1.2 V supply without the LO generator and occupies an area of 0.86 mm^2 excluding PADs. Table 1 gives the performance summary of this work and comparison with other related works[3–5].

References

[1] Hung C M, Floyd B A, Park N, et al. Fully integrated 5.35-GHz CMOS VCOs and prescalers. IEEE Trans Microw Theory Tech, 2001, 49(1): 17

[2] Rogers J, Plett C, Dai F. Integrated circuit design for high-speed frequency synthesis. Artech House, 2006: 315

[3] Lu L, Gong Z, Liao Y, et al. A 975-to-1960 MHz fast locking fractional-N synthesizer with adaptive bandwidth control and 4/4.5 prescaler for digital TV tuners. International Solid-State Circuits Conference, 2009: 395

[4] Kondou M, Matsuda A, Yamazaki H, et al. A 0.3 mm^2 90-to-770 MHz fractional synthesizer for a digital TV tuner. International Solid-State Circuits Conference, 2010: 247

[5] Jian H Y, Xu Z, Y C Wu, et al. A fractional-N PLL for multiband (0.8–6 GHz) communications using binary-weighted D/A differentiator and offset-frequency Δ–Σ modulator. IEEE J Solid-State Circuits, 2010, 45(4): 768