Understanding the failure mechanisms of microwave bipolar transistors caused by electrostatic discharge*

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Abstract: Electrostatic discharge (ESD) phenomena involve both electrical and thermal effects, and a direct electrostatic discharge to an electronic device is one of the most severe threats to component reliability. Therefore, the electrical and thermal stability of multifinger microwave bipolar transistors (BJTs) under ESD conditions has been investigated theoretically and experimentally. 100 samples have been tested for multiple pulses until a failure occurred. Meanwhile, the distributions of electric field, current density and lattice temperature have also been analyzed by use of the two-dimensional device simulation tool Medici. There is a good agreement between the simulated results and failure analysis. In the case of a thermal couple, the avalanche current distribution in the fingers is in general spatially unstable and results in the formation of current crowding effects and crystal defects. The experimental results indicate that a collector-base junction is more sensitive to ESD than an emitter-base junction based on the special device structure. When the ESD level increased to 1.3 kV, the collector-base junction has been burnt out first. The analysis has also demonstrated that ESD failures occur generally by upsetting the breakdown voltage of the dielectric or overheating of the aluminum-silicon eutectic. In addition, fatigue phenomena are observed during ESD testing, with devices that still function after repeated low-intensity ESDs but whose performances have been severely degraded.

Key words: microwave BJT; ESD; failure mechanism; accumulation effect

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1. Introduction

In recent years, the majority of radio frequency (RF) applications are based on microwave BJTs and the failure of such devices may result in the destruction of the whole system[1]. Much work has been devoted to understanding the transient response of a bipolar transistor under an intense electromagnetic pulse (EMP)[2, 3]. Xi and Chai[4−6] have investigated the damage effects of a bipolar transistor by injecting a square-wave pulse into the devices. However, in practice, the complex electrical-over-stress (EOS) induced failure of the devices can not be described as a simple square-wave EMP[4], and, in many cases, failures classified as being due to EOS could actually be due to electrostatic discharge (ESD)[7]. Meanwhile, the potentially destructive effect of ESD on component reliability has become more apparent as semiconductor devices become smaller and more complex. The ESDs result in large electric fields and high current densities in small devices, which can lead to the breakdown of insulators and thermal damage[8]. In silicon bipolar transistors, ESD also accelerates the degradation of the current gain factor, which follows a pattern similar to that caused by thermal stress or ionizing irradiation, and the autoregressive integrated moving average model is used to predict such degradation[9]. Gendron[10] proposed a 1-D analytical description of the injection ratio of a self-biased bipolar transistor under ESD conditions. These efforts have revolved around transistor-based ESD protection, and not involved the multifinger structure. In China, Yang *et al*.[11] have studied the electromagnetic pulse sensitive ports of microwave BJTs, and experimental results show that these kinds of devices are particularly susceptible to ESD, and are generally damaged by about 1–2 kV with the HBM test. The author has also explored the undamaged test method to check ESD latent damage in BJTs[12]. However, no related literature has reported the inner characters such as current, temperature and electric field distribution under the ESD effect.

Typically, failure by the Joule effect occurs where a junction or a metallized trace deteriorates and blows up like a fuse: When the current density exceeds 2 kA/mm^2, aluminum particles start to migrate[8], reducing the available section in the conductor, which ultimately may melt above 10 kA/mm^2 for a typical 2 kV human ESD duration[13]. As a result, there may be an accumulation effect under low-intensity ESDs.

The BJT studied in this paper is the commercial multifinger microwave low-noise NPN silicon epitaxial transistor 2SC3356, whose critical frequency is 7 GHz. It is used widely in the bipolar receiver networks, broadband power amplifiers, and so on. The ESD damage effect has been investigated and the distributions of current, temperature and electric field are also analyzed with the 2-D device simulator Medici. By recording and comparing the damaged voltages of the injected ESD pulses, it has been found that a collector–base (CB) junction

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Table 1. Sensitive ports of 2SC3356 while HBM ESD are injected.

Parameter	Min. degradation voltage (kV)		Min. failure voltage (kV)	
	CB	EB	CB	EB
Value	1.30	> 6.00	1.50	> 6.00

Table 2. Parameter shift of 2SC3356 after ESD injections.

ESD voltage (kV)	h_{FE}	V_{CEO} (V)	V_{CBO} (V)	I_{CEO} (8 V) (pA)	I_{CBO} (20 V) (pA)	I_{EBO} (1.5 V) (nA)
Original value	101	15	35	0.1	0.2	47
1	100	15	35	0.1	0.2	50
1.1	101	15	35	0.2	0.2	48
1.2	101	15	35	0.1	0.2	48
1.3	65	13	27	0.36×10^6	0.73×10^6	47

is more sensitive to ESD than an emitter–base (EB) junction based on the special device structure, although both the Military Standard MIL-STD-750D and national military standard GJB128A-97 define that only the reverse-biased EB junction needs to undergo electrostatic discharge sensitivity testing, and it is generally thought that the most sensitive ports of BJTs should be the EB. It has also demonstrated that the latent failures have degraded the performance of BJTs, devices that still function after repeated low-intensity ESDs but whose performances may be severely deteriorated.

2. Experiment

The ESD robustness of the device is tested using the human body model (HBM) ESD waveform, according to the national military standard GJB 548B-2005[14] and MIL-STD-883C method 3.15.7[15]. The ESD pulses are generated by an ESD simulator ESS-606A, the output range of which is 100–6000 V. All of the 2SC3356 transistors have the same batch number.

During ESD stress, only two of the three terminals are electrically biased, one of the three bipolar terminals is stressed, while the second terminal is at a reference ground potential with the third one floating and the ESD pulse voltage is increased from 1 kV by 100 V steps until a significant degradation ($\geqslant$ 30%) or failure is observed after the ESD stress. In this way, 100 samples are stressed to find the sensitive ports. The results are shown in Table 1.

Table 1 shows that the CB junction is more sensitive to ESD than the EB junction and this is coincident with previous research by our team. When the critical frequency f_T > 600 MHz, the most sensitive junction is CB, not EB[11]. Therefore, the emphasis of the following experiment is focused on the CB junction of 2SC3356, and the results of a 5# sample are shown in Table 2. During ESD stress of collector-to-base, the emitter is floating, this can occur when a bipolar transistor is used as an ESD diode element. Another case is the pin-to-pin RF input-to-RF output stress of a bipolar receiver network, in this case, the emitter may be in a floating state[16, 17].

In Fig. 1, scanning electron microscope failure analysis (SEM FA) shows that the ESD failure occurs between the emitter and base (point A) in a comb-like structure. After removing

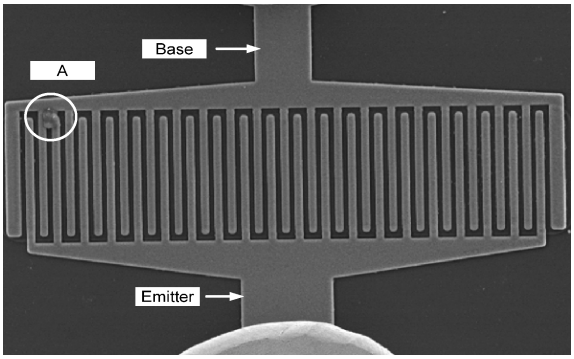

Fig. 1. SEM image of a molten region between the emitter and base.

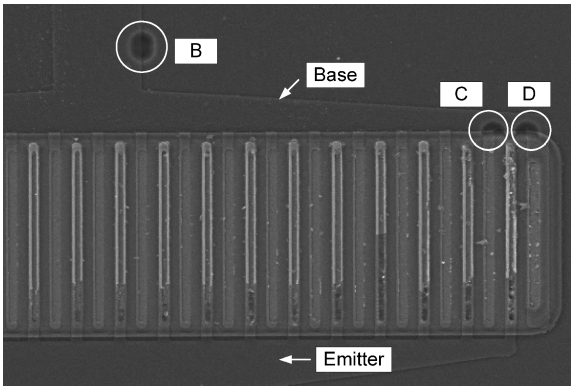

Fig. 2. SEM image of the ESD failure of the BJT after removing the passivation and metal layers.

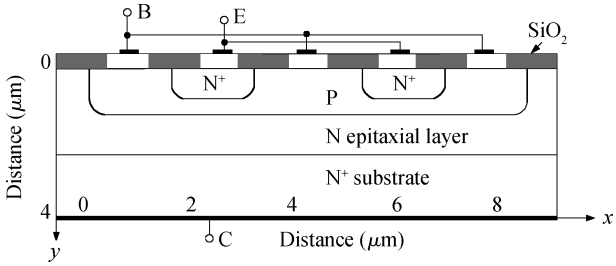

Fig. 3. Structural sketch map of a multifinger BJT.

the passivation and metal layers, another three failure points (B, C, D) are found in the active region, as shown in Fig. 2, however there is no damage observed at point A in this region.

3. Result analysis

3.1. Multifinger structure

The structure of a typical multifinger microwave BJT is given in Fig. 3 and the two-dimensional doping profile is illustrated in Fig. 4. Obviously, considering the simplification, it is an epitaxial n^+–p–n–n^+ bipolar silicon transistor with only two emitters, whereas the model has enough accuracy to describe a multiple-finger structure[18]. There E, B and C denote the emitter, base and collector, respectively. P represents the p-type silicon base regions, N represents the n-type epitaxial layer and N^+ denotes the heavily doped n-type substrate or

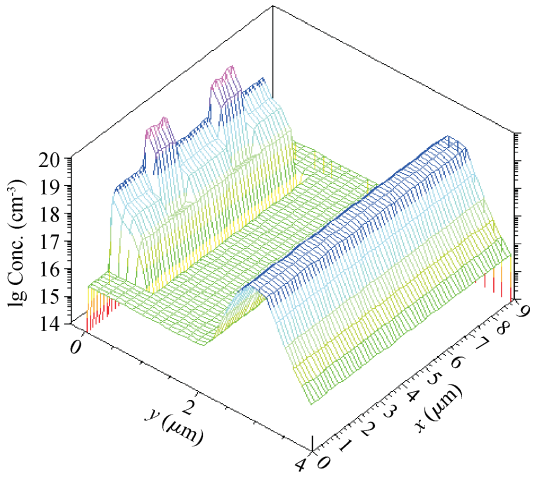

Fig. 4. Doping profile of BJT.

emitters. In order to increase the critical frequency, both the base width and the collector junction depletion region are very small.

3.2. Simulation analysis and discussion

Transient responses of the BJT are performed with the Medici two-dimensional device simulation tool to understand the behavior of the device under HBM ESD conditions. The ambient temperature is 300 K in the simulation.

In the simulation, only the base-collector is electrically biased, the collector is stressed by 1 kV HBM ESD, while the base is at a reference ground potential with the emitter floating. Figure 5 depicts the electric field distribution of the device before and after the avalanche breakdown of the CB junction, the transient electric field of CB junction is as high as 50 MV/m. While some local spots even have a much higher magnitude in the actual structure due to the technical limitation. Then dielectric overvoltage can occur in the junction depletion region adjacent to the electrode. See, for example, point A in Fig. 1 or point B in Fig. 2.

The electro-thermal simulation followed by SEM failure analysis is also developed to investigate the degradation behavior and to help understand the location and the root cause of the ESD failure.

The transistors, when used for power applications, often have multiple fingers to spread out the current and the dissipated heat. Considering a symmetric structure, the current will flow through the fingers equally at the beginning[16, 19] (Fig. 6).

During an ESD event, the temperature transition varies from the ambient temperature to melting temperatures, so the thermal conductivity is not a actually constant[18]. Considering that K is dependent on position x and temperature T during the ESD, K can be expressed as

$$\frac{\partial K}{\partial T} = K\frac{\mathrm{d}(\ln K)}{\mathrm{d}T}\frac{\partial T}{\partial x}. \tag{1}$$

Then, the partial differential equation of heat conduction

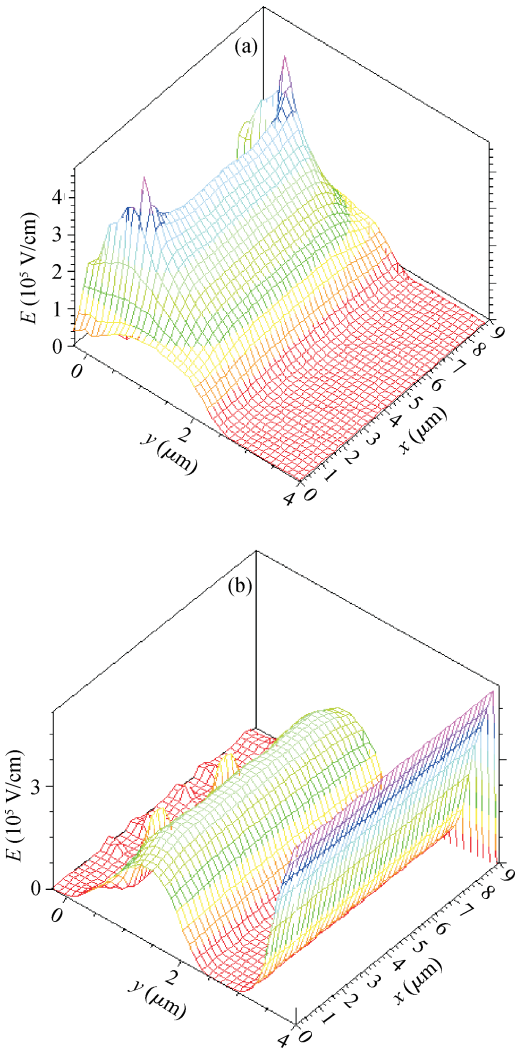

Fig. 5. Distributions of electric field under ESD stress at different times. (a) Before avalanche breakdown at 5 ns. (b) After avalanche breakdown at 15 ns.

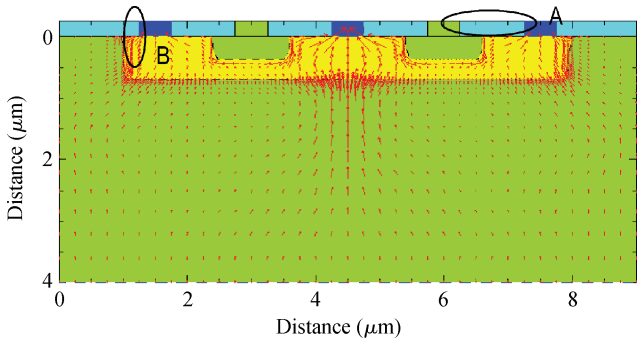

Fig. 6. Distributions of the current density at 5 ns.

with variable conductivity can be put in the form of Eq. (2).

$$K\frac{\partial^2 T}{\partial x^2} + K\frac{\mathrm{d}(\ln K)}{\mathrm{d}T}\left(\frac{\partial T}{\partial x}\right)^2 - \rho c_\mathrm{p}\frac{\partial T}{\partial t} = 0, \tag{2}$$

where c_p denotes the heat capacity, K is the thermal conductivity and ρ is the mass density.

As a result, the increase of temperature may result in un-

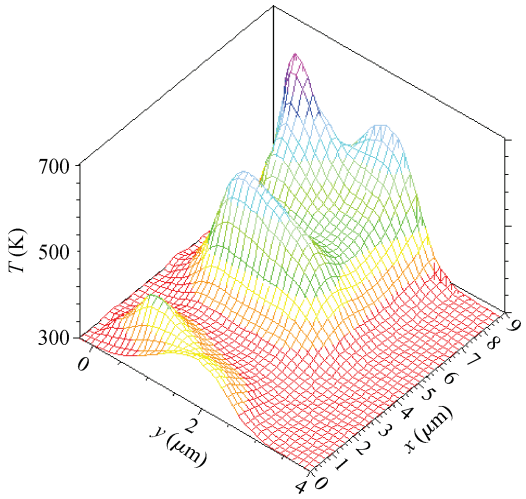

Fig. 7. Nonuniform distributions of temperature at 20 ns.

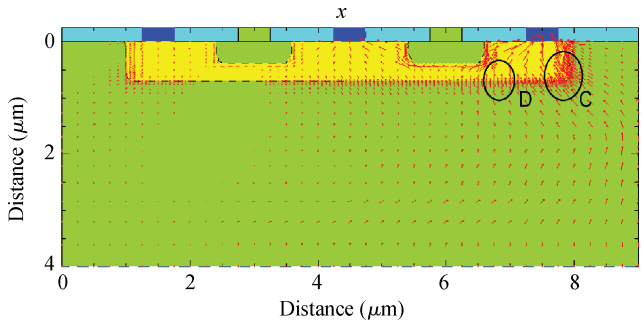

Fig. 8. Nonuniform distributions of the current density at 20 ns.

even heat distribution.

Furthermore, the fingers are actually thermally coupled, which results in a nonuniform temperature distribution, as shown in Fig. 7. Then, because of the heat generated and the uneven heat distribution, the transistors can become unstable at high powers, which seriously limits the power handling capability of the transistors[20]. When this happens, thermal runaway can be observed. The simulation results demonstrate that the peak lattice temperature is at the base edge (Fig. 7), where the current density is also high, as shown in Fig. 8.

To examine the thermal behavior of those fingers, we also use the two-finger configuration for analysis, so the coupled equations can be easily solved and can illustrate the nonuniform temperature distribution for multiple fingers[18]. The temperature of two-finger power consumption dependency can be given as

$$\begin{bmatrix} T_1 - T_A \\ T_2 - T_A \end{bmatrix} = \begin{bmatrix} R_{\text{th1}} + R_{\text{c2}} & R_{\text{c1}} \\ R_{\text{c2}} & R_{\text{th2}} + R_{\text{c1}} \end{bmatrix} \begin{bmatrix} I_1 V_{\text{C}} \\ I_2 V_{\text{C}} \end{bmatrix}. \quad (3)$$

Here, R_{th1} and R_{th2} are the thermal resistances of the fingers, I_1, I_2 are the current flowing through the fingers, T_1 and T_2 are the temperature of fingers, R_{c1} and R_{c2} are the coupling thermal resistances between these fingers, respectively, T_{A} is the ambient temperature and V_{C} is the collector voltage.

A transistor can keep stable when $I_1 = I_2$, but that is almost impossible in practical situations. This is because the nonuniform temperature distribution and any small deviation from the ideal will cause the device to fall into instability.

3.3. Latent failure

The thermal runaway at this region can induce the increase of reverse leakage current of both CB junction and CE junction Because the base width and collector junction depletion region of 2SC3356 are very small.

When the ESD voltage is low, the peak temperature of the contact only reaches the aluminum-silicon eutectic temperature (about 700 K)[8], this can result in aluminum particles starting to migrate and forming a spike through the diffusion without electrical parameters changing, so latent failure will occur.

In the following, the failure analysis of a 5# sample is done using the exclusive method.

Table 2 shows that a significant increase of leakage current I_{CBO}, I_{CEO} is observed with no change in leakage current I_{EBO} after the ESD stress. Comparing the four observed points, only the points C and D can result in the consequence. During the experiment, four ESD pulses are injected into the 5# sample and four damage points are observed, but no electrical parameter shifts are seen until the forth ESD stress. Considering the low-voltage of ESD pulses, it is reasonable to suppose that an ESD pulse only generates one damage point. As a result, it is clear that latent failure caused by the accumulation effect can exist on a BJT without electrical parameters changes being visible by conventional metrology.

4. Conclusions

In this paper, failure mechanisms of microwave bipolar transistors caused by HBM ESD have been investigated. The experimental results indicate that a CB junction is more sensitive to ESD than an EB junction based on the special device structure. Comparing with the SEM failure analysis, 2-D device simulations well reproduce the distributions of electric field, current density and lattice temperature during ESD pulses. When the ESD level is increased to 1.3 kV, the CB junction is burnt out. In addition, the voltage threshold is less than previously thought (1.5–2 kV)[13], therefore no warning exists for possible damage. SEM analysis also demonstrated that ESD failures occur by upsetting the breakdown voltage of the dielectric or local overheating of the aluminum silicon eutectic. Furthermore, fatigue phenomena are observed during ESD testing; devices that still function after repeated low-intensity ESDs but whose performances have been severely degraded. The failure mechanisms of a multifinger bipolar transistor under ESD are very complicated in nature. We use a 2-D simulation tool to analyze the 3-D device in this paper. So, making a model that is closer to the actual situation still needs further studies.

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