Improvement on the dynamical performance of a power bipolar static induction transistor with a buried gate structure*

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Abstract: The failure of a bipolar static induction transistor (BSIT) often occurs in the transient process between the conducting-state and the blocking-state, so a profound understanding of the physical mechanism of the switching process is of significance for designing and fabricating perfect devices. The dynamical characteristics of the transient process between conducting-state and blocking-state BSITs are represented in detail in this paper. The influences of material, structural and technological parameters on the dynamical performances of BSITs are discussed. The mechanism underlying the transient conversion process is analyzed in depth. The technological approaches are developed to improve the dynamical characteristics of BSITs.

Key words: bipolar static induction transistor; dynamical parameters; transient processes; potential barrier; power consumption

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1. Introduction

The bipolar static induction transistor (BSIT) is a new type of power semiconductor device constructed by the comprehensive effects of a static induction transistor (SIT) and a bipolar transistor. In recent years, BSITs have attracted a great deal of attention from scientists and engineers. However, they are mainly interested in steady performances, such as the basic operating mechanism, I–V characteristics, electrical potential distribution in channel and critical fabrication technologies[1−11]. However, BSITs are mainly used in switching application fields. For example, in power frequency conversion, a BSIT turns between the conducting-state and blocking-state frequently. The switching state means a transient process from one steady state to another. It was proved by practice that the failure of devices often occurs neither in the conducting-state nor in the blocking-state, but in the switching state, i.e. the transient process between two steady states. A profound understanding of the physical mechanism of the switching process is of significance for designing and fabricating perfect devices. In this paper, dynamical parameters, such as switching-off time, power consumption, $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ capabilities, are physically discussed in depth, and the processes of turn-on and turn-off of BSITs are studied in detail. Methods to improve the dynamical performances of power BSIT have also been represented.

2. Device structure descriptions

To research the dynamical performances of BSIT, an n-type Si single crystal doped with phosphorus of 1×10^{19} cm^{-3} is used as an original wafer to manufacture BSIT samples. The doping concentrations of the channel, source, drain and gate regions are $N_{\mathrm{DCH}} = 1 \times 10^{14}$ cm^{-3}, $N_{\mathrm{DS}} = 1 \times 10^{19}$ cm^{-3}, $N_{\mathrm{DD}} = 1 \times 10^{19}$ cm^{-3} and $N_{\mathrm{AG}} = 1 \times 10^{19}$ cm^{-3}, respectively. The channel width (L_{D}) is 750 μm, channel length or gate length (L_{G}) is 8 μm, gate-to-gate space, called channel thickness, is 9 μm and repeated period is 25 μm, as shown in Fig. 1. The impurity concentration (N_{DCH}) of the channel region and the gate-to-gate space is so designed that the channel can be completely pinched off by a built-in potential barrier of the gate-channel pn junction. In other words, the channel width must be equal to or smaller than two times of depletion layer width of zero biased gate-channel PN junction, so that the channel can be adequately pinched off. The lightly doped region designated with (n^-) between the gates and drain is referred to as the

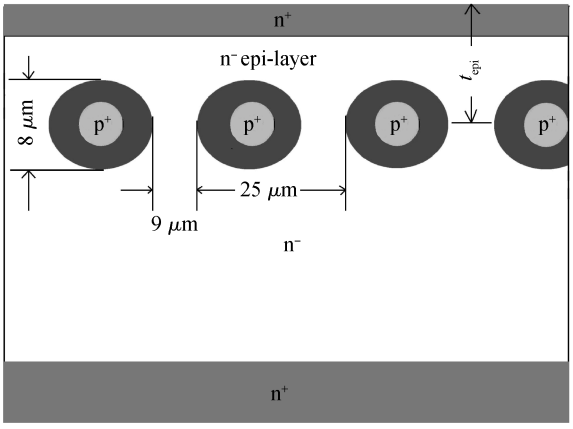

Fig. 1. Cross-section of a segment of BSIT with buried gate structure.

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drift region. The point at the end of the channel near the drain is called the intrinsic drain. In order to research the dynamical electrical performances of BSITs, the active region of the BSIT is designed to be surrounded with a deep trench of which the width is 200 μm, and depth is 60 μm, to cut off the various probable parasitical current effects that may degrade the performance of the BSIT (not shown in figure). The technological processes for fabricating the BSIT sample were described in our previous paper[12].

3. Mechanism underlying the dynamical operation of BSIT

A BSIT is a normally-off device, due to the very lightly doped concentration of the epitaxial layer, and very small gate-to-gate space. The channel of the BSIT is pinched off at zero gate bias. It operates in the blocking state when a negative voltage is applied to the gate. With the increase in drain voltage, there is a very small majority carrier current in the device, dominated by the potential barrier in the channel. At this moment, the BSIT operates in single polar mode and exhibits triode-like I–V characteristics with a certain shift along the voltage $V_{\rm D}$ axis. A potential barrier is established in the channel by the built-in electric field of gate-channel pn junction. The channel of the BSIT is entirely occupied by the depletion region. The width of channel is determined by geometric and technological parameters such as gate-to-gate space, diffusion depth and doping concentration of the epitaxial layer. Most of the electrons can not cross the potential barrier, to form the significant drain current $I_{\rm D}$ by only the effect of drain voltage $V_{\rm DS}$, when the forward voltage is not applied to the gate. The channel is pinched off completely. The height of potential barrier is increased and the device operates in the blocking state when a negative voltage is biased to the gate. The blocking voltage for a given gate voltage represents the voltage capability.

The gate-channel pn junction is forwardly biased and the minority carrier holes are injected into the channel when a high positive voltage ($V_{\rm GS} \geqslant 0.45$ V) is applied to the gate. The operating mechanism of the BSIT has been changed radically by the participation of minority carrier holes. With an increase in the gate voltage, more holes are continuously injected into the channel and the corresponding electrons are injected from the source. Electron-hole plasma with a high concentration is formed in the channel and long drift region, generating a prominent conductance modulation effect. The electric field and the voltage drop are very low in this region. A small increase in drain voltage will result in a rapid increase in drain current. The device operates in the conducting state and can conduct a high drain current with a very low voltage drop, referred to as the saturation state. The magnitude of the drain current is modulated by the minority carrier holes being injected from the source region, it is a current controlled device, called bipolar mode, exhibiting pentode-like characteristics.

When a small positive voltage ($0 \leqslant V_{\rm GS} \leqslant 0.45$ V) is biased to the gate, the device operates in the transient process between the single polar and bipolar modes, called the sub-threshold region. Although the gate is positively based, the concentration of minority carrier holes injected from the source region is very low. The drain current $I_{\rm D}$ is mainly predominated by the potential barrier in the channel.

The current of BSIT is mainly predominated by the potential barrier in the channel in single polar mode biased with reverse gate voltage. With the gradual variation in gate voltage from the negative value to the positive, the control mechanism of drain current is transferred from the potential barrier in the channel to the minority carrier injection. The concentrations of minority carrier holes injected from the gate into the channel and the electrons injected from the source are both very low for the forwardly biased small gate voltage ($0 \leqslant V_{\rm GS} \leqslant 0.45$ V), due to the blocking effect of potential barrier. The electrons drift towards the drain along the channel by the effect of drain voltage. There are very few electrons moving into the gate because of the built-in potential of gate-channel pn junction. The ionized impurity charges in the channel are compensated with the injected electrons from the source, equivalent to a decrease in doping concentration in channel. Therefore, the gate voltage required to pinch off the channel, called pinch-off voltage, is decreased. With the increase in gate voltage, a number of holes accumulate near the source end of the channel, reducing the height of potential barrier due to the reflecting effect of n^+n^- junction. The injected minority carrier holes participate in the drain current modulation of the potential barrier. When the positive gate voltage is increased to a critical high level ($V_{\rm GS} \geqslant 0.5$ V), the potential barrier vanishes completely. A conductance modulation region is built in the channel by the injected holes from the gate and the electrons injected from the source, increasing the gate current. A high density plasma of electrons and holes is established in the channel and a certain realm of epitaxial layer, generating a significant conductance modulation effect at the electrical quasi-neutral region where the electric field is very low. At present, it can conduct a high current with very low voltage drop, the BSIT works in the conducting state, realizing the transformation from off-state to on-state.

There are a large number of majority and minority carriers in lightly doped n^- epitaxial layer in conducting state. The holes near the gate are swept into the gate region, whereas, a portion of the electrons in the channel enter the source region, when a negative voltage is biased to the gate. Most of the carriers in the n^- layer are swept out the channel through the gate region (p^+) and the source region (n^+). When the height of potential barrier increases to high enough to block the electrons injected from the source, the drain current is abruptly cut off. The device begins to operate in the blocking state.

4. Switching-off characteristics

The switching-off time $t_{\rm off}$ is the main factor limiting the frequency performance of BSITs. The dynamical equilibrium between a large number of electrons and holes injected from the source and drain regions, respectively, is kept in the channel in the conducting state. The accumulation of carriers in the channel gives rise to the disappearance of the potential barrier, forming the conditions for current transportation. The effective charge neutrality is built in the channel. With the increase in drain voltage $V_{\rm DS}$, the increased accumulation of carriers injected will leading to much heavier conductance modulation effect and a rapid increase in drain current. The switching-off of drain current is realized by the drawing-out process of ac-

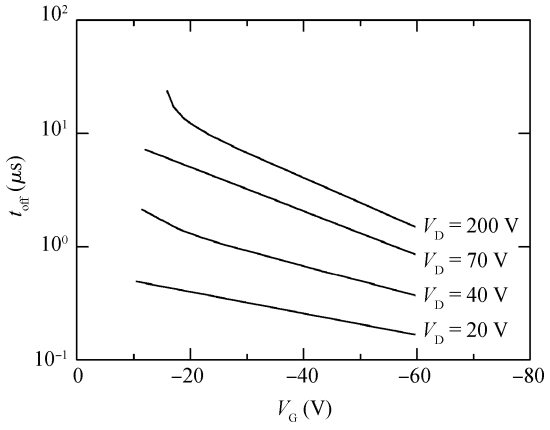

Fig. 2. Dependence of switching-off time t_{off} on V_G and V_D.

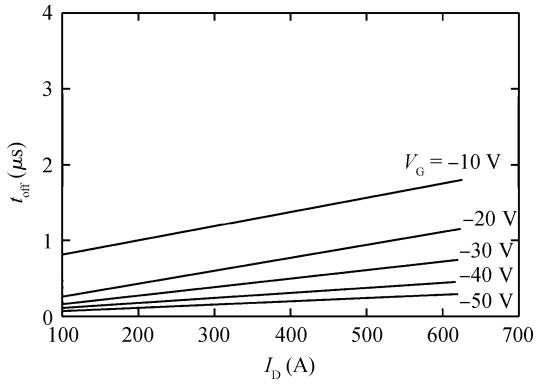

Fig. 3. Dependence of switching-off tome on I_D and V_G.

cumulation carriers in the channel due to a negatively applied gate voltage. With the decrease in accumulated carriers, the potential barrier is gradually established again and the current is cut. The rapid transient process from the conducting state to the blocking state determines the switch frequency performance.

The switching-off process includes three stages. Firstly, a large reverse drawing-off gate current produced by the decrease in gate potential extracts the accumulated charges from the channel, keeping drain current I_D constant. The potential barrier is gradually generated again in the channel due to the vanishing of accumulated charges, resulting in a quick decrease in drain current I_D. Accompanying the continuous recombination of excess carriers in the channel and the drift region, drain current I_D decays exponentially and vanishes eventually.

The switching-off time t_{off} is defined as the time required for the drain current to decrease to 10% of it original value. The switching-off time t_{off} is intimately dependent on the gate drawing-off current, recombination rate and the magnitude of accumulated charges. The degeneration of accumulated charges in the channel can be described with the equation:

$$-\frac{\mathrm{d}Q}{\mathrm{d}t} = I_{GP} + \frac{Q}{\tau_{eff}}, \tag{1}$$

where τ_{eff} is the effective life of carriers in the channel, Q is the magnitude of accumulated charges, Q/τ_{eff} is the recombination current of carriers and I_{GP} is the maximum gate current. Integrating the above equation, the switching-off time t_{off} can be expressed as

$$t_{off} = -\int_{Q_0}^{0} \frac{\mathrm{d}Q}{I_{GP} + \dfrac{Q_0}{\tau_{eff}}} = \tau_{eff} \ln \frac{I_{GP} + \dfrac{Q_0}{\tau_{eff}}}{I_{GP}}$$

$$= \tau_{eff} \ln\left(1 + \frac{I_D}{I_{GP}}\right), \tag{2}$$

where Q_0 is the original charges in the channel at $t = 0$, and $I_D = Q_0/\tau_{eff}$ is the drain current. The dependence of t_{off} on the drain current I_D, drain voltage V_{DS} and gate voltage V_{GS} are experimentally shown in Fig. 2. The switching off time t_{off} is logarithmically dependent on the drain current I_D as shown in Fig. 3. The frequency of the BSIT is mainly determined by the switching-off time t_{off}. With the increase in the maximum gate drawing current I_{GP}, the switching-off time t_{off} is decreased. It is an effective method to increase the maximum gate drawing current I_{GP} for improving the frequency performance of the BSIT. In order to acquire a high gate current I_{GP}, it is necessary to decrease the sheet resistance of gate region by increasing its boron doping concentration. The switching time t_{off} can be effectively reduced by decreasing the lifetime τ_{eff} of carriers as demonstrated in Eq. (2).

5. Theoretical analyses on d*i*/d*t* and d*v*/d*t* capacities

A large varying rate of current ($\mathrm{d}i/\mathrm{d}t$) will be produced in the transient process from the blocking state to the conducting state, since the operating frequency of the BSIT is very high. The $\mathrm{d}i/\mathrm{d}t$ capacity is an important parameter to describe dynamical performance and it is determined both by the vanishing speed of the potential barrier and by establishing the velocity of the conducting channel, determined by the contracting speed of the depletion layer in the channel. The profiles of the depletion layer in the conducting and blocking states are shown in Figs. 4(a) and 4(b), respectively. The width of the conducting channel between the gates can be written as

$$d = 2\left\{\frac{a}{2} - \left[\frac{2\varepsilon\varepsilon_0(V_{GS} + \phi_{in})}{qN_{DCH}}\right]^{1/2}\right\}, \tag{3}$$

where a is the gate-to-gate space, N_{DCH} is the doping concentration in the channel, V_{GS} is the voltage biased to the gate and ϕ is the built-in potential of the gate-channel pn junction.

The width of a BSIT's conducting channel is determined by the doping concentration of the epitaxial layer for a given V_{GS}. A non-uniform channel doping profile will result in a different channel width on chip. The region with a low channel doping concentration, implying wide depletion layer, results in a narrow conducting channel. The current concentration will occur in this region due to the local channel conducting prior to other region, which may degenerate the performance of a BSIT. Furthermore, since the gate stripe has some resistance along the length, even though it is heavily doped with boron impurities, there is a rather voltage drop along the gate stripe from the contact hole to the distant place. Even though the doping concentration is uniform everywhere, the gate voltage V_{GS} can not be biased to the whole gate region at the same time.

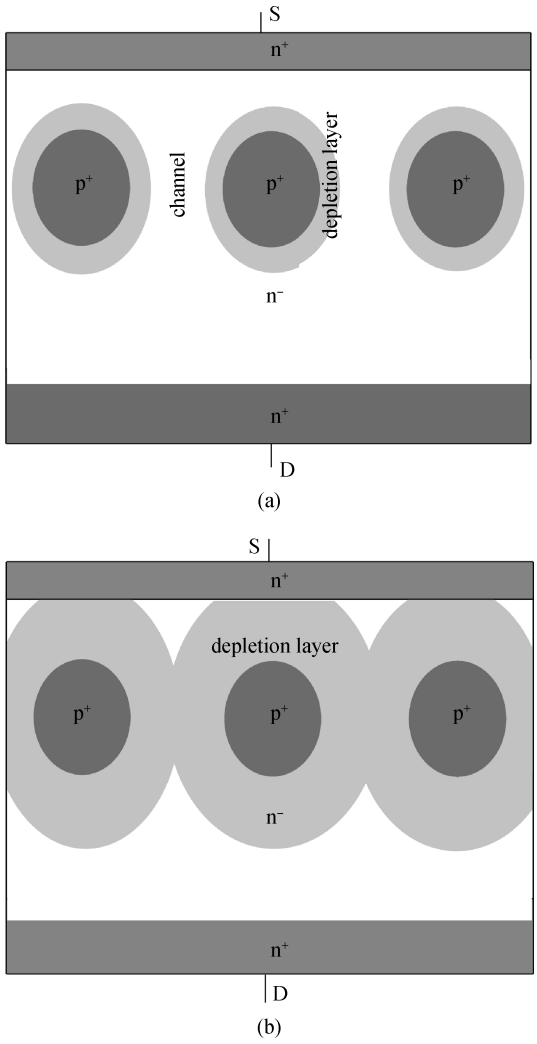

Fig. 4. Profile of the depletion layer at (a) forwardly conducting state and (b) forwardly blocking state.

The BSIT channels can not be switched to the conducting state contemporarily, because of the RC delaying effect. The channel near the contact hole will be conducted prior to the other regions. The conducting current concentrates on the local region near the contact hole at the beginning of conducting process and this may cause catastrophic damage to the BIST.

The raising rate of the voltage at the critical blocking state is described with the $\mathrm{d}v/\mathrm{d}t$ parameter. The BSIT must endure a very high $\mathrm{d}v/\mathrm{d}t$ in switching off process, being equivalent to applying a forward ramping voltage between the drain and source electrodes of the BSIT.

A too large $\mathrm{d}v/\mathrm{d}t$ will deteriorate the switching off performance and operation stability of the BSIT due to the debias effect of gate series resistance, even resulting in that the device can not be switched off. Therefore, it is necessary to improve the $\mathrm{d}v/\mathrm{d}t$ capability of the BSIT. When a reverse current formed by drain voltage cross the gate–drain capacitance C_{GD} flows through the gate–source resistance in the switching off process for a large $\mathrm{d}v/\mathrm{d}t$, a voltage opposite to the gate–source voltage in polarity is generated and the switching off effect of gate–source voltage V_{GS} is weakened, which may even result in miss conductance-on.

6. Analysis on power consumption in dynamical processes

The switching power consumption in dynamical processes can be described with the average power consumption in the conducting period, conducting-on power and switching-off power consumptions. The conducting-on power consumption consists of two parts: delay time and rising time. The switching-off power consumption is generated chiefly in the dropping process and the tail stage. The conducting-on and switching-off power consumptions that are increased with the increase in switching currents can be easily calculated from the switching waveform. With the increase in operation frequency, the power consumption is increased rapidly. The percent of various portions is determined by the operation frequency. In low frequency, the average power consumption in the conducting period is higher than that of switching power consumption. Whereas, in high frequency the switching power consumptions predominate. The driving current of the gate influences the switching power consumption. The high forward driving current will reduce switching speed and delay storage time, giving rise to large switching power consumption in high frequency. The low forward driving current will increase dynamical saturation voltage drop and conducting power consumption. It is of importance to design the driving current of gate electrode correctly.

7. Improvements on the frequency performance

The conducting and blocking states are realized by decreasing and increasing the heights of the potential barrier in the channel. The difference in carrier concentration during the conversion process is higher than 10^9 times. The shorter the time required to complete the conversion process between so different two states, the higher the switching frequency of the BSIT is. A certain time is needed for changing the carrier concentration.

The height of potential barrier in the BSIT channel is lowered by the positive gate voltage in the conducting process. Therefore, the electrons and holes are injected into the channel from the source and gate regions, respectively. The injection of electrons and holes in turn further reduces the height of potential barrier and finally drives the device into the conducting state. Obviously, the conducting time t_{on} is dependent on the original state of the electric field and potential distributions. It is also determined by the diffusion and junction capacitances of the gate–source pn junction. Therefore, it is necessary to decrease the influence of diffusion and junction capacitances in the structural design.

The switching-off time t_{off} is the main factor that influences the frequency performance of a power BSIT. In the switching-off process, firstly, the gate potential barrier is established and raised and then the holes in the channel are drawn out by the negative gate voltage. With the enhancement in the height of potential barrier, the drain electron current I_{DS} quickly decreases to a certain small value I_{R} (referred to as the reverse leakage current). In order to shorten the switching-off time and improve the dynamical performance and frequency, the following technological methods are proposed.

(1) To decrease the effects of diffusion and gate–source pn

junction capacitances, the thickness of the gate region must be reduced to decrease the magnitude of net deposited charges either in the conducting state or in the blocking state. The device can be switched off more quickly, due to the decrease in time for holes to be drawn out.

(2) In order to decrease the number of majority carriers in the drift region in the conducting state, the thickness of the epitaxial layer should be properly reduced. So, the electrons in the drift region can be quickly drawn out by the drain voltage, forming the blocking state.

(3) The establishment and enhancement of the potential barrier in the channel can be promoted with the reverse strong electric field created by increasing the negative gate voltage. The switching-off process can be accelerated by the fast drawing out of electrons and holes.

8. Conclusion

The switching performances of a BSIT, such as $\mathrm{d}i/\mathrm{d}t$, $\mathrm{d}v/\mathrm{d}t$ capabilities and switching power consumption, are the important dynamical parameters of BSITs. The operating frequency is mainly determined by the switching-off time t_{off}, which can be much improved by the proposed technological approaches. The switching-off time t_{off} was reduced from 1 to 0.1 μs by using the technological methods proposed in this paper.

References

[1] Bencuya I, Cogan A J, Butle S J, et al. Static induction transistors optimized for high-voltage operation and high microwave power output. IEEE Trans Electron Devices, 1985, 32(7): 1321

[2] Nishizawa J I, Ohmi T, Chen H L. Analysis of static characteristics of a bipolar-mode induction transistor (BSIT). IEEE Trans Electron Devices, 1982, 29(8): 1233

[3] Wang J, Williams B W. A new static induction thyristor (SITh) analytical model. IEEE Trans Power Electron,1999, 14(5): 866

[4] Ohnuma T, Obonai F, Hayasaka E. Development of high-frequency, high-power static induction transistor for 13 MHz band. Proc 10th Int Symp Static Induction Transistor Devices, Tokyo, 1997

[5] Nishizawa J I, Motoyan K, Itioh A. The 2.45 GHz 36 W CW Si recessed gate type SIT with high gain and high voltage operation. IEEE Trans Electron Devices, 2000, 47(2): 482

[6] Sankin V I, Shrebiy P P, Kuznetsov A N, et al. The development of ultra-high frequency power 6H-SiC vertical static induction transistor with p–n junction as a gate. Mater Sci Forum, 2002, 389–393: 1407

[7] Chen X A, Liu S, Huang Q A. A static induction device manufactured by silicon direct bonding. Semicond Sci Technol, 2004, 19(7): 819

[8] Onose H, Yatsuo T, Watanabe A, et al. Design consideration for 2 kV SiC-SIT. Proc Int Symp on Semiconductor Devices & ICs, Osaka, 2001: 179

[9] Sung Y M, Casady J B, Dufrene J B, et al. A review of SiC static induction transistor development for high-frequency power amplifiers. Solid-State Electron, 2002, 46: 605

[10] Wang Y S, Li S Y, Yang J H, et al. A novel buried-gate static induction transistor with diffused source region. Semicond Sci Technol, 2004, 19: 152

[11] Wang Y S, Li H R, Wu R, et al. Mechanism of reverse snapback on I–V characteristics of power SITH with buried gate structure. Journal of Semiconductors, 2008, 29(3): 101

[12] Wang Y S, Luo X L, Li H R, et al. Improvements on radiation-hardened performance of static induction transistor. Science in China Series F: Information Sciences, 2010, 53(5): 1089