GIDL current degradation in LDD nMOSFET under hot hole stress*

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Abstract: The degradation of gate-induced drain leakage (GIDL) current in LDD nMOSFET under hot holes stress is studied in depth based on its parameter $I_{\rm DIFF}$. $I_{\rm DIFF}$ is the difference of GIDL currents measured under two conditions of drain voltage $V_{\rm D} = 1.4$ V and gate voltage $V_{\rm G} = -1.4$ V while $V_{\rm DG}$ is fixed. After the stress GIDL currents decay due to holes trapping in the oxide around the gate-to-drain overlap region. These trapped holes diminish $\Delta E_{\rm X}$ which is the deference of the lateral electrical field of these two symmetrical measurement conditions in the overlap region so as to make $I_{\rm DIFF}$ lessening. $I_{\rm DIFF}$ extracted from GIDL currents decreases with increasing stress time t. The degradation shifts of $I_{\rm DIFF,\,MAX}$ ($\Delta I_{\rm DIFF,\,MAX}$) follows a power law against t: $\Delta I_{\rm DIFF,\,MAX} \propto t^m$, $m = 0.3$. Hot electron stress is performed to validate the related mechanism.

Key words: GIDL; hot hole; LDD; band-to-band
DOI: 10.1088/1674-4926/32/11/114001 **EEACC:** 2530; 2560R

1. Introduction

Gate-induced drain leakage (GIDL) current originates from the gate-drain overlap region and is easily affected by the trapped charge and interface states in this region[1]. Reference [2] found that GIDL current increases after hot electron injection. Lo *et al*. show that the oxide trapped charge has different effect on GIDL current from the interface state[3]: the oxide trapped charges shift the flat-band voltage and interface states introduce the trap-assisted GIDL tunneling current.

As the effective channel length of MOSFET decreases sharply, the ratio of gate-to-drain overlap to whole device's size becomes larger. Meanwhile, the maximal lateral electric field moves from channel on the gate-to-drain region because the light drain doping (LDD) structure is adopted. These two factors lead to the gate-to-drain overlap of LDD MOSFET suffering more severe hot carrier damage than before[4, 5]. Because the GIDL current is sensitive to the damage in this region, using GIDL current to evaluate the damage should be very effective. A lot of interest has been focused on this field. Cheng studied the anneal of LDD nMOSFET's damage in hydrogen or deuterium based on the GIDL current[6]. Recently, Hu[7] discussed HCI effects on ultra-thin LDD nMOSFET through GIDL current degradation and Reference [8] also used this method to investigate the oxide degradation under alter stresses in the LDD nMOSFET's. However, all of them only focused on the varieties of current value of certain point at GIDL current curve pre and post the stress and cannot have a further research on this GIDL current degradation itself.

In our previous paper[9], we proposed a parameter $I_{\rm DIFF}$ of GIDL current and used it to study the influence of gate voltage $V_{\rm G}$ and drain voltage $V_{\rm D}$ on GIDL current. $I_{\rm DIFF}$ is the difference of GIDL currents measured under two conditions at the constant $V_{\rm DG}$: in one condition $V_{\rm D}$ is fixed and in another's $V_{\rm G}$ is fixed while $V_{\rm D} = |V_{\rm G}|$.

Based on the parameter $I_{\rm DIFF}$ of GIDL current, this paper studies the degradation of GIDL current deep in LDD nMOSFET damaged by the hot holes stress (HHS). The mechanism and the characteristics of degradation are discussed. Hot electron stress (HES) is also used to validate the related mechanism.

2. Devices and experiments

The devices used in this study were LDD nMOSFETs with n^+ poly-Si fabricated by 90 nm CMOS technology. The gate oxide thickness $T_{\rm ox}$ was 4 nm with decoupled-plasma-nitridation (DPN) processing and the gate length L was 0.16 μm. HHS was performed at condition: $V_{\rm G} = V_{\rm TH} = 0.45$ V, $V_{\rm D} = 2.5$ V. Stress was interrupted at regular intervals (200, 400, 600, 800 and 1000 s) while GIDL current was measured. The whole stress time was 1000 s. GIDL currents $I_{\rm GIDL}$ were the drain currents measured at $V_{\rm D} = 1.4$ V with sweeping $V_{\rm G}$ from 0 to -1.4 V and also measured at $V_{\rm G} = -1.4$ V with sweeping $V_{\rm D}$ from 0 to 1.4 V, respectively. All the electrical tests were performed by using a Keithley 4200 precision semiconductor parameter analyzer. In addition, Silvaco software was applied to simulate the electrical field under the stress condition in the device for analyzing degradation.

3. Results and discussion

Figure 1(a) shows the $I_{\rm GIDL}$–$V_{\rm D}$ curves at $V_{\rm G} = -1.4$ V and $I_{\rm GIDL}$–$V_{\rm G}$ curves at $V_{\rm D} = 1.4$ V pre and post HHS. After hot holes are injected in the oxide, it can be seen that $I_{\rm GIDL}$ curves shift downwards and shifts much more as the stress time increases. This shift arises from the reason as follows:

* Project supported by the Specialized Research Fund of the Education Department of Shaanxi Province, China (No. 11JK0902) and the Innovational Fund for Applied Materials of Xi'an, China (No. XA-AM-201012).
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Received 26 April 2011, revised manuscript received 17 July 2011

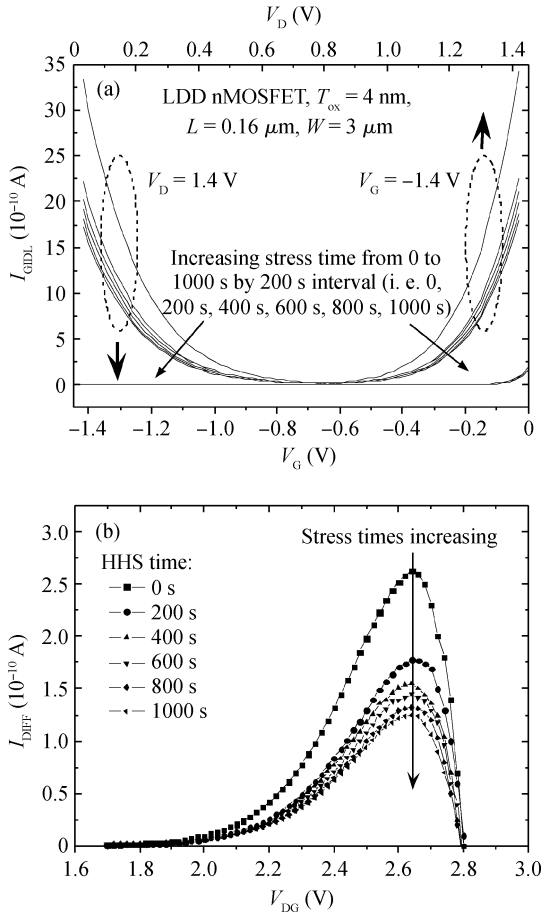

Fig. 1. (a) I_{GIDL}–V_G curves at V_D = 1.4 V and I_{GIDL}–V_D curves at V_G = −1.4 V pre and post HHS. The HHS condition is: V_G = V_{TH} + 0.45 V, V_D = 2.5 V. (b) I_{DIFF}–V_{DG} curves extracted from GIDL current pre and post HHS.

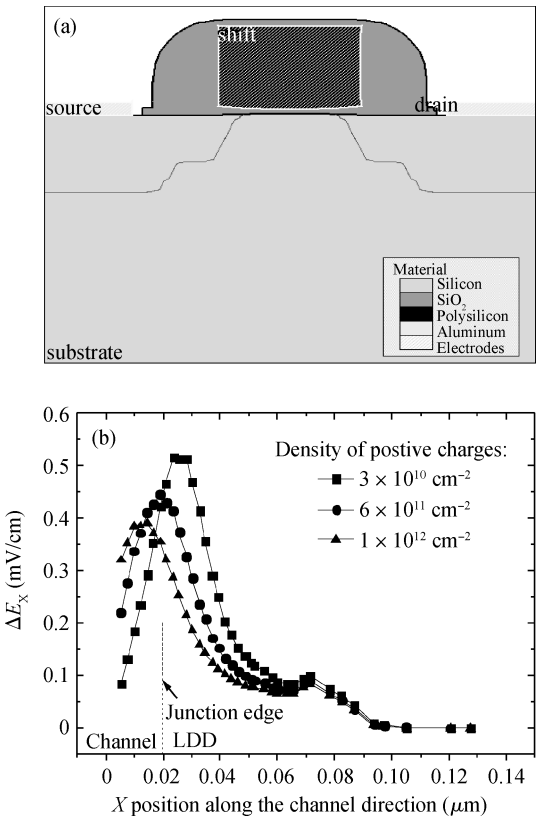

Fig. 2. (a) Schematic structure of the LDD nMOSFET (L = 0.16 μm, T_{ox} = 4 nm) simulated with Silvaco software. (b) Simulated distribution ΔE_X of $I_{DIFF,MAX}$ along the channel direction while the positive charges are trapped in oxide of the overlap region.

the trapped holes make silicon surface field in the overlap region decrease so as to make the electron tunneling length increase. Then the band-to-band tunneling (BBT) monishes and the GIDL current relying on BBT decay. The decay of I_{GIDL} increases with the trapped holes increasing as stress time continues. From Fig. 1(a), it is also found that the GIDL currents after stress do not enhance in the low V_G region and low V_D region, respectively. Namely, there are few or no interface states generated in this HHS and so trap assistant BBT cannot take place to enhance the GIDL current.

For studying the degradation of GIDL current deeply, we adopt the conception of the parameter I_{DIFF} of GIDL current mentioned in Ref. [9]. In the case of this letter, I_{DIFF} equals the value of the GIDL current in I_{GIDL}–V_G curve at V_D = 1.4 V minus that in I_{GIDL}–V_D curve at V_G = −1.4 V under constant V_{DG}. GIDL current composes of electron tunneling and hole tunneling current. GIDL electron tunneling current part related with whole electrical field keeps invariable under the constant V_{DG}. However the different V_D in the two measurement conditions above under the constant V_{DG} results in the different lateral electrical field and the GIDL hole tunneling current part relying on the lateral electrical field is different. Thus the whole GIDL currents in these two symmetrical conditions are not same and I_{DIFF} reflects the difference. Further, this difference of lateral electrical field of the two measurement conditions under constant V_{DG}, defined as ΔE_X, induces the diverse hole-tunneling and leads to the appearance of I_{DIFF}. It is well known that the damage of device during stress often occur in the maximum electrical field[10]. So hole trapping occurs in the oxide at the interface of the LDD region during HHS because the maximum electrical field of LDD nMOSFET locates in this region. These trapped holes affect the lateral electrical field. Accordingly, they change ΔE_X and make I_{DIFF} vary. I_{DIFF} increases with increasing ΔE_X and vice versa. Figure 1(b) is the I_{DIFF}–V_{DG} curves extracted from GIDL current pre and post stress. It shows that the I_{DIFF} curve's peak $I_{DIFF,MAX}$ around V_{DG} = 2.6 V decreases and the whole curve shift downwards as the stress time increases from 0 to 1000 s. On the basis of discussion above, the trapped holes should induce ΔE_X decrease and then I_{DIFF} decreases.

In order to assure whether ΔE_X decrease due to holes trapping, we simulate ΔE_X of two dimension (2D) in the overlap region pre and post HHS. The simulated LDD nMOSFET has the same 2D structure of T_{ox} = 4 nm and L = 0.16 μm as the experimental device, as shown in Fig. 2(a). Because $I_{DIFF,MAX}$ is around at V_{DG} = 2.6 V, so here ΔE_X is expressed as the difference of the lateral electrical fields at the condition of V_D = 1.4 V/V_G = −1.2 V and at that of V_D = 1.2 V/V_G = −1.4 V under V_{DG} = 2.6 V. Since the reportorial maximum density of trapped positive charges generated during the HHS stress in the oxide approaches the magnitude of 10^{12} cm^{-2}[11, 12], the density of trapped positive charges located in the oxide of gate-to-drain overlap region is set to increase from 3 × 10^{10} to 1 ×

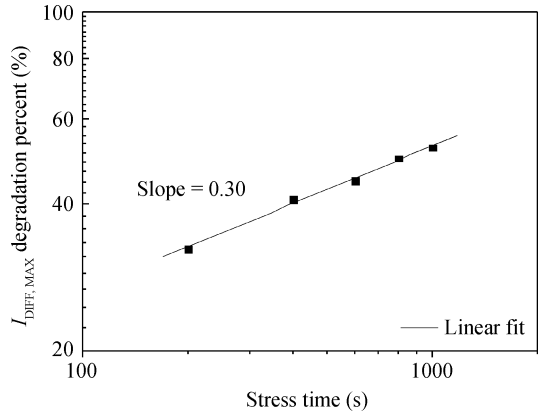

Fig. 3. $I_{DIFF, MAX}$ degradation varies with stress time at the double logarithmic coordinate.

10^{12} cm^{-2} during the simulation. Figure 2(b) shows the distribution of ΔE_X of $I_{DIFF, MAX}$ along the channel direction after hot holes(positive charges) are trapped in oxide of the overlap region. From Fig. 2(b), it can be seen that ΔE_X curve shifts downwards and its peak lowers while increasing the density of trapped positive charges. It can be deduced that more and more positive charges are trapped as stress time is prolonged, lessen and lessen ΔE_X of every certain point of I_{DIFF} curve becomes. Thus the curve of I_{DIFF} shifts downwards according to the relationship of ΔE_X and I_{DIFF}. The simulated result in Fig. 2(b) accounts for the degradation of I_{DIFF} in Fig. 1(b).

$I_{DIFF, MAX}$ are extracted from Fig. 1(b) to describe the effect of HHS on the degradation of I_{DIFF} quantificationally. Figure 3 shows the relationship of $I_{DIFF, MAX}$ degradation with stress time t under double-logarithm coordinate. Notes that $I_{DIFF, MAX}$ degradation varies linearly with stress time under double-logarithm coordinate. Namely, $I_{DIFF, MAX}$ degradation follows a power law against t. This relationship is: $\Delta I_{DIFF, MAX} \propto t^m$, m denotes the slope of line and $m = 0.3$. This degradation equation has the similar form with the threshold voltage V_{TH} under hot carrier stress. Accordingly, $I_{DIFF, MAX}$ can reflect the degradation of device after HHS like V_{TH}.

The discussion on relationship of I_{DIFF} degradation with stress time under HHS above is based on the theory of ΔE_X affecting I_{DIFF} mentioned above. On the assumption that our theory is reasonable, I_{DIFF} should increase while ΔE_X increases. We simulate the situation of hot electron trapping in the oxide of gate to drain overlap region. Since the reportorial maximum density of HES induced trapped negative charges in the oxide also approaches the magnitude of 10^{12} cm^{-2}[11], the density of trapped negative charges is also set from 3×10^{10} to 1×10^{12} cm^{-2} during the simulation. Figure 4(a) shows ΔE_X become larger and larger as the density of trapped negative charges varies from 3×10^{10} to 1×10^{12} cm^{-2}. Also according to the theory of ΔE_X affecting I_{DIFF}, I_{DIFF} should increase. We apply the HES on the LDD nMOSFET with $T_{OX} = 4$ nm, $L = 0.16$ μm and $W = 6$ μm to testify this deduction. The HES condition is set up[13, 14]: $V_G = V_D = 2.5$ V. The experiment shows that I_{DIFF} curve shifts upwards while HES time increases from 0 to 200 s to 600 s, as can be seen in Fig. 4(b). As we known, longer and longer the stress time, more and more electrons are trapped. So the experiment indicates that I_{DIFF} increases with increasing trapped hot electrons (negative charges).

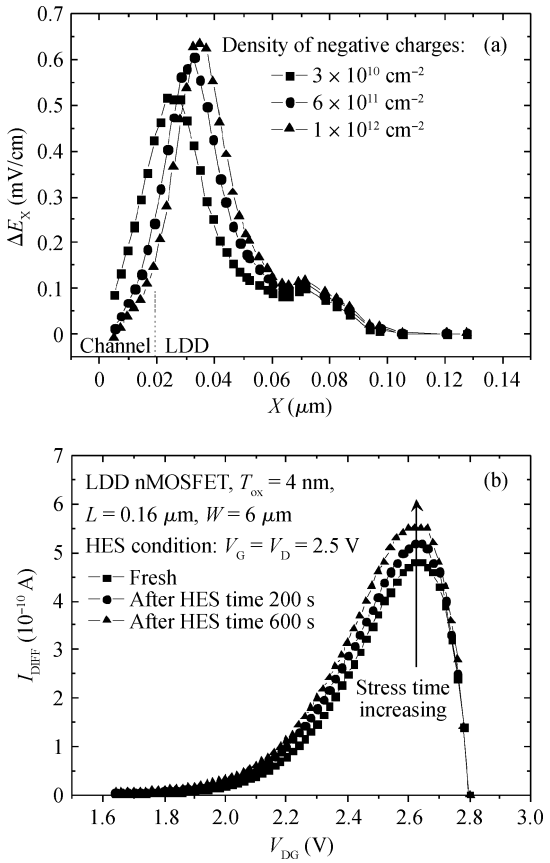

Fig. 4. (a) Distribution ΔE_X of $I_{DIFF, MAX}$ along the channel direction simulated with Silvaco software while the negative charges are trapped in oxide of the overlap region. (b) I_{DIFF}–V_{DG} curves extracted from GIDL current pre and post HES.

This HES experimental result matches the simulation result well, which sufficiently approves the theory of ΔE_X affecting I_{DIFF} and also indicates that the discussion above on relationship of I_{DIFF} degradation with stress time under HHS is reasonable.

4. Conclusion

This paper studies the degradation of GIDL current deeply in LDD nMOSFET damaged by the HHS through discussing characteristics of the parameter I_{DIFF}. I_{DIFF} is extracted from GIDL current pre and post stress. It decreases with increasing stress time. This ascribes that the holes trapping in the oxide of gate to drain overlap region induce ΔE_X. Consequently I_{DIFF} decreases. The degradation shifts of $I_{DIFF, MAX}$, $\Delta I_{DIFF, MAX}$, follows a power law against stress time t. This relationship is: $\Delta I_{DIFF, MAX} \propto t^m$, $m = 0.3$. Based on the simulation and hot electron experiment result, the mechanism of I_{DIFF} degradation under HHS is approved. I_{DIFF} provides another way to analyze GIDL current degradation further. Although this way deals with the case without interface states, it still should be helpful to study this current degradation in the gate-to-drain overlap region of LDD nMOSFET.

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