A novel 2-T structure memory device using a Si nanodot for embedded application*

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Abstract: Performance and reliability of a 2 transistor Si nanocrystal nonvolatile memory (NVM) are investigated. A good performance of the memory cell has been achieved, including a fast program/erase (P/E) speed under low voltages, an excellent data retention (maintaining for 10 years) and good endurance with a less threshold voltage shift of less than 10% after 10^4 P/E cycles. The data show that the device has strong potential for future embedded NVM applications.

Key words: nonvolatile memory; nanocrystal; reliability
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1. Introduction

The scaling down of conventional floating gate memories for embedded applications is becoming more and more difficult[1]. The use of high voltage to program or erase increases power consumption, process complexity and reliability concerns. Similarly, the generation of high voltage leads to a relatively large module size. Therefore, operation voltage reduction is a very important driver for embedded memory scaling. However, voltage scaling always results in a degradation of retention performance due to oxide thickness reduction. Several new technologies, such as SONOS[2] and MANOS[3], have been explored to overcome this dilemma over the past few years. However, reliability, especially data retention, is still an issue for these devices.

Nanocrystal (NC) nonvolatile memory (NVM) is one of the promising candidates to reduce operation voltage without compromising the data retention[4–6]. The memory cells can be operated with a maximum on-chip voltage of 4.5 V because of the reduction of tunneling oxide thickness. At the same time, the memory still maintains excellent data retention performance due to discrete charge storage. It also has merits of high reliability, low cost and compatibility with CMOS processes[5,6]. Several groups have developed different types of Si-NC devices. Of them, one transistor (1T) and split-gate (1.5T) are the most used ones due to their compatibility with CMOS technology. Tiwari[7] firstly developed 1T structure Si-NC NVM and verified its potential application in embedded systems. Yater *et al.*[8] proposed split-gate (1.5T) Si-NC NVM and obtained a more than 2 V storage window. However, the 1T structure is limited by an over-erase problem and the 1.5T structure by process complexity. In this work, for the first time, a 2T structure nanocrystal NVM is proposed to estimate its potential for future embedded NVM application. It is shown that this type of NVM has advantages of process simplicity and over-erase immunity to reduce the read-out circuit complexity[9–11].

2. Cell design and fabrication

Figure 1 illustrates the schematic layout and the cross sectional view of a 2T NC memory cell. The device consists of two N-channel transistors connected in series: one is the select transistor with a thick gate oxide and the other is the NC memory transistor for data storage. A select transistor is used to open the whole channel to read the data in the NC memory transistor. It also can prevent read error caused by over-erase. This architecture uses Fowler–Nordheim (FN) tunneling to realize P/E operations[9]. The sizes of these two transistors are $W/L = 0.32\ \mu$m/0.17 μm and 0.32 μm/0.24 μm, respectively. The total area of a cell is 0.475 μm^2 under a 0.18 μm standard process.

The fabrication of the 2T NC NVM followed a conventional logic process, as shown in Fig. 2. The process flow is simple. The integration of the NC into conventional CMOS flow can be accomplished with the addition of only four non-critical masks over the baseline logic process. After trench isolation and well implantation, a charge storage stack is formed consisting of a 3.5-nm-thick thermal grown tunnel oxide, 20-nm-diameter NCs and 11-nm-thick HTO as the top blocking oxide. Formation of Si-NCs is very critical and is realized by a two-step LPCVD process, which has advantages of good control and excellent compatibility with CMOS technology[12]. The size and density of Si-NC can be controlled by adjusting growth time and temperature. Figure 3 gives a scanning electron microscope (SEM) image of Si-NCs with a density of about 1.2×10^{11} cm^{-2} and an average diameter of 20 nm. Next, a mask is used to define the NC-transistor area and the three

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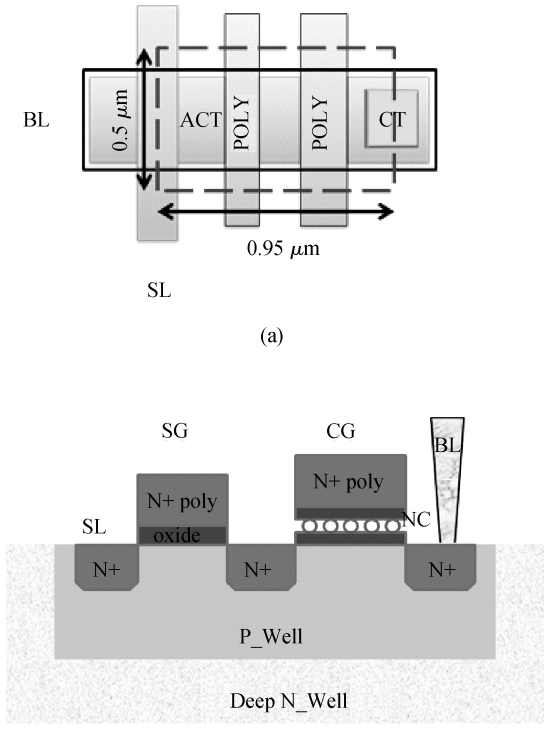

Fig. 1. (a) Schematic layout and (b) cross sectional view of a 2T NC NVM.

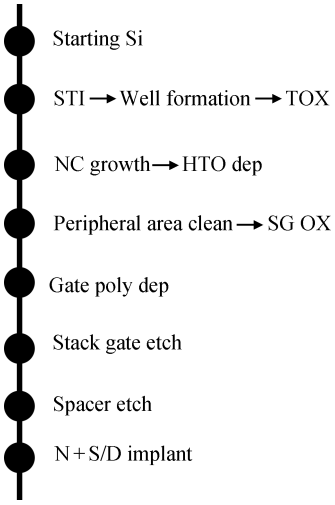

Fig. 2. Simplified process flow of 2T NC NVM.

stacked layers in other places are etched away. After cleaning, the select transistor gate oxide is grown. Then, a 180-nm-thick gate polysilicon layer is deposited and followed by a dry etch to form the whole transistor gate stack. Finally, spacer formation and source/drain implantation were performed to complete the device.

3. Result and discussion

The charging characteristic of Si nanocrystals embedded in silicon oxide is analyzed by drain current–gate voltage (I_d–V_g) measurement at room temperature, as shown in Fig. 4.

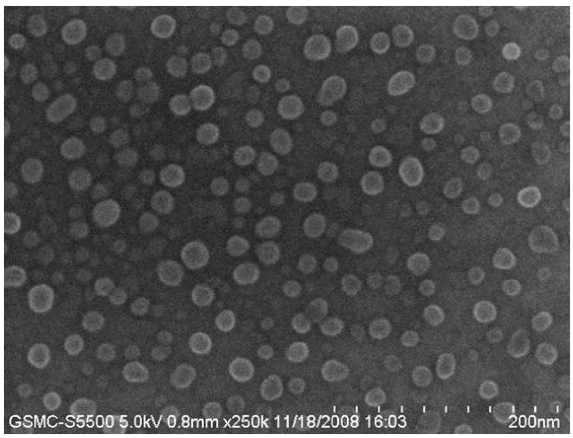

Fig. 3. SEM cross sectional view of 20-nm Si-NCs with a density of 1.2×10^{11} cm^{-2}.

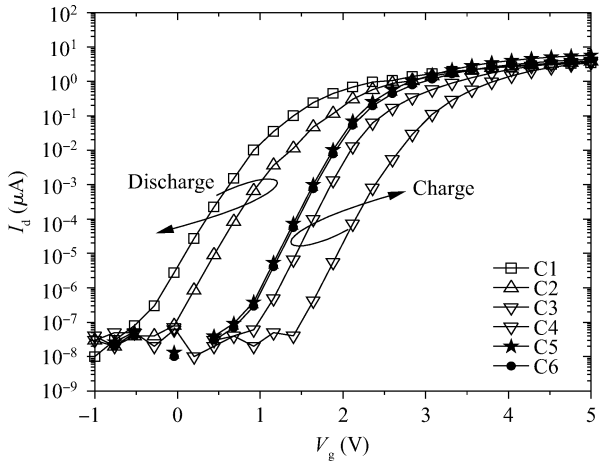

Fig. 4. I_d–V_g curves for 2T NC NVM. Solid dots are for sample without NC and hollow dots for sample with NC.

The measurement is carried out by sweeping V_{cg} from a negative voltage to a positive voltage with $V_d = 0.1$ V in both programmed and erased states to extract the memory window. The P/E operations are realized by FN tunneling, as listed in Table 1, where $V_{cg}/V_{sg}/V_s/V_d/V_b$ stands for the voltages of the control gate, select gate, source, drain and substrate, respectively. As can be seen that for the control sample without NCs (solid dots), the I_d–V_g curves in the programmed and erased states almost merge together and exhibit a zero storage window. In contrast, a large memory window is observed in the sample with Si-NCs. The observed memory window is attributed to the electron charging and discharging of Si-NCs. As indicated in Fig. 4, the left branches represent electron discharge while the right branches represent electron charging.

As the memory window is strongly dependent on the P/E voltages, the P/E speed is further measured under various control gate voltages. Figure 5 presents the FN P/E speed characteristics at various program and erase voltages. FN tunneling is used for both program and erase. To reduce periphery circuit loading, a positive voltage is applied to the control gate during programming and a negative voltage is applied to the p-well (substrate) during erasing. The schematic energy band diagrams for programming and erasing are shown in Fig. 6. Dur-

Table 1. Operation conditions for P/E.

	Sample	V_{cg} (V)	V_{sg} (V)	V_d (V)	V_s (V)	V_b (V)	t (ms)
C1	With NC	−4.5	4.5	4.5	4.5	4.5	5
C2	With NC	−2.5	4.5	4.5	4.5	4.5	5
C3	With NC	2.5	−4.5	−4.5	−4.5	−4.5	5
C4	With NC	4.5	−4.5	−4.5	−4.5	−4.5	5
C5	Without NC	−4.5	4.5	4.5	4.5	4.5	5
C6	Without NC	4.5	−4.5	−4.5	−4.5	−4.5	5

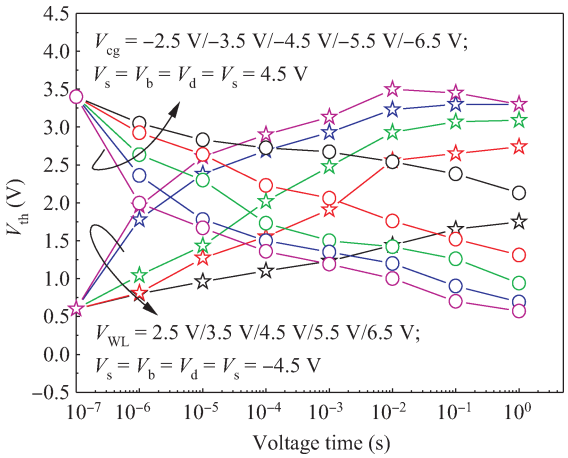

Fig. 5. P/E speed characteristics of NC NVM.

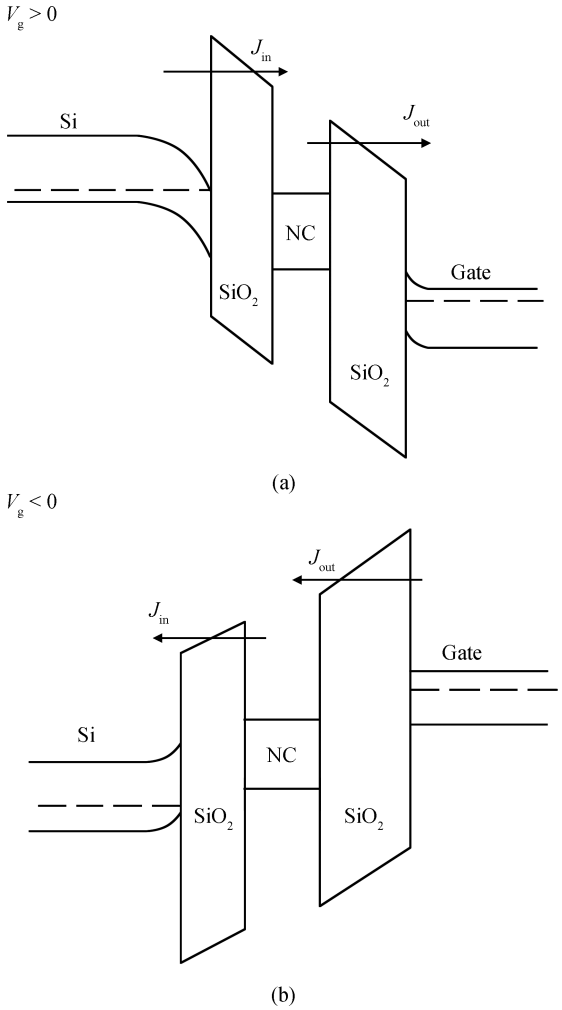

Fig. 6. Schematic energy band diagram when (a) programming and (b) erasing.

ing programming, the positive gate bias leads to electron injection from the inverted channel into Si-NCs. At the same time, electrons leak from Si-NCs to the poly gate, across the interpoly oxide layer[13]. In erase mode, the devices can be erased by electron de-trapping from the nanocrystals. The memory window is determined by the tunneling current densities of both into NCs (J_{in}) and out of NCs (J_{out}). It can be observed that both program and erase speed increase with increasing P/E voltage and tend to saturate eventually. This is because of the balance between J_{in} and J_{out}[13]. Based on P/E speed and reliability considerations, "$V_{cg} = 4.5$ V; $V_{sg} = V_b = V_d = V_s = -4.5$ V, $T = 5$ ms" and "$V_{cg} = -4.5$ V; $V_{sg} = V_b = V_d = V_s = 4.5$ V, $T = 5$ ms" are chosen as the typical program and erase operation conditions, respectively. As shown in Fig. 5, a larger than 1.7 V window can be obtained under typical operation conditions. As the maximum on-chip-voltage is only 4.5 V, high voltage transistors are not needed, thus the process flow is simplified and a great deal of the periphery module area is saved.

The endurance characteristic of the NC memory cell is shown in Fig. 7. The data were measured under typical P/E conditions, as shown above. There is a small increase of programmed V_{th} about 0.2 V after 10^4 cycles, which is mainly due to traps generated in the tunnel oxide or at the silicon surface during the cycling. The programmed state has a larger V_{th} shift than the erased state possibly due to the reason that more traps in tunnel oxide are charged in the programmed state. After 10^4 P/E cycles, the memory window shows only slight degradation.

In order to analyze the charge retention capacity of 2T NC NVM, V_{th} versus time (V_{th}–t) measurement is performed under 150 ℃ to accelerate the charge loss. One of the main advantages of NC NVM is the potential good data retention. Due to discrete charge storage, it is expected that a current leakage path in the tunneling oxide of one NC does not cause the charges in other NCs to leak. Thus, NC NVM can still maintain a good retention even when the tunnel oxide thickness is very thin. The normalized V_{th}–t curve in Fig. 8 for a NC cell at 150 ℃ proves that the above expectation is the case. The cell had a fresh $V_{th} = 1.2$ V and then programmed to $V_{th} = 2.5$ V. It can be seen that V_{th} decreases with time due to the charge loss from the Si-NC memory cell. After 10^4 s (equivalent to about 10 years at room temperature[14]), the NC memory cell has a charge loss of less than 15%, which guarantees high performance NVM applications.

To further evaluate the performance of 2T NC memory,

Table 2. Comparisons between our sample and 2T SONOS[15].

Parameter	Program Voltage (V)	Erase Voltage (V)	Storage window (V)	Endurance (V_t shift after 10^5 cycles) (V)	Data retention
SONOS	13	–13	3	1	Lost 0.7 V after 10^5 s at 20 ℃
Si-NC	9	–9	1.7	0.2	Lost 0.3 V after 10^5 s at 150 ℃

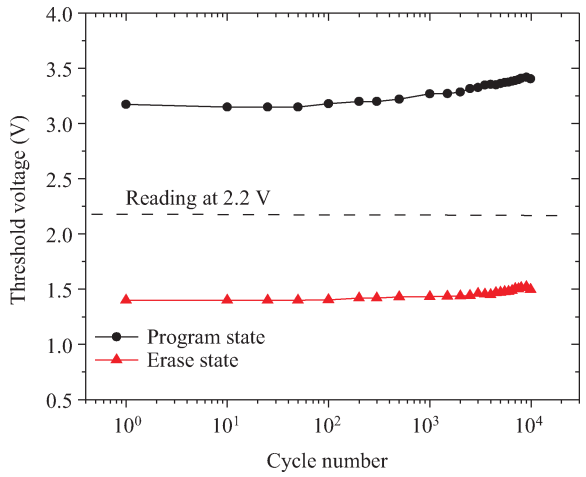

Fig. 7. Endurance characteristics with typical P/E conditions.

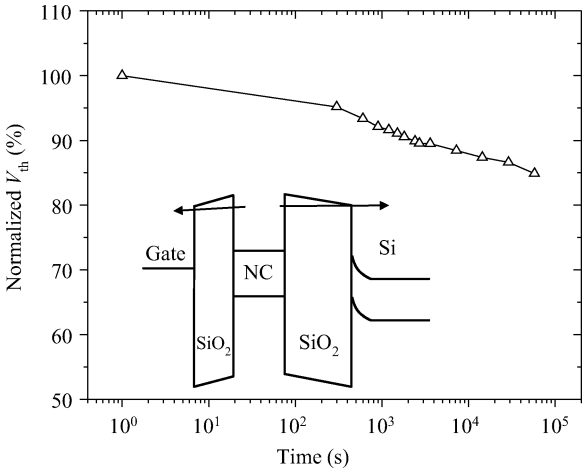

Fig. 8. Data retention for 2T NC NVM at 150 ℃.

we made a comparison between our sample and 2T SONOS in terms of storage window, endurance and data retention in Table 2[15]. Both of these two devices use low voltage FN/FN operation and have a similar P/E mechanism. Though a larger storage window SONOS is observed, its data retention is much worse than nanocrystal. In the SONOS structure, stored charges can easily de-trap from the shallow trap level of Si_3N_4 and then leak out through the small band offset of Si_3N_4/SiO_2. In nanocrystal, the higher band offset to SiO_2 can strongly suppress the tunneling current both to the substrate and the gate[2], so better retention can be achieved. Also, because of a thicker bottom oxide is no solution for SONOS devices due to erase saturation[16, 17], the SONOS has to reduce tunneling oxide as to below 20 A, which causes a severe charge loss problem, as Table 2 shows.

4. Conclusion

In this paper, a new 2T nanocrystal memory with low operation voltage and high reliability is demonstrated. The device process is simple and fully compatible with conventional CMOS technology. As a thinner tunneling oxide used, the operation voltage is distinctly reduced. This device shows excellent performance in terms of endurance and data retention, and also with an acceptable storage widow of 1.7 V, which makes the nanocrystal NVM suitable for the next generation of high performance embedded NVM applications.

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