Ultra-low specific on-resistance SOI double-gate trench-type MOSFET*

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Abstract: An ultra-low specific on-resistance ($R_{on,sp}$) silicon-on-insulator (SOI) double-gate trench-type MOSFET (DG trench MOSFET) is proposed. The MOSFET features double gates and an oxide trench: the oxide trench is in the drift region, one trench gate is inset in the oxide trench and one trench gate is extended into the buried oxide. Firstly, the double gates reduce $R_{on,sp}$ by forming dual conduction channels. Secondly, the oxide trench not only folds the drift region, but also modulates the electric field, thereby reducing device pitch and increasing the breakdown voltage (BV). A BV of 93 V and a $R_{on,sp}$ of 51.8 mΩ·mm^2 is obtained for a DG trench MOSFET with a 3 μm half-cell pitch. Compared with a single-gate SOI MOSFET (SG MOSFET) and a single-gate SOI MOSFET with an oxide trench (SG trench MOSFET), the $R_{on,sp}$ of the DG trench MOSFET decreases by 63.3% and 33.8% at the same BV, respectively.

Key words: double gates; trench; specific on-resistance; breakdown voltage
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1. Introduction

There is a super-linear relationship of $R_{on,sp} \propto BV^{2.5}$ between the specific on-resistance ($R_{on,sp}$) and breakdown voltage (BV) of lateral power devices, the trade-off between $R_{on,sp}$ and BV is thus the main issue for power MOSFETs[1,2]. Reduced surface field (RESURF) technology is traditionally used to improve the trade-off[3]. An oxide trench can modulate the drift electric field and enhance the RESURF effect, thereby increasing the BV and reducing $R_{on,sp}$[4−6]. Channel resistance accounts for a large proportion in $R_{on,sp}$ for medium- and low- voltage devices. A trench gate MOSFET can reduce channel resistance and eliminate the junction field effect transistor (JFET) effect, resulting in a reduced $R_{on,sp}$[7]. Double gates can further reduce $R_{on,sp}$[8]. Three structures have been proposed in which the gate and source or the gate and drain were placed in one trench thereby reducing the cell pitch and $R_{on,sp}$[9−11].

We propose a novel double-gate SOI trench-type MOSFET to further decrease $R_{on,sp}$. The double gates reduce $R_{on,sp}$ by forming dual conduction channels. The oxide trench improves the BV as well as decreasing $R_{on,sp}$ by reducing device pitch. Three merits are noted in a comparison with conventional SOI lateral MOSFETs: (1) $R_{on,sp}$ is reduced dramatically due to the double gates and the oxide trench; (2) the BV is increased because the oxide trench modulates the electric field in the drift region; (3) junction isolation and the dielectric isolation process in conventional power integrated circuits are removed due to the extended trench gate.

2. Structure and mechanism

Figure 1 shows the schematic cross section of a DG trench MOSFET, an SG trench MOSFET and an SG MOSFET. For DG and SG trench MOSFETs, an oxide trench is placed in the drift region to share the voltage drop in Figs. 1(a) and 1(b). Compared with an SG trench MOSFET, a DG trench MOSFET has an extra trench gate in the oxide trench and thus an extra conduction channel. W_T and D_T are the width and depth of the oxide trench. T_S and N_d are the thickness and doping concentration of the SOI layer. T_I is thickness of the buried oxide layer.

In a DG trench MOSFET and an SG trench MOSFET, the drift region is folded in the vertical direction by the oxide trench, reducing the cell pitch. The equivalent drift region length, $L_{d,eq}$, is determined by the depth and width of the oxide trench, that is $L_{d,eq} \approx W_T + 2D_T - D_{p\text{-well}} - D_{drain}$, where $D_{p\text{-well}}$ is the depth of the p-well and D_{drain} is the depth of the drain junction.

In the on-state, the DG trench MOSFET forms dual conduction channels owing to the double gates; furthermore, the drift doping concentration is increased because of the depletion assistance of the oxide trench, $R_{on,sp}$ is therefore reduced. Moreover, the oxide trench reduces cell pitch due to the folded drift region. All of these significantly decrease $R_{on,sp}$ as compared to a conventional lateral power MOSFET. In the off-state, the oxide trench reshapes the electric field in the drift region, so the blocking voltage capability can be enhanced. The equi-potential contours of the DG trench MOSFET at BV =

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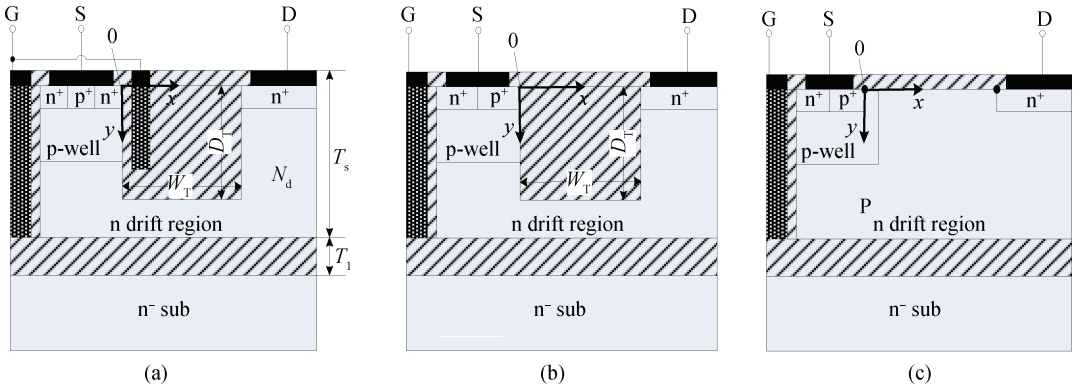

Fig. 1. Schematic cross section of (a) DG trench MOSFET, (b) SG trench MOSFET and (c) SG MOSFET.

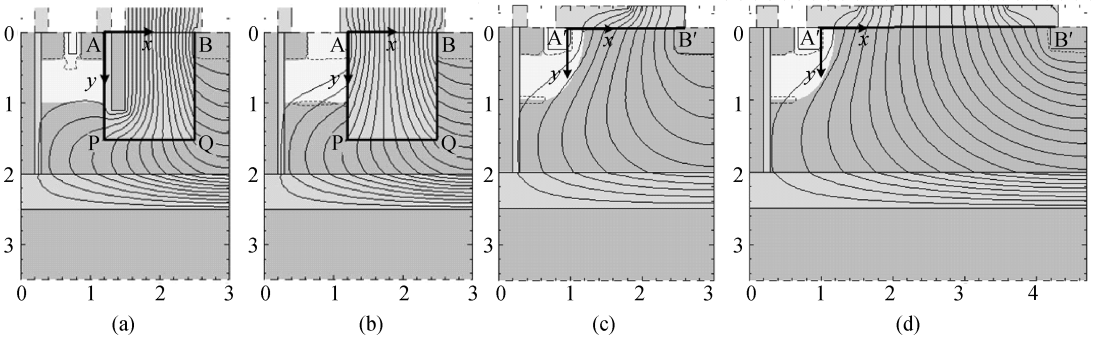

Fig. 2. Equi-potential contours (5 V/contour) at BV for (a) DG trench MOSFET (93 V), (b) SG trench MOSFET (96 V), (c) SG MOSFET (A-type) (49 V), (d) SG MOSFET (B-type) (92 V). ($T_S = 2$ μm, $T_I = 0.5$ μm for all devices, a half-cell pitch of 3 μm for Figs. 2(a)–2(c), a half-cell pitch of 4.7 μm for Fig. 2(d), respectively.) N_d is optimized to obtain the maximum BV for each device.

Table 1. $L_{d,eq}$, optimized N_d, BV and $R_{on,sp}$ for the four devices (note: $R_{on,sp}$ is the specific on-resistance at $V_{GS} = 5$ V).

Device type	Half-cell pitch (μm)	$L_{d,eq}$ (μm)	Optimized N_d (cm^{-3})	BV (V)	$R_{on,sp}$ ($m\Omega\cdot mm^2$)	$BV^2/R_{on,sp}$ (MW/cm^2)
DG trench MOSFET	3.0	3.0	3.5×10^{16}	93	51.8	16.697
SG trench MOSFET	3.0	3.0	3.0×10^{16}	96	78.2	11.785
SG MOSFET (A-type)	3.0	1.3	1.3×10^{16}	49	63.1	3.805
SG MOSFET (B-type)	4.7	3.0	0.8×10^{16}	92	141.0	6.003

93 V is shown in Fig. 2(a). The strong RESURF effect can be observed along the drain pillar and underneath the oxide trench.

3. Results and discussion

Figure 2 shows the potential distribution of the DG trench MOSFET, the SG trench MOSFET and the SG MOSFET at breakdown. Herein SG MOSFETs are divided into A-type and B-type, an A-type MOSFET with a 3 μm half-cell pitch is shown Fig. 2(c) and a B-type MOSFET with a 4.7 μm half-cell pitch is shown in Fig. 2(d). For an A-type MOSFET, the equi-potential contours are crowded at the Si surface, resulting in a high electric field and thus premature breakdown in the Si surface. To release the crowding equi-potential contours, one way is to increase the length of the drift region, which will result in an increase in cell pitch and $R_{on,sp}$ (in Table 1). Another effective way is to inset an oxide trench in the drift region in case the high electric field is located the oxide thereby avoiding premature breakdown, because silicon dioxide has a low relative permittivity and a high critical field, as given in Fig. 2(b). From Fig. 2, it is observed that the voltage drop along the Si surface (AB line) is equal to the one around the oxide trench (APQB line), which indicates that the oxide trench folds the drift region and reduces the device pitch. In order to further reduce $R_{on,sp}$, a trench gate is inset in the oxide trench to form dual conduction channels, as shown in Fig. 2(a). It is very important for low- and medium-voltage power MOSFETs.

Figure 3 shows the electric field distributions on the Si surface and around the oxide trench for DG and SG trench MOSFETs, as well as the surface field distributions for A- and B-type SG MOSFETs. In Fig. 3(a), it is observed that the oxide trench modulates the electric field of the drift region. New electric fields are therefore formed at the corners of the oxide trench, which increases the average field strength in the Si region. Figure 3(a) shows that the oxide trench folds the drift region around the oxide trench. From Fig. 3(b), it is also shown that the peak electric field shifts from the surface to the bulk. It is more important that the field strength in the buried oxide

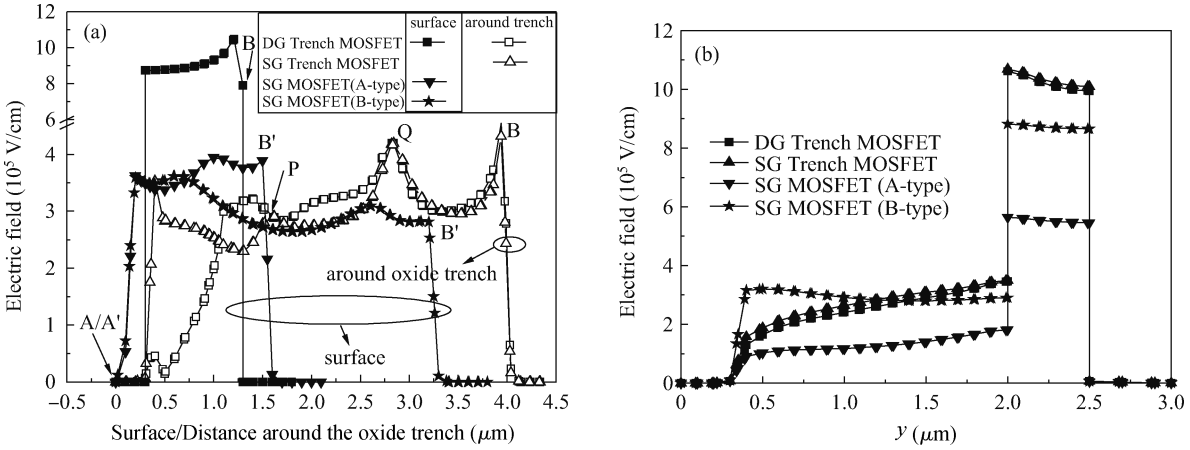

Fig. 3. Field distributions in the (a) surface/around the trench (start point: A'/A shown in Fig. 2) and (b) y-direction (start point: $x = 2.99$ μm for half-cell pitch of 3 μm and $x = 4.69$ μm for half-cell pitch of 4.7 μm).

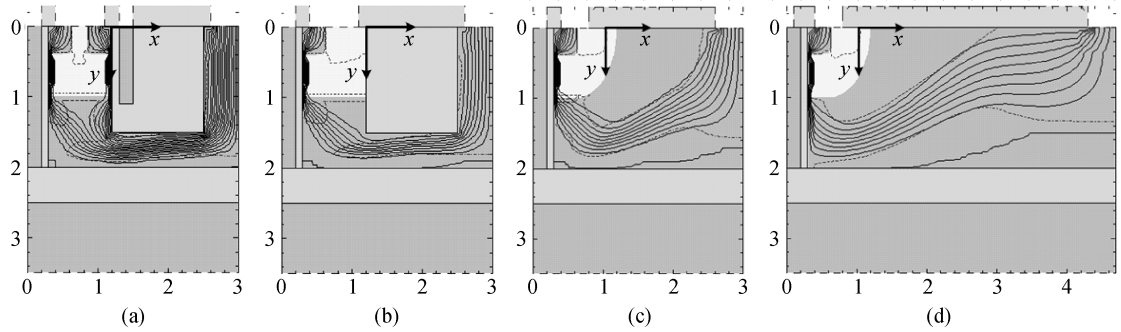

Fig. 4. Current lines contours for (a) DG trench MOSFET, (b) SG trench MOSFET, (c) SG MOSFET (A-type) and (d) SG MOSFET (B-type). (10^{-5} A·μm^{-1}/contour and $V_{GS} = 5$ V).

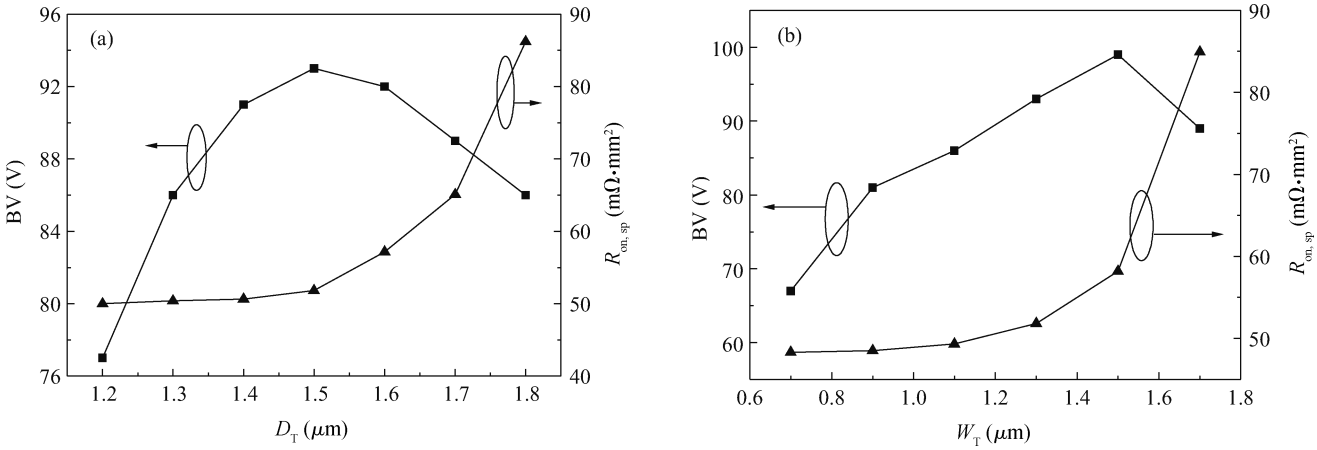

Fig. 5. Influences of D_T and W_T on the BV and $R_{on, sp}$ for a DG trench MOSFET at a 3 μm half pitch. (a) D_T ($W_T = 1.3$ μm); (b) W_T ($D_T = 1.5$ μm).

(BOX) is enhanced for DG and SG trench MOSFETs. Figures 3(a) and 3(b) demonstrate that both the lateral BV and the vertical BV can be improved.

Figure 4 shows the 2-D current lines of the four devices. Owing to the dual conduction channels in the on-state and the highest optimized N_d, the number of current lines in Fig. 4(a) is the highest, which indicates that $R_{on, sp}$ is the lowest. In Fig. 4(d), the current path is very long and there is only one conduction channel, so $R_{on, sp}$ is the highest.

Figure 5 shows the influence of the trench depth (D_T) and trench width (W_T) on the BV and $R_{on, sp}$. In Fig. 5(a), the BV rises from 78 to 93 V as D_T increases from 1.2 to 1.5 μm because the equivalent length of the drift region (L_d) increases with the increase of D_T. The BV starts to decrease at $D_T >$ 1.5 μm because the narrow Si space below the oxide trench leads to a high electric field and premature breakdown at the right corner of the trench. $R_{on, sp}$ of 51.8 mΩ·mm^2 and a BV of 93 V are obtained by simulation with the optimized D_T of

1.5 μm. In Fig. 5(b), the BV rises from 42 to 99 V as W_T increases from 0.5 to 1.5 μm because the equivalent length of the drift region (L_d) becomes longer. In addition, the BV starts to decrease at $W_T > 1.5$ μm because the Si region below the drain is too narrow to sustain high voltage. From Figs. 5(a) and 5(b), it can be observed that the $R_{on,sp}$ increases with the increase of D_T and W_T, which leads to the narrowed current path.

The values of half-cell pitch, $L_{d,eq}$, optimized N_d, BV, $R_{on,sp}$ and FOM (FOM $= BV^2/ R_{on,sp}$) for a DG trench MOSFET, an SG trench MOSFET, an SG MOSFET (A-type and B-type) are given in Table 1. Firstly, when the three types of devices have the same equivalent $L_{d,eq}$, the BV is the same, and the DG trench MOSFET has the smallest $R_{on,sp}$ owing to the effect of the oxide trench and the double gates. Secondly, an oxide trench in the DG and SG Trench MOSFETs contributes to a higher BV and higher optimized N_d than those of the SG MOSFET at the same half-cell pitches (A-type). Thirdly, comparing with the other devices, the $R_{on,sp}$ of DG trench MOSFET is the smallest owing to the dual conduction channels and the high optimized N_d. Fourthly, a longer drift region results in a higher BV, a lower optimized N_d, a longer current path and a higher $R_{on,sp}$ for the B-type SG MOSFET than those of the A-type SG MOSFET.

The key fabrication processes of the DG trench MOSFET are as follows: (1) select an SOI wafer and thin to the specified thickness; (2) etch silicon, thermal oxidation and depositing oxide to form the oxide trench; (3) etch oxide in the oxide trench; (4) etch silicon to the buried oxide layer, thermal oxidation and deposit poly-silicon to form the double gates; (5) implant and diffuse to form a p well, n^+ source and drain regions; (6) make contact holes and deposit metal to form the source, drain and gate electrodes. In steps (3) and (4), polysilicon is doped by using *in-situ* doping technology.

4. Conclusion

The SOI double-gates trench-type MOSFET is proposed and investigated by simulation. The double gates decrease the specific on-resistance by forming dual conduction channels. The oxide trench not only folds the drift region, but also modulates the electric field, thereby reducing cell pitch and increasing the BV. The proposed device features an enhanced BV and a reduced $R_{on,sp}$. BV $= 93$ V and $R_{on,sp} = 51.8$ mΩ·mm^2 are obtained at 3 μm half-cell pitch. Compared with an SG trench MOSFET, an SG MOSFET (A-type) and an SG MOSFET (B-type), the specific on-resistance of the DG trench MOSFET is decreased by 33.8%, 17.9% and 63.3%, respectively.

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