A wideband RF amplifier for satellite tuners

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Abstract: This paper presents the design and measured performance of a wideband amplifier for a direct conversion satellite tuner. It is composed of a wideband low noise amplifier (LNA) and a two-stage RF variable gain amplifier (VGA) with linear gain in dB and temperature compensation schemes. To meet the system linearity requirement, an improved distortion compensation technique and a bypass mode are applied on the LNA to deal with the large input signal. Wideband matching is achieved by resistive feedback and an off-chip LC-ladder matching network. A large gain control range (over 80 dB) is achieved by the VGA with process voltage and temperature compensation and dB linearization. In total, the amplifier consumes up to 26 mA current from a 3.3 V power supply. It is fabricated in a 0.35-μm SiGe BiCMOS technology and occupies a silicon area of 0.25 mm^2.

Key words: SiGe BiCMOS; linearization; wideband matching; process voltage and temperature compensation
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1. Introduction

With the ever-increasing demands of the digital multimedia applications market in recent years, more and more interest is focused on digital TV, which may eventually take the place of its analog counterpart in the future. A satellite network, along with cable networks and terrestrial networks, is considered as one of the most effective ways to deliver digital TV programs. The available digital satellite television standards include European standard DVB-S/S2, North American ATSC and Japanese ISDB-S. Recently, China developed its own satellite standard, ABS-S. Among all these standards, DVB-S/S2 is the most popular in the world. In the DVB-S/S2 downlink, the low noise block (LNB) down-converter translates RF satellite signals from the C, Ku or Ka band down to the L-band (950–2150 MHz). This signal is then sent to a satellite TV set-top box through a coaxial cable, where a tuner performs the final down conversion to baseband signal.

In contrast to the narrow-band wireless receiver, a satellite tuner must receive RF carriers spanning from 950 to 2150 MHz. This presents new challenges for LNA input matching. Also, in the bandwidth over 1 GHz, multiple channels at similar power levels require LNAs with high linearity in order to avoid in-band inter-modulation. In addition, there are many blockers, such as GSM, PCS, and DECT, existing in the signal band. This brings more stringent linearity requirements. Due to the gain variation of up-to-date LNBs, cable losses and weather conditions, a large dynamic range is required, which is realized by an RF VGA with sufficient controllable gain.

Considering the above requirements, the amplifier for a satellite tuner should achieve features of wideband input matching ($S_{11} < -10$ dB), large gain control range (> 80 dB) and high linearity (tolerance with strong interference). Of course, low NF (< 5 dB) is also required as it is the first stage of the receiver.

2. Overview of the amplifier

The amplifier, as shown in Fig. 1, consists of a wideband LNA and a two-stage VGA followed by a buffer. It supports a power-down mode through software configuration. For multi-tuner usage, such as watch and record or the picture-in-picture function, the LNA has a loop through output. It has separate control bits and can operate with the remainder of the device in power-down mode.

There are many possible solutions for wideband LNAs, such as distributed amplifiers and inductively degenerated LNAs with an LC lumped matching network. However, when considering power consumption and chip area, resistive feedback amplifiers are more suitable due to their good wideband matching characteristics and compact physical realization.

The variable gain amplifier has two stages to meet the requirement of a large dynamic range. A current steering type VGA is chosen for its excellent linear gain in dB characteristic over a wide gain control range.

In order to be compatible with most demodulators, the VGA gain is designed such that it is inversely proportional to the gain control voltage. The gain control voltage is buffered by a rail-to-rail operation amplifier first, and then it is converted

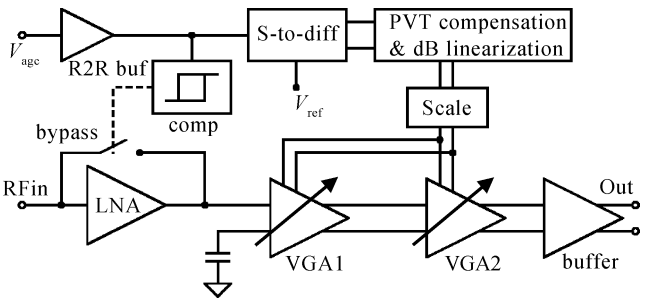

Fig. 1. Book diagram of the wideband amplifier

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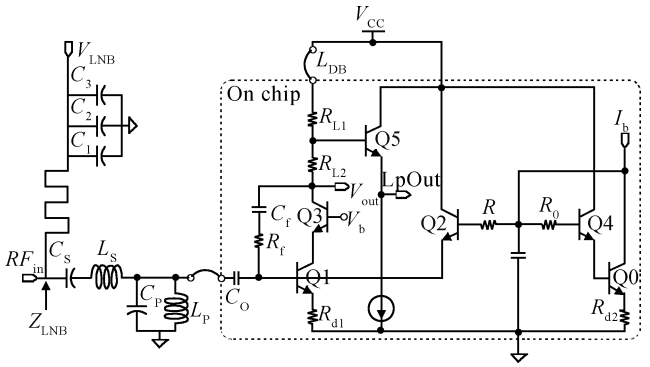

Fig. 2. Simplified schematic of a wideband LNA.

to a differential voltage and processed by a PVT compensation circuit and a dB linearization circuit to achieve simple and accurate RSSI estimation. The differential control voltage is finally scaled to fit each stage of the VGA.

3. Circuit description

3.1. Wideband LNA

A simplified schematic of the proposed LNA is depicted in Fig. 2. A cascode topology is utilized to improve frequency response and reverse isolation. Emitter follower Q5 is used as a buffer for loop through output and measurement purposes. The transistor pairs Q1–Q4 and the resistors R_0, R, R_{d1} and R_{d2} compose a stacked current mirror to make the bias current of Q1 stable. It is noted that the noise figure improves quadratically with the transistor unity gain frequency f_T[1]. Thus transistor Q1 should be biased to its peak f_T. In fact, the transistor is biased at 80% f_T because it is not recommended to operate the transistor at the peak current density, which can markedly degrade performance due to process variations. The amplifier uses resistive load and shunt feedback to provide broadband operation. Capacitor C_f is added to allow for independent biasing of the base and collector. It is large enough to be a short circuit over the frequency of interest[2]. The bond wire inductor L_{DB} is used to boost the gain at high frequencies and equalize the power gain of the LNA to a constant value. It extends the bandwidth without bulky on-chip inductors.

To enhance the linearity of the LNA, an improved distortion compensation technique is applied. As the equivalent base–emitter DC resistance of Q2 decreases as the input RF power increases, the collector current of the transistor Q1 increases as the RF signal increases, as shown in Fig. 3(a). It compensates the gain compression and linearity is improved[3]. The simulation results in Fig. 3 plot the current compensation and power gain versus bias resistors R. The simulation shows that small R will result in over compensation, which makes the power gain peak at large input. Thus a moderate R of 1 kΩ is chosen in the design. To handle the very large input signal and release the linearity requirement of the following stages, bypass mode is activated when the amplifier gain control signal indicates that large attenuation is required. A hysteretic comparator keeps the LNA stable when it switches between these two modes. With these methods, a simulated 1 dB compression point of the LNA loop through is improved by nearly 6 dBm.

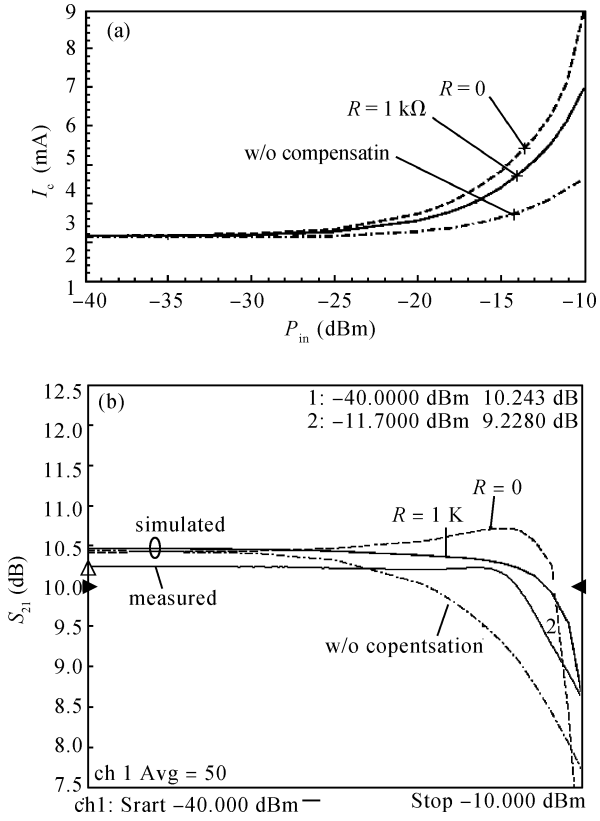

Fig. 3. Measured and simulated LNA distortion compensation. (a) LNA bias current versus RF input. (b) LNA loop output power gain versus RF input.

The measured result is –11.7 dBm at a gain of 10.24 dB, as shown in Fig. 3(b) and +2 dBm at gain of 0 dB.

Due to non-ideal factors, such as the parasitic capacitance of the pad, self and mutual inductance of the wire bond etc., the input impedance of the chip will deviate from the designed value after assembly. A bandpass ladder filter is used as the input matching network[1]. These capacitors and inductors are used off the chip for two reasons: they can compensate the non-ideal factors of the package and they save a lot of chip area thus cutting down costs. In the satellite TV receiver system, the power supply of the LNB is provided by the same cable as the one through which the tuner receives the RF signal. The series capacitor C_s is also used as a DC blocker to keep the internal circuit from breakdown by high LNB voltage (usually DC 13 V or 18 V). Since the LNB power supply line is in parallel with the tuner, the RF signal will be lost if the LNB power supply has low impedance. To minimize the impact, impedance seen from the RF input to LNB power supply should be designed as large as possible. As we all know, $\frac{1}{4}\lambda$ transmission line with another terminal grounded has infinite impedance, so the LNB power supply trace is designed as a transmission line with a grounded capacitor. Considering that the bandwidth is over 1 GHz, three capacitors are used to form three caves, as shown in Fig. 7(b). The nearest capacitor, C_1, intends to ground at the highest frequency while leaving the low frequency signal untouched. Unfortunately, the high frequency and low frequency are not well separated, C_1 will affect the low frequency signal. Thus careful simulation and adjustment is needed.

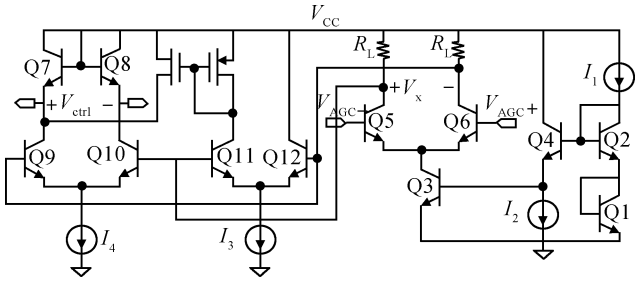

Fig. 4. Simplified schematic of a PVT compensation and dB linearization circuit.

3.2. RF VGA

The gain of the current steering type VGA can be expressed by Eq. (1), where g_m is the transconductance of the differential pair and V_{bc} is the control voltage shown in Fig. 5.

$$G = g_m R\left[1 + \exp\left(-\frac{V_{bc}}{V_T}\right)\right]^{-1}. \quad (1)$$

Equation (1) shows that the gain of the VGA is highly temperature dependent and the characteristic is fairly linear-in-dB at high attenuations, but poor at high gains. When the maximum gain is expected, a compensation and linearization circuit is required. Since $g_m = I_c/V_T$ in bipolar transistors, a PTAT current source is used to obtain a temperature independent g_m. In order to get linear gain in a dB characteristic, the control voltage should be compensated.

The gain control voltage is first buffered by a rail-to-rail operation amplifier (Op-Amp). The Op-Amp has a constant g_m input stage formed by an electronic Zener diode and a class-AB output stage.

Figure 4 illustrates the PVT compensation and dB linearization circuit, where I_1 is a PTAT type current and I_2 is a constant current. Neglecting the base current of Q3, the voltage V_x can be written as Eq. (2), where K is a constant independent of temperature. V_x is in proportion to the absolute temperature, which cancels the factor V_T in the denominator of Eq. (1).

$$V_X \approx \alpha_F R_L \frac{I_1^2 I_{s3} I_{s4}}{I_2 I_{s1} I_{s2}} \frac{V_{AGC}}{2V_T} = K V_T V_{AGC}. \quad (2)$$

The function of the rest circuit is dB linearization. Assuming that transistors Q9–Q12 have the same size and Q7, Q8 have the same size, the output voltage V_{ctrl} can be written as Eq. (3).

$$V_{ctrl} = V_T \ln \frac{1}{\exp(K V_{AGC}) - 1}. \quad (3)$$

3.3. Control voltage compensation

If this voltage V_{ctrl} is applied as VGA control voltage V_{bc}, from Eqs. (1) and (3) we can get

$$G(\text{dB}) = -8.69 K V_{AGC} + 20 \lg(g_m R). \quad (4)$$

In this manner, linear gain in the dB characteristic and temperature stabilization of the current steering VGA gain is achieved[4].

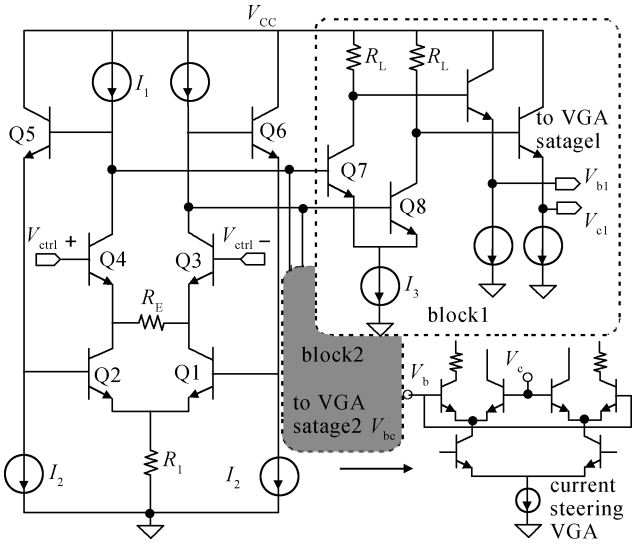

Fig. 5. Simplified schematic of the scaling circuit.

In practice, the VGA gain control range of each stage needs to be carefully designed to trade off between the noise figure and linearity. A large gain of the first stage is desired in order to reduce system NF when the input signal is weak. A large attenuation is also desired to enhance system linearity when the input signal is huge. Usually the first stage requires a large gain control range. Thus a scaling circuit is used, as shown in Fig. 5. The voltage V_{ctrl} is converted into a differential current at the collectors of Q1 and Q2, which makes a pre-distorted differential voltage appear across the bases of Q1 and Q2. It is shifted to a higher common-mode level by Q5 and Q6 to drive the differential pair Q7 and Q8, and then provided as a control voltage to the VGA core. If I_1 and I_3 are the same type of current source and transistors Q1–Q8 are symmetrically sized (i.e., $AE_1 = AE_2$, …, $AE_7 = AE_8$), the voltage V_{ctrl} can be linearly scaled independent of the temperature[5].

$$V_{bc} = \frac{R_L}{R_E}\frac{I_3}{I_1} V_{ctrl}. \quad (5)$$

By selecting R_L or I_3 of each block respectively, a different gain control range can be realized in the two stages. As we notice, if the coefficient of V_{ctrl} in Eq. (5) is not equal to one, a perfectly linear dB characteristic may not be achieved. However, if the VGA gain control range is large enough, a slight sacrifice in the linear characteristic is well worth the improvement of some other system performances such as the noise figure.

4. Measurement results

The wideband amplifier has been fabricated in an IBM 0.35-μm SiGe BiCMOS process. It features four metal layers, a 43 GHz f_T high performance NPN transistor and dual metal–insulator–metal (MIM) capacitors (4.1 fF/μm^2). A die photograph is shown in Fig. 6. It occupies a total die area of 0.25 mm^2 and consumes 26 mA current from a 3.3 V power supply. The amplifier is tested on a four-layer FR4 printed circuit board (PCB). Table 1 summarizes the wideband amplifier performance.

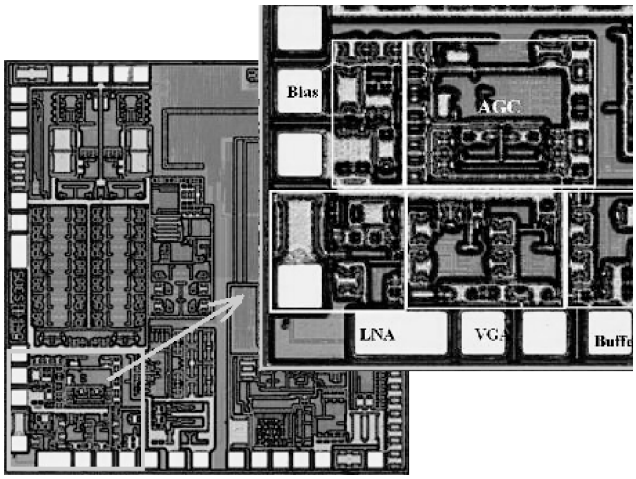

Fig. 6. Die photograph of the wideband amplifier.

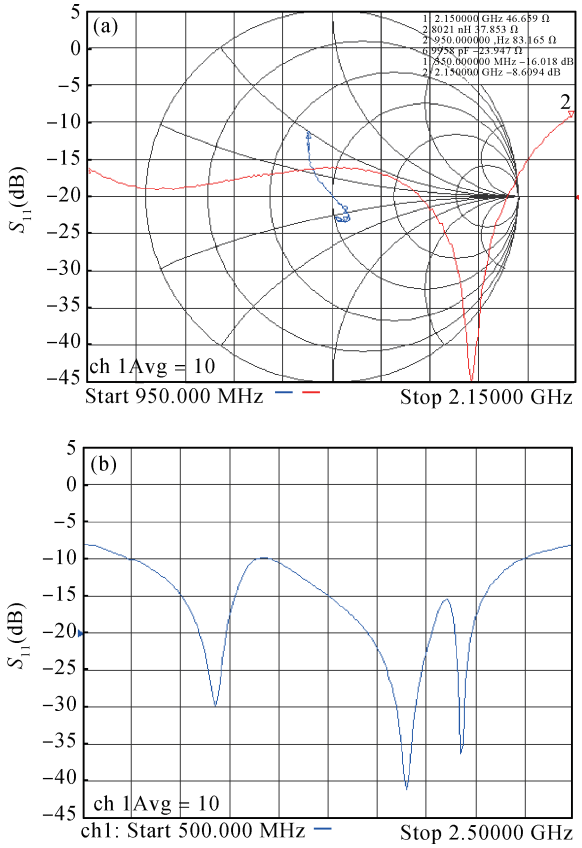

Fig. 7. Measured wideband LNA input matching. (a) Without the LNB transmission line. (b) With the LNB transmission line.

Figure 7 shows the measured S_{11} of the amplifier. Firstly, a PCB without an LNB transmission line is used for wideband matching. By selecting proper L_S, C_S, L_P and C_P, a good matching (S_{11} < –10 dB) can be achieved in the frequency band from 950 to 2100 MHz. Then these inductor and capacitor values are used for a PCB with an LNB transmission line. By carefully choosing the locations and values of capacitors C_1, C_2 and C_3, three caves can be achieved in the frequency band, as shown in Fig. 7(b).

The LNA gain and noise figure are tested from the loop through port with an Agilent noise figure analyzer. As shown in Fig. 8, the measured gain has a peak of 11.5 dB at 1.5 GHz and rolls off by 2 dB at 950 MHz and 2150 MHz. As expected, the noise figure increases with the frequency and reaches a maximum value of 4.5 dB at 2150 MHz. In normal operation mode, the LNA gain is almost twice as much as the loop output gain, so the noise figure of the LNA is expected to be less than 4.5 dB, which is low enough for a satellite tuner.

Table 1. Summary of wideband amplifier performance.

Parameter	Condition	Measured value
S_{11}	With LNB	< -10 dB
Max gain		53.2 dB
Gain range		> 85 dB
NF	At max gain	$\leqslant 5$ dB
IIP3	At low gain	6 dBm
Loop gain	LNA on	9 dB
Loop NF	LNA on	$\leqslant 4.5$ dB
Loop 1 dB CP	LNA on	−11.7 dB

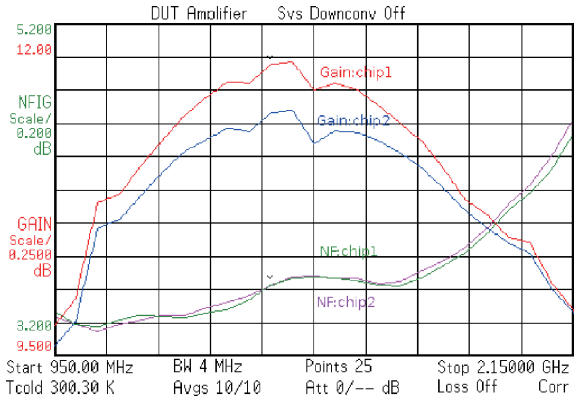

Fig. 8. Measured noise figure and power gain of LNA loop out versus frequency.

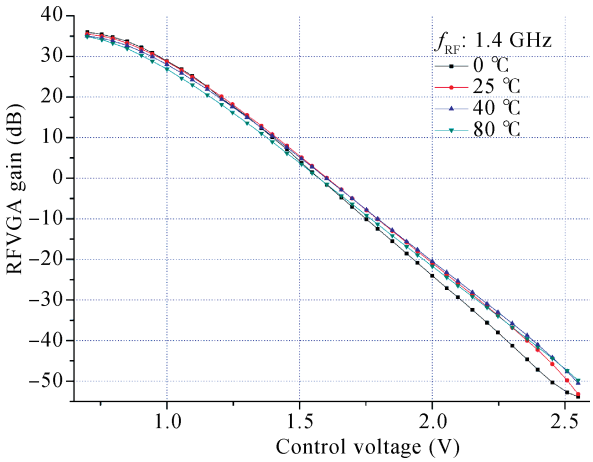

Fig. 9. Measured VGA gain versus control voltage over temperature.

Figure 9 plots the VGA voltage gain versus gain control voltage over temperature. The frequency of the RF input is 1.4 GHz. Four groups of data are measured at temperatures of 0, 25, 40 and 80 ℃. It shows a high dynamic range over 80 dB with a fairly well linear gain-control characteristic except for the extremely low gain condition. This is because as the gain

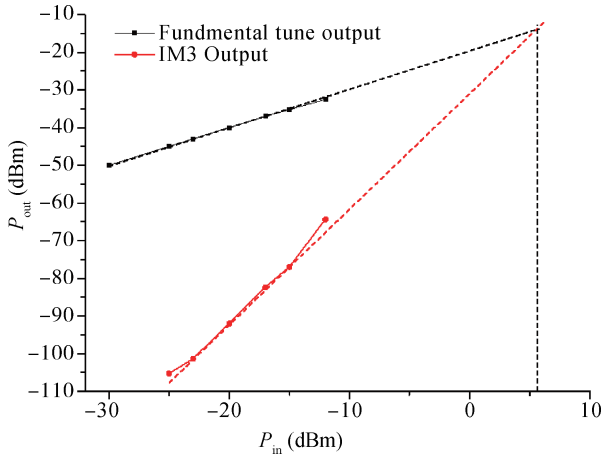

Fig. 10. Measured two tune test of the wideband amplifier at low gain.

control voltage increases, the collector current of transistor Q8 in Fig. 4 should decrease, such that the V_c in Fig. 5 increases and then the VGA gain decreases. However, in fact, Q8 drives the transistor Q3 in Fig. 5, thus the collector current has an inferior limit—the base current of Q3. The gain variation over the entire temperature range is less than 4 dB. This includes contributions from other parts of the chip, such as the LNA and the buffer.

The linearity of the amplifier is measured by a two-tune test. The RF input power is swept from –30 to –12 dBm and the amplifier acts as an attenuator. Two tunes are located at 1499 MHz and 1501 MHz. Figure 10 shows that the input third order intercept point is about 6 dBm.

5. Conclusion

A wideband amplifier for a satellite tuner has been realized in a 0.35-μm SiGe BiCMOS technology. It consists of a wideband LNA, a two-stage VGA with a buffer. The LNA uses resistive shunt feedback to match over the entire band. The LC ladder network helps the input matching despite the package non-ideal factors. The distortion compensation technique and bypass mode improve the linearity effectively. With the PVT compensation and linearization, the current steering type VGA shows a good linear gain control characteristic and no more than 4 dB gain variation over temperatures from 0 to 80 ℃. In total, the wideband amplifier consumes up to 26 mA current from a 3.3-V power supply and less than 1 mA in power-down mode.

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