A cryogenic SAR ADC for infrared readout circuits

Zhao Hongliang(赵宏亮)[1, 2, †], Zhao Yiqiang(赵毅强)[1], and Zhang Zhisheng(张之圣)[1]

[1]School of Electronic Information Engineering, Tianjin University, Tianjin 30072, China
[2]College of Physics, Liaoning University, Shenyang 110036, China

Abstract: A cryogenic successive approximation register (SAR) analog to digital converter (ADC) is presented. It has been designed to operate in cryogenic infrared readout systems as they are cooled from room temperature to their final cryogenic operation temperature. In order to preserve the circuit's performance over this wide temperature range, a temperature-compensated time-based comparator architecture is used in the ADC, which provides a steady performance with ultra low power for extreme temperature (from room temperature down to 77 K) operation. The converter implemented in a standard 0.35 μm CMOS process exhibits 0.64 LSB maximum differential nonlinearity (DNL) and 0.59 LSB maximum integral nonlinearity (INL). It achieves 9.3 bit effective number of bits (ENOB) with 200 kS/s sampling rate at 77 K, dissipating 0.23 mW under 3.3 V supply voltage and occupies 0.8×0.3 mm^2.

Key words: cryogenic ADC; low power; successive approximation register; temperature-compensated time-based comparator

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1. Introduction

With the development of space exploration for the mid- and far-infrared wavelength region, the systems require the cooling of the sensing elements below 77 K[1, 2]. Therefore, ultra-low-temperature front-end circuits[3−5] are required to be close to the sensor arrays and cool down to the same temperature level. The output signals of the front circuit, transported to room temperature analog to digital converter (ADC) through long shielded cables, will suffer from electromagnetic interference and noise coupling problems. The signal integrity of the system can be improved by integrating ADC in the cryogenic system[6−8].

Some cryogenic ADCs developed in standard CMOS technologies have been reported in Refs. [6–8]. The ADC reported in Ref. [6] has an 8 bit successive approximation architecture, however it only has a 3 kS/s sampling rate. A 12 bit cryogenic successive approximation register (SAR) ADC is presented in Ref. [7], whereas the signal-to-noise and distortion ratio (SNDR) attenuates rapidly at low temperature, and the effective number of bits (ENOB) is only 8.3 bit with the sampling rate of 50 kS/s at 77 K. In Ref. [8], a flash ADC provides faster operation over a wider temperature range but consumes higher power for the same resolution level.

The standard CMOS SAR ADC presented in the paper provides a steady performance over a wide temperature range. This improvement is achieved by the employment of a time-based comparator which performs independence of temperature. It operates from room temperature down to 77 K, achieving from 8.7 to 9.3 bit ENOB at a 200 kS/s sampling rate with a current consumption of 70 μA from a 3.3 V supply. The ADC architecture can be applied to extremely low temperature infrared readout applications.

2. Proposed SAR ADC architecture

Figure 1 shows the proposed SAR ADC architecture which is composed of a passive capacitive feedback digital to analog converter (DAC), a digital SAR logic circuit and a high-resolution comparator. At the sampling phase, the switches S1 and S2 are turned on, while a difference of the bias voltage $V_{\rm BIAS}$ and the input signal $V_{\rm IN}$ is sampled on the capacitors array. Next, the switches S1 and S2 are turned off and the conversion phase begins. At the first conversion cycle, the most significant bit (MSB) b9 will be set to 1 and MSB-1 b8 to least significant bit (LSB) b0 will be set to 0. Then the voltage of node $V_{\rm DAC}$ is

$$V_{\rm DAC} = V_{\rm BIAS} + \frac{V_{\rm DD}}{2} - V_{\rm IN}, \tag{1}$$

which will be compared with $V_{\rm BIAS}$ by the comparator. The compared result determines MSB is 1 or 0. Meanwhile, MSB-1 b8 is set to 1 and MSB-2 b7 to least significant bit (LSB) b0 is set to 0. The proposed SAR ADC repeats above mentioned conversion step until the LSB is resolved, then EOB signal is set to 1, which indicates the finish of a conversion phase.

Compared with other ADC architectures[9,10], the proposed ADC is more suitable for wide operation temperature range due to the almost temperature-independent performance of the passive components and the digital circuits. Thus, the design of high-resolution comparator for cryogenic temperatures is the most challenge. The next section will introduce a temperature-compensated time-based comparator architecture in detail.

3. Cryogenic comparator design

The conventional comparator consisting of low-gain preamplifiers and a latch is shown in Fig. 2(a), which provides

† Corresponding author. Email: zhaohl@tju.edu.cn
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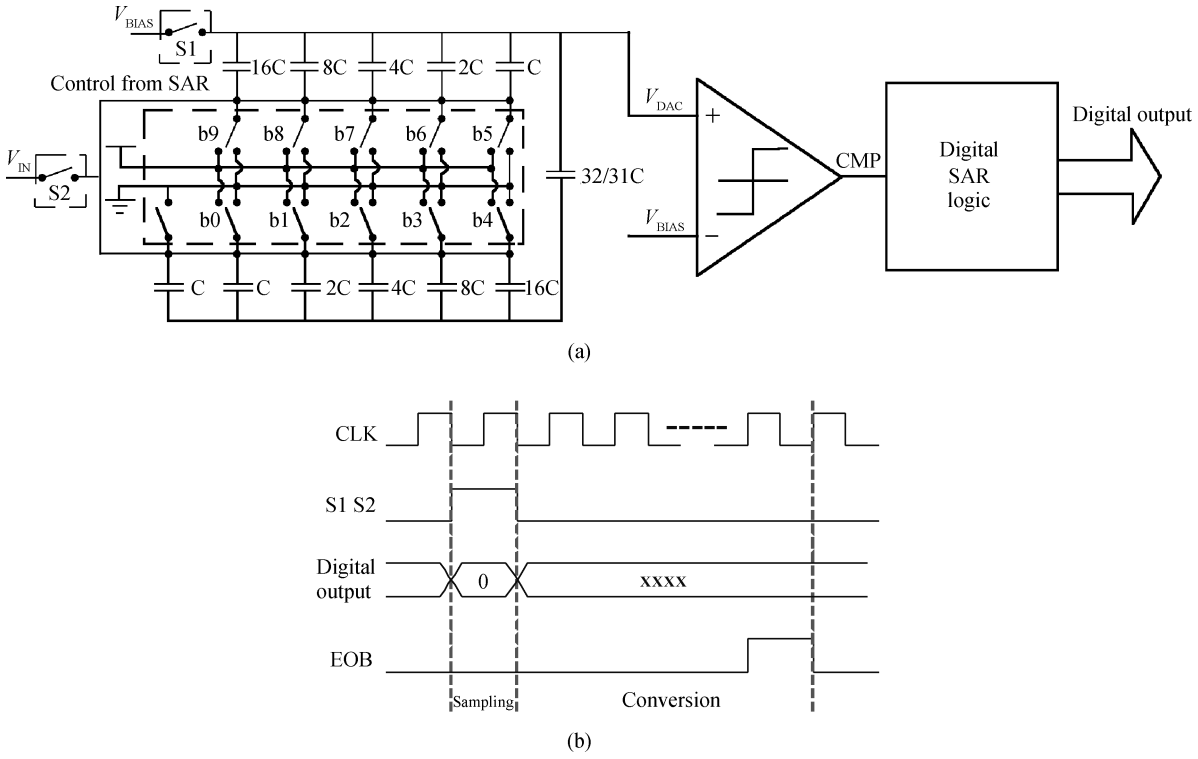

Fig. 1. The proposed ADC architecture and timing diagram.

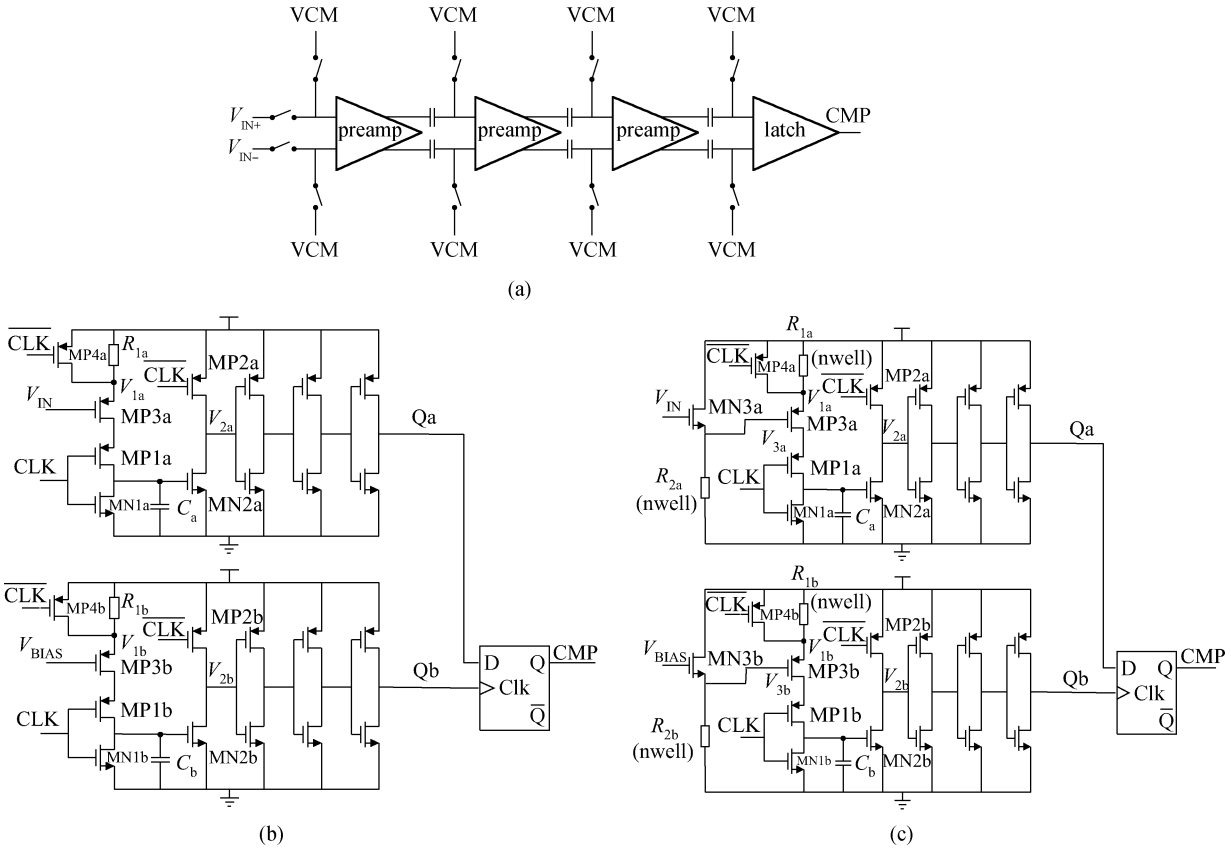

Fig. 2. (a) Conventional comparator. (b) Time-based comparator. (c) Time-based comparator with temperature compensation.

high resolution with offset cancellation technique[11]. However, due to the anomalous dc and transient behavior of MOSFETs at cryogenic temperatures, the transistors in the preamplifiers will be likely to operate in linear region, which result in the attenuation of the comparator performance. Moreover, the offset cancelling in the beginning of the conversion pro-

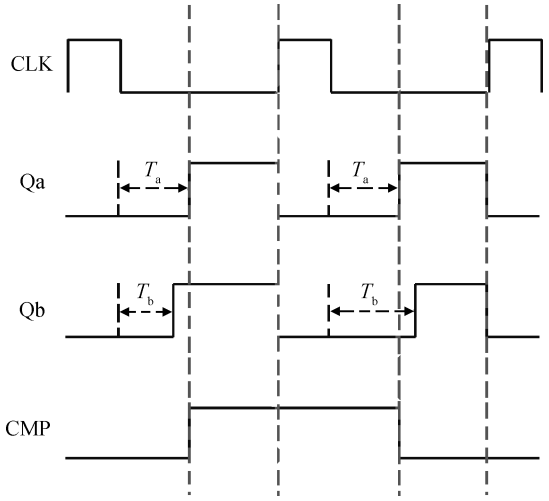

Fig. 3. Timing diagram of the time-based comparator.

cess is not reliable resulting from the hysteresis at cryogenic temperatures[6].

A time-based comparator introduced in the proposed ADC is shown in Fig. 2(b), which is composed of two voltage-to-time converters (VTCs) and a flip-flop. When the signal CLK is high, transistors MN1a and MN1b discharge the same capacitors C_a and C_b to ground, while nodes V_{1a}, V_{1b}, V_{2a} and V_{2b} are set to V_{DD}. When CLK falls, constant currents with I_{1a} and I_{1b} across transistors MP3a and MP3b charge capacitors C_a and C_b at constant rates, respectively, where I_{1a} and I_{1b} are equal to

$$I_{1a} = \frac{V_{DD} - V_{1a}}{R_a}, \tag{2}$$

$$I_{1b} = \frac{V_{DD} - V_{1b}}{R_b}. \tag{3}$$

When the voltages of C_a and C_b reach the threshold voltages of MN2a and MN2b, the node V_{2a} and V_{2b} change from high to low, and the following inverter stages produce two pulses with durations T_a and T_b given as

$$T_a = \frac{C V_{th}}{I_a} = \frac{RC V_{th}}{V_{DD} - V_{1a}}, \tag{4}$$

$$T_b = \frac{C V_{th}}{I_b} = \frac{RC V_{th}}{V_{DD} - V_{1b}}, \tag{5}$$

where $R = R_a = R_b$, $C = C_a = C_b$, and V_{th} is the threshold voltage of MN2a and MN2b. Then the comparison of the voltages V_{IN} and V_{BIAS} change to the comparison of durations T_a and T_b. The difference between T_a and T_b is given as

$$\Delta T = \frac{RC V_{th}(V_{1a} - V_{1b})}{(V_{DD} - V_{1a})(V_{DD} - V_{1b})} \approx \frac{RC V_{th}\Delta V_{in}}{(V_{DD} - V_1)^2}, \tag{6}$$

where $\Delta T = T_a - T_b$, and the power supply voltage V_{DD} is equal to 3.3 V. When V_{IN} is closed to V_{BIAS}, $\Delta V_{in} = V_{IN} - V_{BIAS} \approx V_{1a} - V_{1b}$ and $V_1 \approx V_{1a} \approx V_{1b}$.

The flip–flop is used to generate the comparison results by latching the D input at the positive edge of the clock input. The accuracy of the comparator depends on ΔT, R, C, V_{th} and V_1. The minimum ΔT is the setup time of the flip-flop. In the

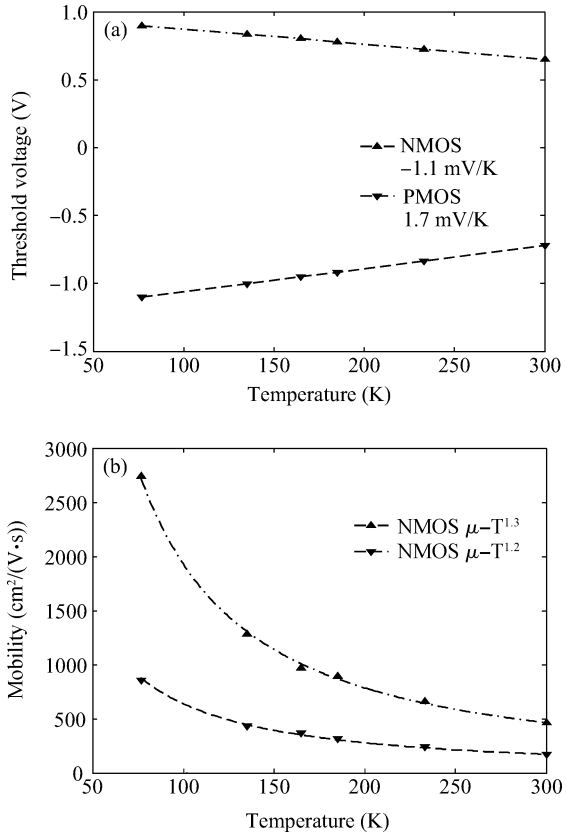

Fig. 4. (a) Variation of threshold voltage with temperature. (b) Variation of mobility with temperature.

used technology, $T_{setup} = 240$ ps, $V_{th} = 0.65$ V, $V_1 \approx 2.4$ V at room temperature. For 10 bit resolution, the RC should exceed 0.1 μs since the minimum resolution of the comparator is 3 mV. Equations (4)–(6) suggest that the accuracy of the comparator is contradictory to the speed of that. Therefore, for the tradeoff between the accuracy and speed, R and C are equal to 1.5 pF and 200 kΩ in the design, respectively. Meanwhile, in order to increase the charge time at a clock cycle, the duty cycle of the CLK signal is 25%. The timing diagram is shown in Fig. 3.

Since the precise bias voltage or current is not required in the time-based comparator, the anomalous dc and transient behavior of the MOS transistors have little effect on the performance of the comparator at cryogenic temperatures. On the contrary, the resolution of the comparator will be improved resulting from the increase in the transistor threshold voltage and carrier mobility, and the decrease in the flip–flop setup time and KT/C noise at low temperatures. However, considering the contradiction between the accuracy and speed, appropriate temperature compensation is required to ensure the sampling rate of the SAR ADC within the whole operation temperature range (from room temperature to liquid nitrogen temperature).

Figure 4 shows the temperature dependence of threshold voltage and carrier mobility for both NMOSFET and PMOSFET, measured on the used 0.35 μm CMOS technology. With the temperature decreasing, the threshold voltage and carrier mobility increase resulting in the rise of voltage V_1 and the fall of current I_1, which will increase the reverse time and reduce the operating clock frequency. The source follower consisted of MN3 and R_2 as shown in Fig. 3(c) is employed to com-

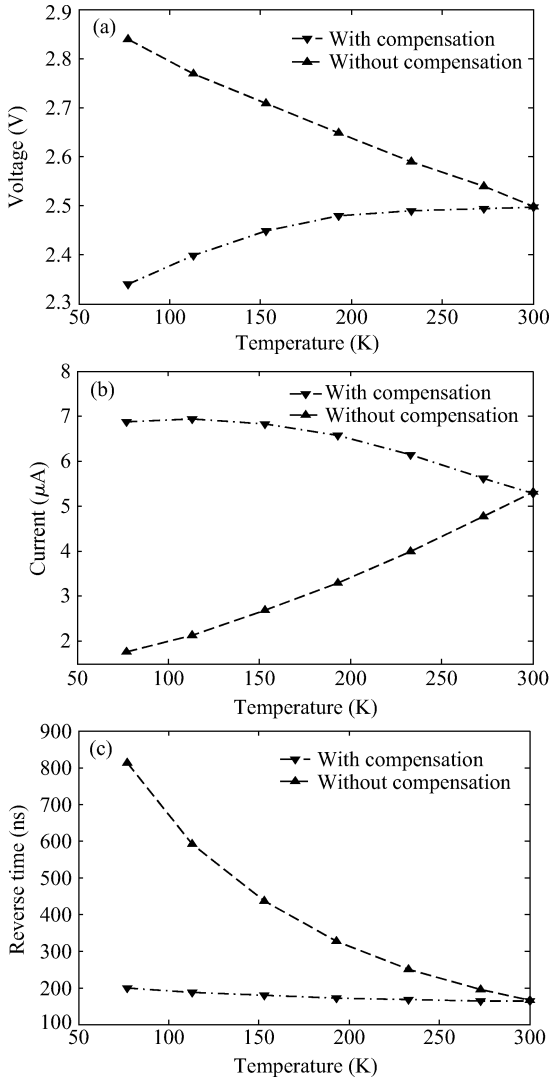

Fig. 5. (a) Voltage V_1 versus temperature. (b) Current I_1 versus temperature. (c) Reverse time T versus temperature.

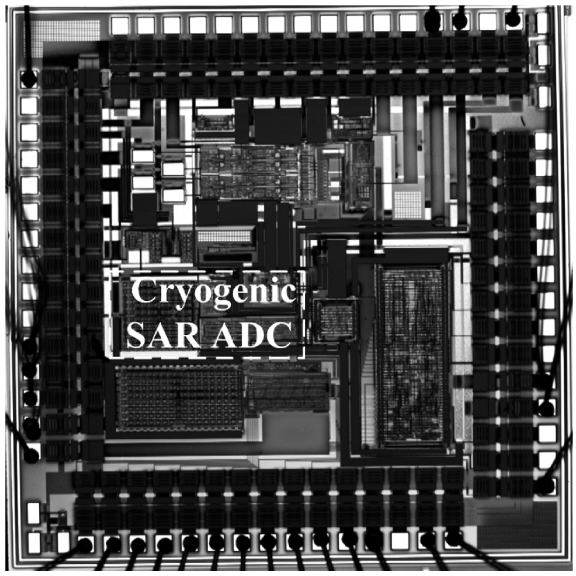

Fig. 6. Chip micrograph.

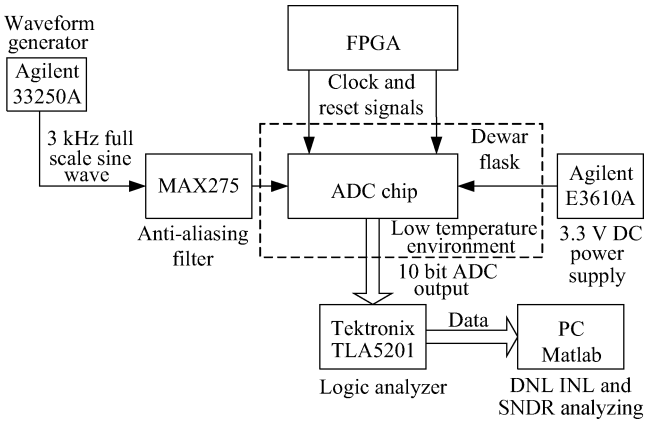

Fig. 7. Test system.

pensate for the characteristic variations of transistor MP3 at low temperature. As the temperature is reduced, the voltage V_1 trends upwards, while the voltage V_3 trends downwards, which results in voltage V_1 tending to a constant. Meanwhile, R_1 and R_2 are implemented by positive temperature coefficient nwell resistors to compensate for the threshold variation of MN1a and MN1b at low temperatures. When the temperature is lowered, the reverse time increases since the increase in the threshold voltage of MN2. Whereas, the nwell resistance is reduced resulting in the increase in charge current at low temperature, which eliminates the effect of threshold voltage variation on the reverse time. The voltage V_1, current I_1 and reverse time T versus temperatures are shown in Figs. 5(a)–5(c) respectively, which declare that the stability of the comparator performance at low temperatures is significantly improved through the temperature compensation.

4. Experimental results

The prototype circuit of a 10 bit cryogenic SAR ADC has been designed using Chartered 0.35 μm CMOS process. As shown in Fig. 6, the chip area of the ADC is 0.8×0.3 mm^2.

The test system is illustrated in Fig. 7. The ADC chip is packaged in a Dewar flask which provides 77 K to room temperature operation environment. A 3 kHz full scale sine wave test signal is generated through Agilent 33250A waveform generator and MAX275 antialiasing filter. The clock and reset signals are generated by FPGA. The Tektronix TLA5201 logic analyzer is used to record the results which will be analyzed by Matlab software. When the ADC operates at room temperature, the differential nonlinearity (DNL) and the integral nonlinearity (INL) are within $-0.89/1.7$ LSB and $-1.1/1.1$ LSB, respectively, as shown in Fig. 8(a), and the measured SNDR is 54.1 dB, as shown in Fig. 8(b). When the ADC operates at 77 K, DNL and INL are within $-0.12/0.64$ LSB and $-0.59/0.37$ LSB respectively, as shown in Fig. 8(c), and the measured SNDR is 57.7 dB at a conversion rate of 200 kS/s, as shown in Fig. 8(d). The measured results show that the performance of the ADC is slightly improved with the temperature decreasing. The ADC dissipates 0.23 mW with 3.3 V supply. The common figure of merit (FOM) is 1.8 pJ/step based on

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot f_{\text{s}}}. \tag{7}$$

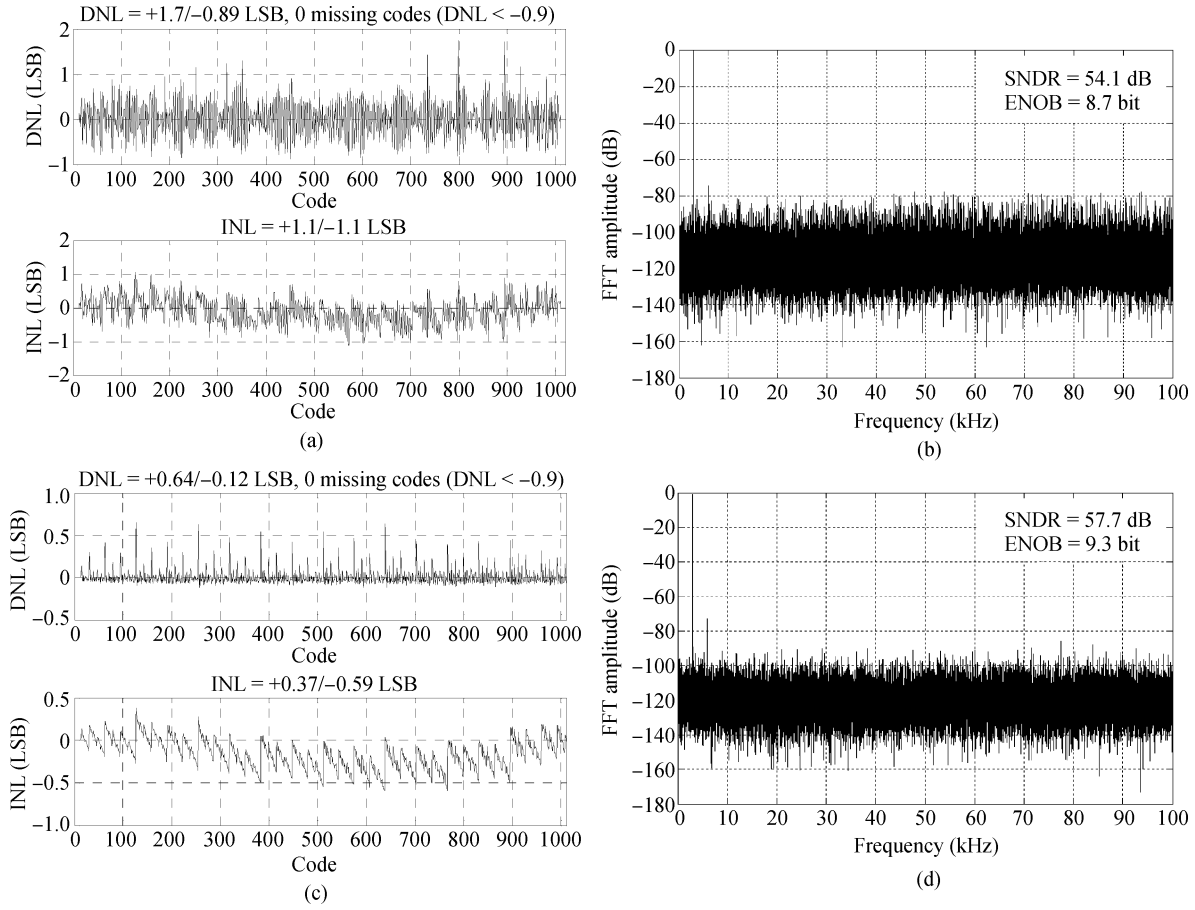

Fig. 8. (a) DNL and INL of the ADC at room temperature. (b) Output spectrum for input frequency of 3 kHz at room temperature. (c) DNL and INL of the ADC at 77 K. (b) Output spectrum for input frequency of 3 kHz at 77 K.

5. Conclusion

A novel SAR ADC with temperature-compensated time-based comparator for cooling infrared readout circuit has been designed and manufactured in this paper. The proposed ADC performs simple circuit configuration, low power dissipation and superior FOM, and provides a stable performance over an extremely wide temperature range. Simulation and experimental results indicate a potential superiority of implementing the ADC architecture for applications on ultra low temperature and ultra low power systems.

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