Indium bump array fabrication on small CMOS circuit for flip-chip bonding

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Abstract: We demonstrate a novel method for indium bump fabrication on a small CMOS circuit chip that is to be flip-chip bonded with a GaAs/AlGaAs multiple quantum well spatial light modulator. A chip holder with a via hole is used to coat the photoresist for indium bump lift-off. The 1000 μm-wide photoresist edge bead around the circuit chip can be reduced to less than 500 μm, which ensures the integrity of the indium bump array. 64×64 indium arrays with 20 μm-high, 30 μm-diameter bumps are successfully formed on a 5×6.5 mm^2 CMOS chip.

Key words: flip-chip bonding; indium bump; array; small-size
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1. Introduction

In recent years, flip-chip bonding (FCB) has been widely used because of its high connection density, superior electrical performance, good reliability and reasonable cost[1]. The connections of various semiconductor devices, such as vertical-cavity surface-emitting lasers (VCSELs), quantum well infrared photodetectors (QWIPs) and spatial light modulators (SLMs), with their CMOS driving circuits using FCB technology have been studied intensively[2−5]. A typical FCB process includes under bump metallization (UBM) formation, bump deposition, bonding, underfill injection and wafer thinning[6]. Generally, large bumps are required to reduce the thermal expansion mismatch and ensure good underfill flow[7]. However, to save costs, the CMOS circuit usually comes from a Multi Project Wafer (MPW) project[8], which introduces a problem: the CMOS chip diced from a MPW wafer is usually very small, with very little margin left on the edge. For such a small chip, the patterning of a thick photoresist required for a high indium bump lift-off is very difficult, because in the resist coating process, thick photoresist beads will be left at the edges of the chip. The edge beads may enter the patterning area of the indium bump array and cannot be removed by a regular edge-bead removal process. Non-uniformity of exposure and development between the center and the edge will therefore appear. With normal processing procedures, the thick edge beads will be under-exposed and under-developed. Thus, the indium bumps at these places will be deposited on the photoresist and will be removed by the subsequent lift-off process. Consequently, uniform and complete indium bumps cannot be obtained.

In this paper, a method that employs a chip holder with a via hole to spin the photoresist is proposed. The photoresist edge bead can be transferred from the CMOS chip to the chip holder. Indium arrays with 20 μm-high, 30 μm-diameter bumps are successfully formed on 5×6.5 mm^2 CMOS driving circuits for our GaAs/AlGaAs multiple quantum well spatial light modulators.

2. Chip holder fabrication

The chip holder with a via hole was fabricated in 4 steps: SiO_2 deposition, via hole patterning, SiO_2 wet-etching, and inductively coupled plasma (ICP) deep Si etching, as illustrated in Fig. 1. The thickness of the holder should be identical to the CMOS circuit for a smooth surface. First, 3000 nm SiO_2 was deposited on the holder wafer in a plasma-enhanced chemical vapor deposition (PECVD) system to serve as a hard mask for the subsequent deep Si etching. Then the wafer was cut into pieces (15×15 mm^2). It is not necessary to have any special mask to pattern the via hole. Reversible AZ5214 was used as negative photoresist, and the CMOS chip itself was placed above the holder wafer as a self-adapting mask. The holder was exposed in a Karl-Suss MA6 aligner for 4.5 s and the CMOS chip was subsequently removed. Then the holder was baked at 105 ℃ for 90 s, flood-exposed for 55 s and developed in 2.38% TMAH solution for 90 s to open the via hole window. After that, the holder was etched in HF : $NH_4F = 1 : 5$ solution for 10 min to expose the Si opening at the via hole area. Finally, the holder was etched in an ICP etching system (STS MPX HRM) for about 1 h to obtain the via hole. Figure 2 shows a photograph of our fabricated chip holder and the CMOS circuit.

3. Photoresist coating and indium bump lift-off

The photoresist coating process is shown in Fig. 3. First, the CMOS chip was placed into the via hole of the holder. Then both of them were stuck to a piece of adhesive tape. Viscous photoresist (AZ4620) was dropped to the surface of the CMOS chip and filled into the gap between the chip and the holder. The adhesive tape was spun at 3k rpm for 30 s in a KW-4A spin coater. With the holder, the photoresist edge bead was transferred from the edge of the CMOS chip to the edge of the chip holder. The CMOS chip and the holder were then removed from the tape and baked at 100 ℃ for 60 s. Another layer of

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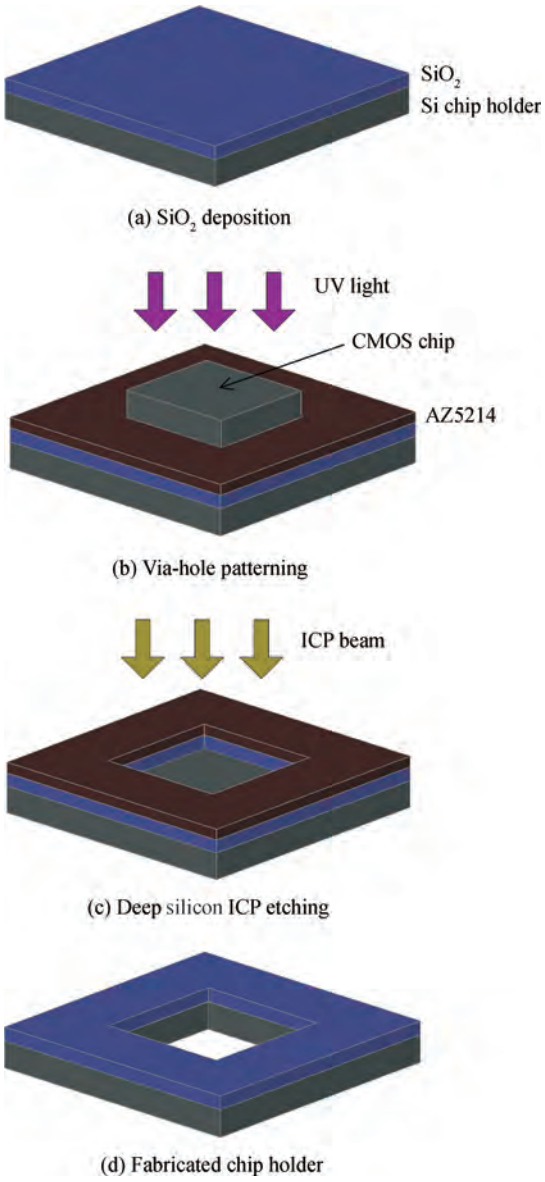

Fig. 1. Schematic of chip holder fabrication process.

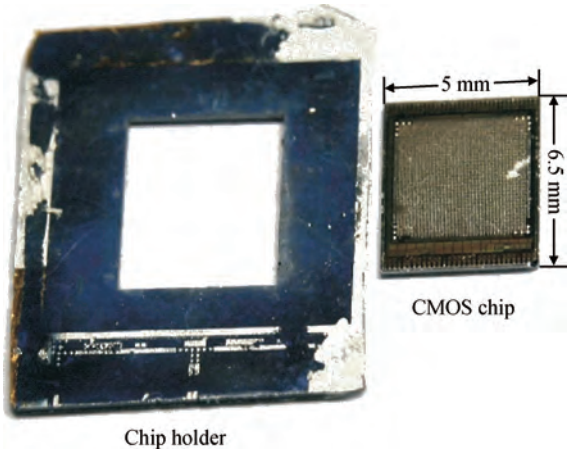

Fig. 2. Photograph of fabricated chip holder and CMOS circuit.

AZ4620 was coated using the same method and baked at 100 ℃ for 180 s. After the photoresist coating, the indium bump array was patterned. The exposure and development times were 40 s and 90 s, respectively. 50 nm/300 nm Ti/Au was evaporated in an Ulvac Ei-5z e-beam evaporator, followed by a 10 μm thick indium film deposition in a home-made thermal evaporation system. Then the photoresist was removed in hot NMP for 20 min in an ultrasonic cleaning bath. Finally, the chip was reflowed at 180 ℃ for 60 s in a formic acid atmosphere.

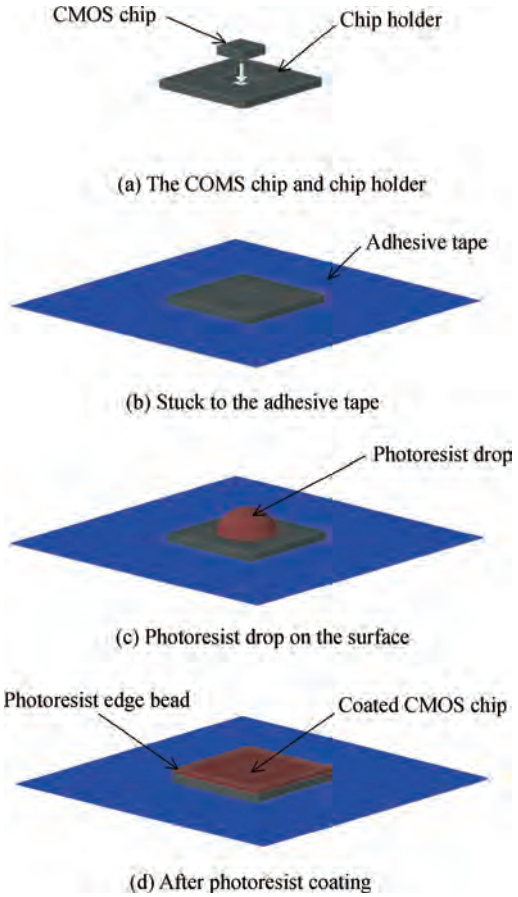

Fig. 3. Schematic of photoresist coating process using a chip holder.

4. Experimental results

Figure 4 shows the appearance of the coated photoresist and indium bump array fabricated without/with the chip holder. Figure 5 plots the width and thickness of the edge bead as measured by a Veeco Dektak 150 surface profiler. The solid and dashed lines correspond to the marked points in Figs. 4(a) and 4(b), respectively. It can be clearly seen that by using the chip holder, the edge bead of the double-layer AZ4620 photoresist decreases from 1000 to about 400 μm, while the height of the edge bead decreases from 20 to 15 μm. After the lift-off and reflow process, a uniform and complete indium array was obtained, as shown in Figs. 4(c) and 4(d).

Figure 6 shows an SEM picture of our indium bumps deposited on the 5 × 6.5 mm^2 CMOS circuit. The indium bump array size is 64 × 64, while the bump dimension is 30 μm in diameter and 20 μm in height.

5. Conclusion

A novel approach for fabricating indium bump arrays on small CMOS circuits is presented. A chip holder with a via hole

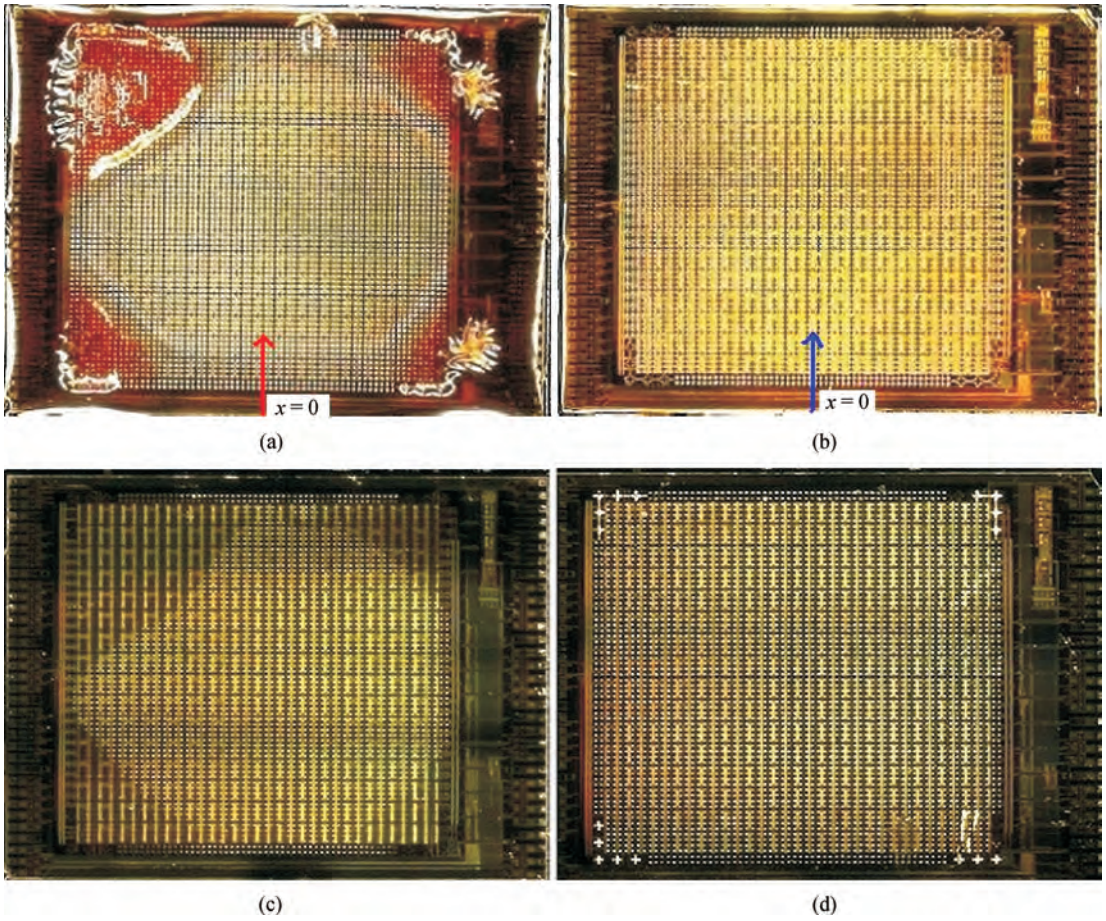

Fig. 4. Photoresist deposition profile (a) without and (b) with the chip holder, and indium bumps after reflow (c) without and (d) with the chip holder.

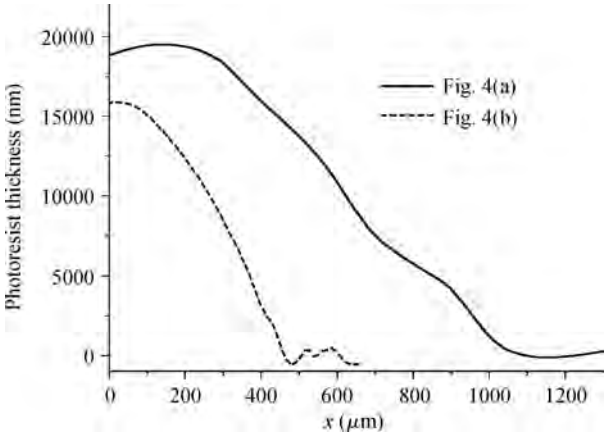

Fig. 5. Photoresist edge bead height profile without/with the chip holder.

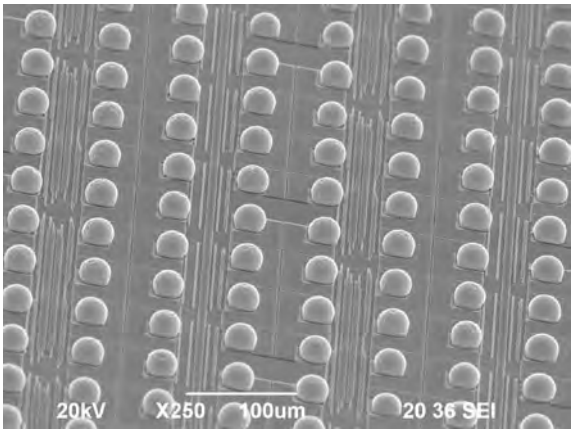

Fig. 6. SEM picture of indium bumps formed on the 5 × 6.5 mm^2 CMOS circuit.

is used to coat thick photoresist for the lift off process for indium bumping. The fabrication procedure of the chip holder is described, and the photoresist coating and indium array lift-off process are discussed. Coated with the chip holder, the width of edge bead of the double-layer AZ4620 photoresist is decreased from 1000 to about 400 μm, and the thickness is decreased from 20 to 15 μm. 20 μm-high 30 μm-diameter indium bumps are successfully formed on our 5 × 6.5 mm^2 CMOS circuit chips. This work forms the foundation for the flip-chip bonding of our GaAs/AlGaAs MQW SLM and CMOS circuit in a follow-up development.

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