A transformer-loaded receiver front end for 2.4 GHz WLAN in 0.13 μm CMOS technology

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Abstract: A 2.4 GHz radio frequency receiver front end with an on-chip transformer compliant with IEEE 802.11b/g standards is presented. Based on zero-IF receiver architecture, the front end comprises a variable gain common-source low noise amplifier with an on-chip transformer as its load and a high linear quadrature folded Gilbert mixer. As the load of the LNA, the on-chip transformer is optimized for lowest resistive loss and highest power gain. The whole front end draws 21 mA from 1.2 V supply, and the measured results show a double side band noise figure of 3.75 dB, –31 dBm IIP3 with 44 dB conversion gain at maximum gain setting. Implemented in 0.13 μm CMOS technology, it occupies a 0.612 mm^2 die size.

Key words: zero-IF; direct-down-conversion; WLAN; CMOS RF; on-chip transformer
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1. Introduction

In the past decade, the extraordinary growth of the wireless communication market, such as cell phones, wireless local area networks (WLANs), personal digital assistants (PDAs) and other hand-held devices, has led to a great demand for wireless connectivity devices, also generates huge interest in low cost, silicon based, radio frequency integrated circuits (RFICs) using complementary metal–oxide–semiconductor (CMOS) technology.

Due to the continuously shrinking feature size of CMOS technologies, the integration of the analog and digital components for the "system-on-chip" solution is now available. To succeed in the current market and to keep cost down, fully integrated low power wireless transceivers have now become mainstream.

Although monolithic inductors have been found extensive usage in RF CMOS circuits to reduce the number of passive components on board, the balun is traditionally realized off-chip. This increases the system cost and reduces the sensitivity by at least 1 dB for its insertion loss before the LNA.

Although some on-chip spiral transformers used in silicon radio-frequency integrated circuits have been reported to perform impedance matching[1], signal coupling[1, 2], etc, the performance of these circuits is strongly affected by the quality of the transformer itself. Therefore, an optimization procedure is required when designing the transformer to achieve high performance in terms of higher power gain and lower resistive losses.

Meanwhile, as a critical building block in the receiver, the performance of an RF front end determines the sensitivity and linearity of the system. In order to meet the strict 802.11b/g standards, a 2.4 GHz receiver front end with an optimized on-chip transformer implemented with 0.13 μm CMOS technology is presented in this paper.

Based on zero-IF architecture[3], the front end includes a transformer-loaded LNA, a quadrature-folded Gilbert mixer with high linearity and a TIA (transimpedance amplifier) buffer. The on-chip transformer is designed and optimized for lower resistive losses and higher power gain. This design achieves a measured voltage gain of 44 dB, 3.75 dB DSB noise figure and –31 dBm IIP3 at high gain mode. The front end can provide 32 dB gain variation range with 16 dB/step while drawing 21 mA from a 1.2 V supply.

2. Receiver front end architecture

According to the standards of IEEE 802.11b/g, the signal from 2.412 to 2.484 GHz is available, and the required receiver sensitivity is better than −65 dBm for 64QAM at 54 Mb/s. For Sensitivity $= -174$ dBm/Hz $+$ NF $+ 10\lg B + \mathrm{SNR}_{\mathrm{min}}$[3], the noise figure of the receiver must be lower than 10 dB, when B is 20 MHz and $\mathrm{SNR}_{\mathrm{min}}$ is 26.5 dB. In addition, if the receiver sensitivity is better than –70 dBm, the noise figure of receiver front end should be lower than 5 dB and the conversion gain of FE must be higher than 35 dB.

A narrowband zero-IF architecture is used in this work to achieve high level integration and to avoid image signal interference. Although the zero-IF architecture brings a high DC-offset, it can be cancelled after VGA through a DCOC in baseband. The flicker noise corner frequency of the mixer must be lower than 100 kHz for the zero intermediate frequency.

In the RF receiver front end, the noise of the LNA is the biggest contributor to the overall noise of the WLAN system. Thus, the LNA must be designed to have low noise, while keeping high power gain and high linearity. The mixer should have good linearity. The noise figure of the mixer is affected by the amplitude of the LO (local oscillator) signal, so the amplitude of LO signal must be large enough.

A simplified block diagram of the front end for a 2.4 GHz

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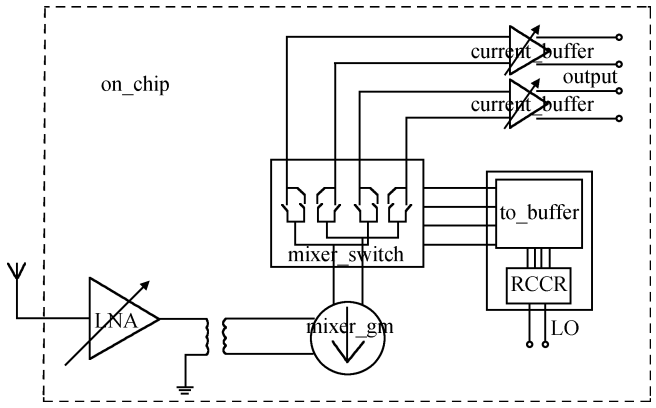


Fig. 1. Block diagram of receiver front end.

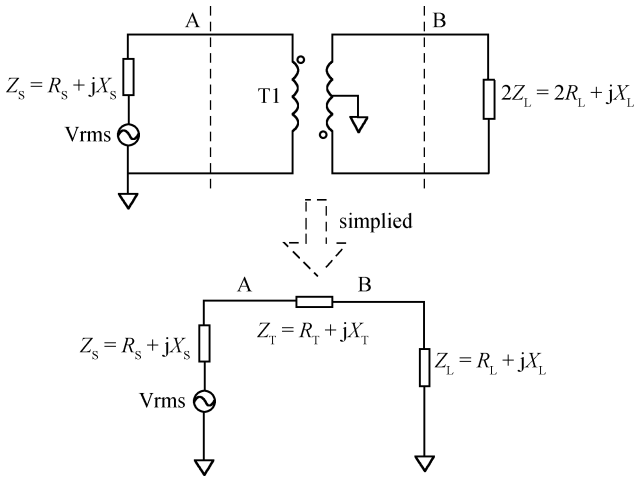


Fig. 2. Resistive loss diagram for balun.

receiver is shown in Fig. 1.

The single-ended input signal is amplified by an inductor-degenerated CSLNA, which is also single-ended and loaded by an optimized transformer. The on-chip transformer converts the 2.4 GHz single-ended signal to a differential one. After that, the differential RF signal is delivered to a transconductance stage with an LC tank and is subsequently down-converted to base-band signal by active double-balance mixer switches. Mixer linear switches carry few DC currents for flick noise reduction in this structure. The down-converted baseband signal current is delivered to a transimpedance amplifier (TIA) buffer which is also a current to voltage converter.

3. Circuit implementation

3.1. Optimization of transformer

An on-chip balun is optimized for area efficiency and a high Q characteristic. When it operates as a tuned load, the high Q characteristic can reduce the power consumption of the circuit.

Various methods for transformer optimization have been reported, such as minimizing the insertion loss[4] and maximizing the available power gain[5]. In this paper, the key is maximizing the power delivered to the load. A diagram is shown in Fig. 2, where Z_T represents the resistive loss of the balun.

Due to the resistive elements, it is impossible to achieve a conjugate match at the primary coil (point A) and the secondary coil (point B) of the transformer at the same time.

When conjugate matching at A, $R_S = R_T + R_{L1}$, the power delivered is simply,

$$P_{A1} = \frac{|V_{rms}|^2}{(R_S + R_T + R_{L1})^2 + (X_S + X_T + X_{L1})^2}(R_{L1} + R_T) = \frac{|V_{rms}|^2}{4R_S}, \tag{1}$$

$$P_{B1} = \frac{|V_{rms}|^2}{(R_S + R_T + R_{L1})^2 + (X_S + X_T + X_{L1})^2} R_{L1} = \frac{|V_{rms}|^2}{4R_S^2}(R_S - R_T), \tag{2}$$

where V_{rms} is the root-mean-square (RMS) voltage across source.

On the other side, conjugate matching at B, $R_{L2} = R_S + R_T$,

$$P_{A2} = \frac{|V_{rms}|^2}{(R_S + R_T + R_{L2})^2 + (X_S + X_T + X_{L2})^2}(R_{L2} + R_T) = \frac{|V_{rms}|^2}{4(R_S + R_T)^2}(R_S + 2R_T), \tag{3}$$

$$P_{B2} = \frac{|V_{rms}|^2}{(R_S + R_T + R_{L2})^2 + (X_S + X_T + X_{L2})^2} R_{L2} = \frac{|V_{rms}|^2}{4(R_S + R_T)}. \tag{4}$$

Comparing the results, it is clear that conjugate matching at the secondary coil of the balun can transfer a higher power to R_L.

$$P_{A1} - P_{A2} = \frac{|V_{rms}|^2}{4R_S}\left(\frac{R_T}{R_S + R_T}\right)^2 > 0,$$
$$P_{B2} - P_{B1} = \frac{|V_{rms}|^2}{4R_S^2}\frac{R_T^2}{R_S + R_T} > 0. \tag{5}$$

3.2. CSLNA

The low noise amplifier is a key block in a typical radio receiver. Generally, the main goal of LNA design is to achieve simultaneous noise and input power matching. Although common source input stages degrade the linearity and increase the sensitivity of the input matching, it is still a widely used topology in narrow-band RF applications.

In the previous work of this author, a common-gate topology was employed to obtain better linearity and easier matching[1]. However, it degrades the sensitivity of whole system for a higher noise figure.

Thus, a cascode CSLNA with inductive source degeneration is used in this paper, as shown in Fig. 3. The inductive

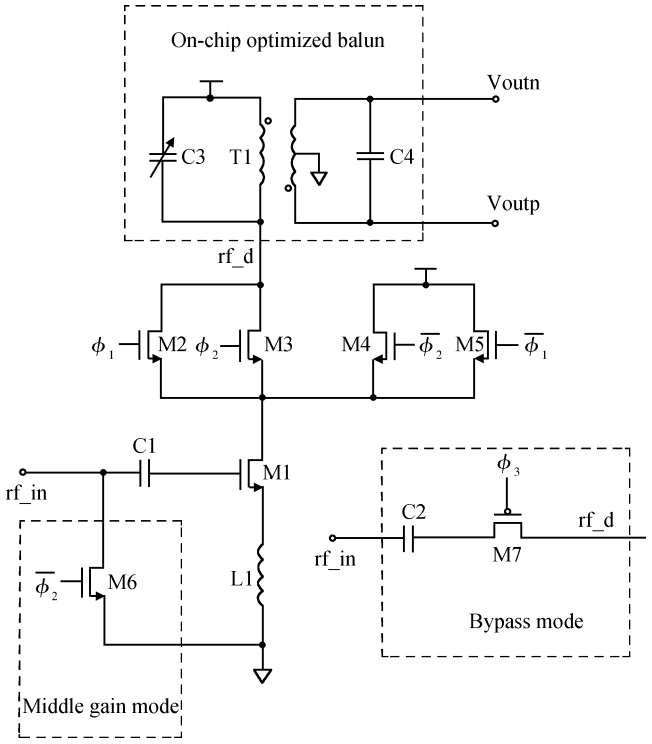


Fig. 3. Transformer-loaded CSLNA.

source degeneration produces a real part $w_T L_1$ in the input impedance, which can be matched to the real part of the source impedance. As a tuned-load of CSLNA, the integrated transformer T1 makes a single-ended-to-differential conversion and reduces current consumption by half, as compared with a differential LNA of the same power gain.

The high Q characteristic of the on-chip balun is required as mentioned above. The reactive impedance $\frac{1}{\mathrm{j}wC_3}$ is shunt-connected to the primary coil to maximize the available output power for conjugate matching at secondary coil[5]; meanwhile, the capacitor C_4 tunes the tank resonance at 2.45 GHz.

The cascode transistors M2 and M3 isolate the input and output matching, and the gain can be changed by current steering with different sizes of cascode transistors. However, it cannot satisfy the need of higher linearity at middle-gain and low-gain mode just by the steering current. A shunt transistor M6 and a bypass switch M7 are used to obtain higher linearity for middle-gain and low-gain mode respectively, which bring about high noise at the same time.

3.3. Folded Gilbert mixer

The mixer is the last stage of the RF front end followed by filter. The filter block makes the linearity of mixer one of the bottlenecks of the whole receiver chain. As an RF block, a mixer should be also designed with a low noise figure and a moderate conversion gain to reduce the noise contribution of the subsequent IF blocks.

Different topologies are used for implementing mixers: current commutated mixer, sub-sampling mixer, potentiometric mixer, passive mixer, etc.[2, 6, 7]. Figure 4 illustrates a conventional Gilbert mixer, which is also a double-balance active mixer. It is widely used to achieve good port-to-port isolation,

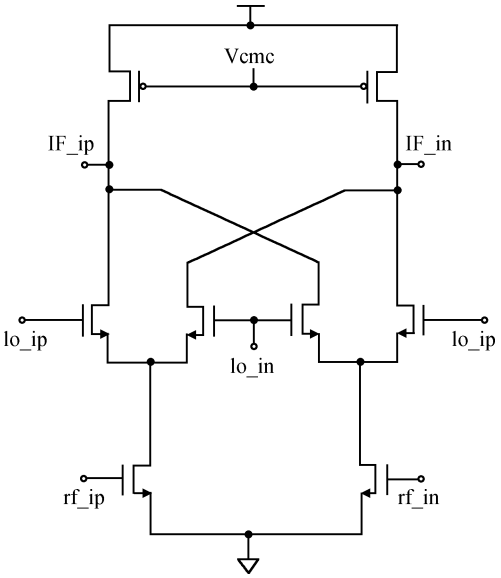


Fig. 4. Typical Gilbert mixer.

a medium noise figure and a moderate conversion gain.

However, the linearity of this configuration is bounded by the input NMOS transconductor and the voltage supply[8]. To improve linearity, a proper Gilbert mixer is presented in this paper, which can operate at low supply voltages by folding the input transconductor stage.

The transconductor and switch stage can be biased separately in the folded cascode structure, which can supply more voltage headroom for both stages[9]. Flicker noise can be reduced by minimizing the DC current of the switches, meanwhile, the required linearity can be satisfied by biasing the transconductor stage appropriately. In fact, the folded cascode mixer has the same theory to improve linearity as immitting current to transconductor stage[2], which optimized the noise figure and linearity simultaneously.

As described in Fig. 1, the whole mixer includes a transconductance stage, active switches, RC-CR, LO buffer and TIA buffers. The main block of folded Gilbert mixer is depicted in Fig. 5, and the diagrams of LO buffer and RC-CR are shown in Fig. 6.

The transconductance stage of folded Gilbert mixer, loaded by an on-chip LC tank, is a differential common-source amplifier with resistive degeneration. Although resistive degeneration adds noise, its advantage for improving linearity is clear too. To reduce power consumption, one common transconductance stage is used for both IQ paths.

Mixing is achieved by the active switches, which are biased with few DC current to reduce the flicker noise of mixer. Furthermore, the common mode noise produced by the switch-transistors and LO port, is rejected at the differential output.

The transconductance stage performs a voltage to current conversion of the RF signal, and, then, the current signal can be commuted by the local oscillator (LO) through the active switches. Following the quadrature active switches, there is a TIA buffer at both I and Q paths. It performs as a current-to-voltage converter and also a first order low pass filter.

For a quadrature mixer, a better orthogonality can minimize the image interference. As shown in Fig. 6, the LO signal

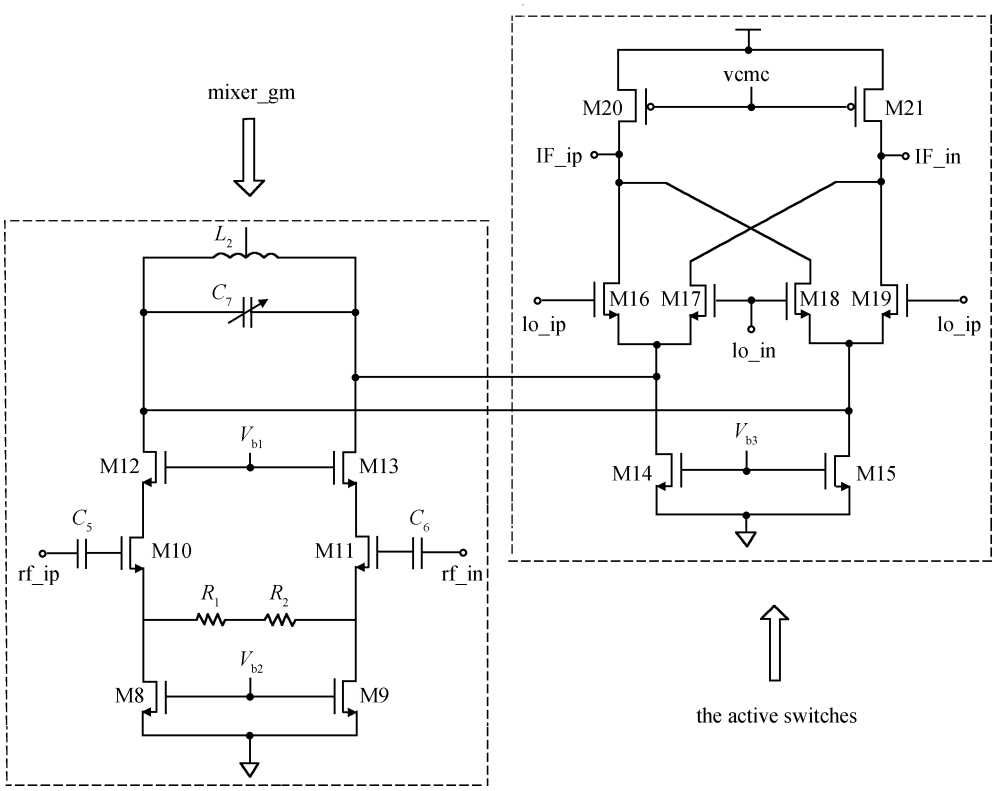


Fig. 5. Main block of folded Gilbert mixer.

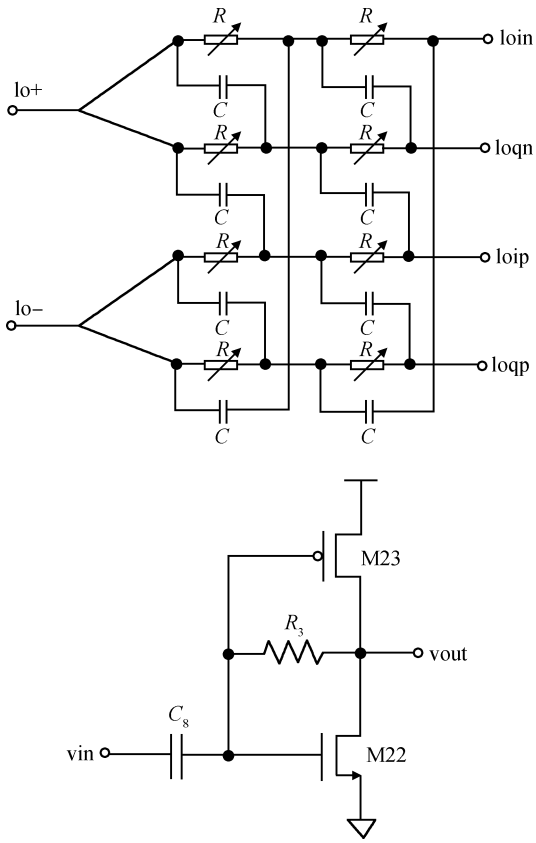


Fig. 6. RC-CR and LO buffer.

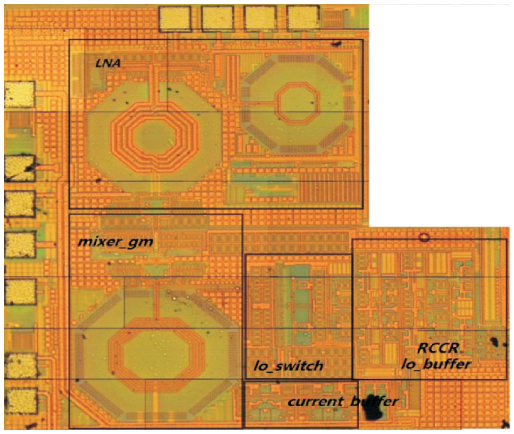


Fig. 7. Die photograph of the receiver front end.

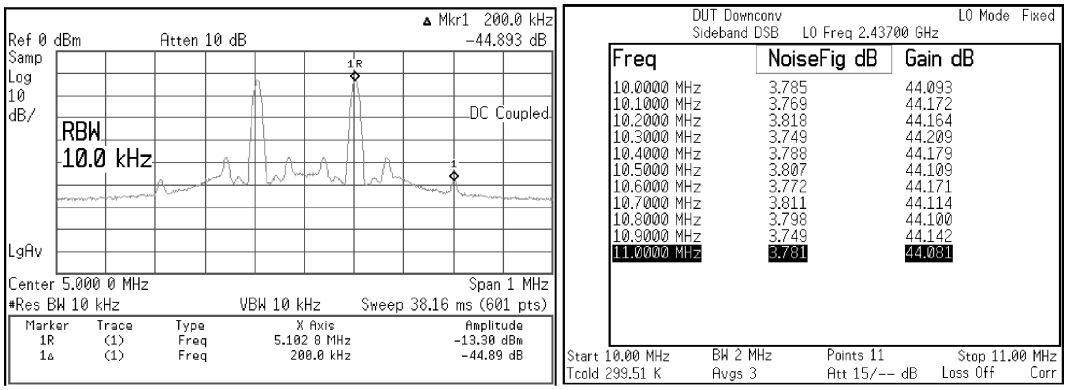
Table 1. Summary of WLAN front-end performance.

Parameter	Measured value		
	HG	MG	LG
Conversion gain (dB)	44	29	12
DSB noise figure (dB)	3.75	14	30
IIP3 (dBm)	–31	–16	0
Current consumption (mA)	21		
Supply voltage (V)	1.2		
Area (mm^2)	0.612		
Technology	0.13 μm CMOS		

is converted from differential to orthogonal locally by using a RC-CR circuit and amplified by a LO buffer to guarantee its amplitude. Even for long running layout lines of differential RF signal, the local orthogonal LO signal achieves a good performance.

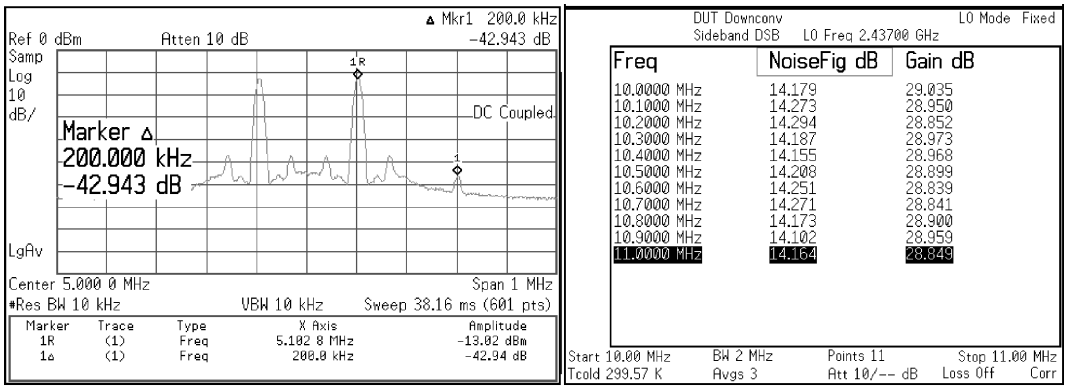
Table 2. Front-end performance comparison.

Parameter	Ref. [10]	Ref. [11]	Ref. [12]	This work
Process	0.18 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS
Support voltage (V)	1.2	1.8	1.5	1.2
Architecture	Low-IF	N/A	Low-IF	Zero-IF
Noise figure (dB)	5	3.9 (only LNA)	3.1	3.75
IIP3 (dBm)	N/A	N/A	–12	–31
Gain (dB)	43 (total receiver)	12.9 (only LNA)	30	44
Area (mm^2)	N/A	N/A	1.1	0.612
Current consumption (mA)	2.2	8	8	21



(a) High gain mode IIP3 (b) High gain mode NF DSB and gain

Fig. 8. Measurement result of the front end at high gain mode.



(a) Middle gain mode IIP3 (b) Middle gain mode NF DSB and gain

Fig. 9. Measurement result of the front end at middle gain mode.

4. Measurement results

The front end of the receiver is designed and fabricated in a 0.13 μm CMOS technology with 1.2 V power supply. The die photograph of the whole front end, which only occupies 0.612 mm^2 die size, is shown in Fig. 7.

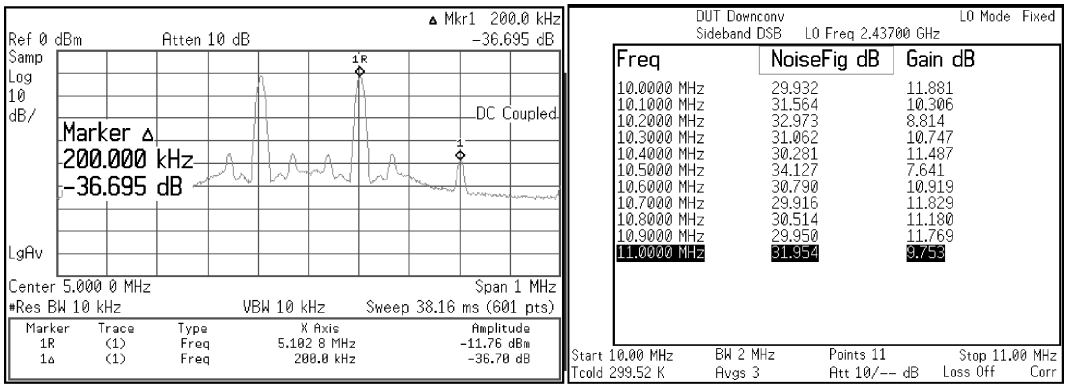
The measured noise figure, conversion gain and IIP3 of the front end at different gain modes are shown in Figs. 8–10, respectively. The spur in the spectrum, which is close to the first-order IF output, is caused by the PLL output spurs.

Since the lowest operating frequency of the noise figure analyzer is 10 MHz, the noise figure and conversion gain are measured with the IF output at 10–11 MHz. The input frequency of the two tone testing for IIP3 is setting at 2.4419 and 2.4421 GHz, with the first-order IF output at 4.9 and 5.1 MHz. Meanwhile, the input power is –53, –37 and –14 dBm at different gain modes.

Based on the following formulation, the linearity of front end at different modes is gotten.

$$\mathrm{IIP_3(dBm)} = P_{\mathrm{in}} + \frac{P_{\mathrm{1st}} - P_{\mathrm{3rd}}}{2}. \tag{6}$$

In general, the measured results of the front end are listed in Table 1. Table 2 compares the proposed front end with the recently reported CMOS receiver's front end. It can be seen that this work shows a better performance on less die area, low noise figure and high conversion gain.



(a) Low gain mode IIP3 (b) Low gain mode NF DSB and gain

Fig. 10. Measurement result of the front end at low gain mode.

5. Conclusion

A 2.4 GHz zero-IF direct conversion receiver front end, which is implemented in a 0.13 μm CMOS technology, has been presented in this paper. The front end includes an inductive degeneration common-source LNA and a quadrature folded Gilbert mixer. As the load of an LNA, the on-chip transformer is optimized for lower resistive loss and higher power gain. The front end draws 21 mA from 1.2 V and attains a measured DSB NF of 3.75 dB, a conversion gain of 44 dB and IIP3 of –31dBm at maximum gain setting. The front end occupies 0.612 mm^2 die size in the 0.13 μm CMOS technology.

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