High performance QVCO design with series coupling in CMOS technology*

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Abstract: A high performance quadrature voltage-controlled oscillator (QVCO) is presented. It has been fabricated in SMIC 0.18 μm CMOS technology with top thick metal. The proposed QVCO employed cascade serial coupling for in phase and quadrature phase signal generation. Source degeneration capacitance is added to the NMOS differential pair to suppress their flicker noise from up-conversion to close in phase noise. A dedicated low noise and high power supply rejection low drop out regulator is used to supply this QVCO. The measured phase noise of the proposed QVCO achieves phase noise of –123.3 dBc/Hz at an offset frequency of 1 MHz from the carrier of 4.78 GHz, while the QVCO core circuit and LDO draw 6 mA from a 1.8 V supply. The QVCO can operate from 4.09 to 4.87 GHz (17.5%). Measured tuning gain of the QVCO (K_{vco}) spans from 44.5 to 66.7 MHz/V. The chip area excluding the pads and ESD protection circuit is 0.41 mm^2.

Key words: QVCO; CMOS; $1/f$ noise; phase noise; series coupling

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1. Introduction

A fully integrated VCO is a key building block in a modern transceiver. It is the most important and difficult block for a fully integrated phase locked loop (PLL), which serves as local oscillator (LO) signals for modulation or demodulation.

The VCO determines the outband phase noise of the PLL system, as the PLL features a high pass transfer function for VCO phase noise. Therefore, designers usually focus on VCO phase noise at the out band frequency offset. However, for an integer frequency synthesizer in a communication system with narrow channel spacing or a fractional synthesizer with large sigma–delta modulator (SDM) quantization noise, narrow loop bandwidth is desired. Then the upconversion of the device's flicker noise into phase noise would be a problem. In addition, the advance into deep submicron technologies makes the flicker noise corner frequency up to hundreds of kHz or MHz. Recently, the development of phase noise analysis theory[1,2] laid the foundation for developing new VCO topology to improve its phase noise in the close-in $1/f^3$ region and $1/f^2$ region. Ismail[3] proposed a VCO with capacitance degeneration to reduce flicker noise corner frequency based on frequency domain theory. Soltannian[4,5] implemented improved VCO and QVCO through pulsed biasing, which is based on Hajimiri's time domain analysis method. Jerng[6] reported that we can minimize flicker noise upconversion by using an all-PMOS VCO and reducing the transistor size to increase the switch on resistor (R_{on}). Levantino[7] first proposed a VCO without a current source to remove its flicker noise and thermal noise at the second harmonic frequency, then more recently suggested improved topology by inserting a resistor into the drain of the negative-G_m transistors to further suppress flicker noise from switching transistors[8].

Quadrature signals from a VCO are desired for a fully integrated zero-IF or low-IF transceiver. Many techniques have been developed to generate quadrature signals[9], such as a VCO followed by RC–CR phase shift network; a double frequency VCO with /2 divider; and a ring oscillator and two LC VCOs with inverse coupling transistors. Among these, an LC VCO with inverse coupling transistors is the best fully integrated candidate owing to its good phase noise and phase error.

The first QVCO of this kind was proposed by Rofougaran[10]. It had been briefed as a parallel coupling QVCO, which shows a large frequency shift from resonance frequency, causing a degraded quality factor of the tank and then bad phase noise performance. An improved method was proposed by adding a phase shift network[11] to the parallel coupling transistors. Sub-harmonic coupling through a transformer[12] shows much better phase noise performance than a conventional QVCO, sacrificing the extra chip area occupied by a coupling transformer. Andreani[13] proposed a serial coupling technique without increasing the chip area and power consumption, compared with a phase-shift parallel QVCO and a transformer coupling QVCO.

In this paper, we present a fully integrated QVCO with cascade serial coupling. Complementary cross-coupled pair and cascade coupling without a tail current source[14] are exploited to implement a fully differential QVCO to suppress flicker noise upconversion. Additional capacitance degeneration is used to further suppress flicker noise from the NMOS cross-coupled pair. Four bit differential switched capacitor arrays are added to cover a large tuning range with a small K_{vco}. The measured results show that the QVCO can operate from

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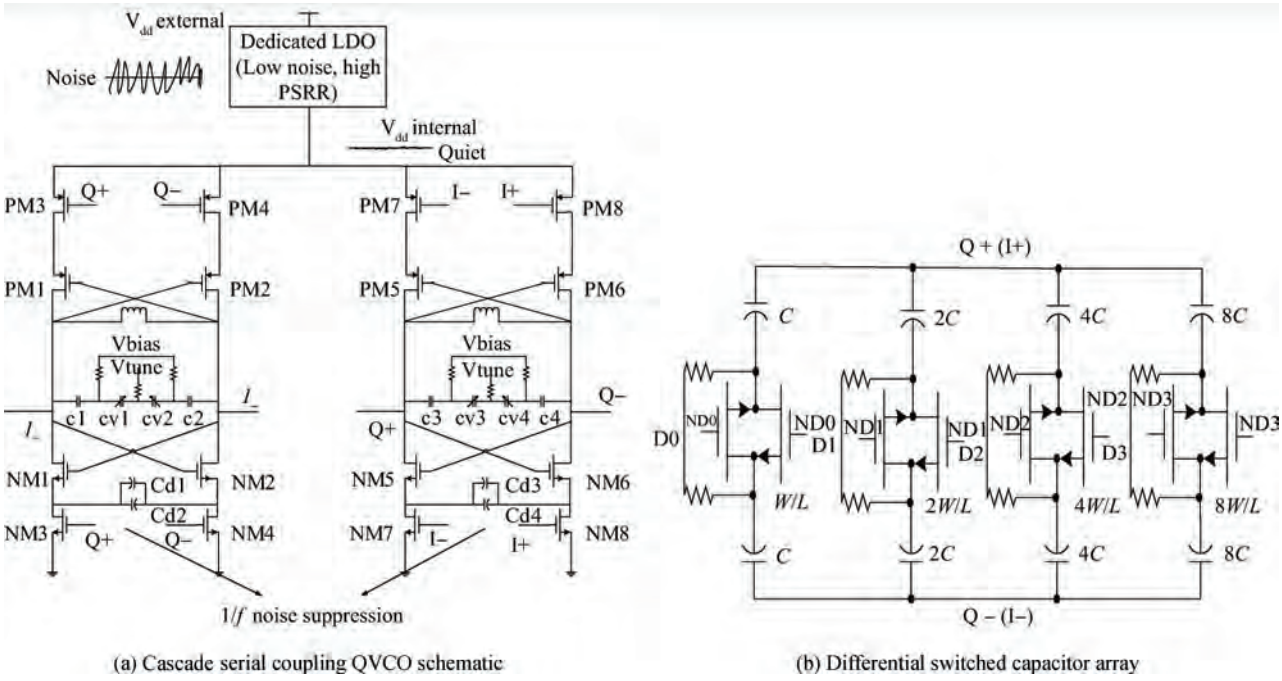

Fig. 1. Quadrature VCO schematic.

4.09 to 4.87 GHz with good phase noise performance.

2. Circuit design and analysis

The proposed QVCO circuit is shown in Fig. 1. Complementary cross-couple pairs NM1, NM2 and PM1, PM2 (NM5, NM6 and PM5, PM6) are employed to generate a negative resistor to compensate energy loss from the on-chip planar inductor. Cascade serial coupling is used to couple those two LC-VCOs to a ring-based QVCO. Although cascade serial coupling QVCO consumes more voltage headroom than their conventional NMOS or PMOS only serial coupling counterpart, it is preferred in this paper as complementary VCO with this coupling structure constructs a fully symmetrical circuit. The proper dimensions of MOS transistors in this QVCO would generate a more symmetrical output waveform than conventional serial coupling, which is very helpful to suppress flicker noise upconversion. The tail current source is omitted to enlarge the output voltage swing, but the sensitivity to power supply noise is increased[7]. To solve this problem, a dedicated LDO is employed to provide a clean supply for the supply sensitive QVCO, making sure of robust operation of the QVCO under a noisy system-on-chip (SOC) environment.

2.1. Device noise and phase noise optimization

The proposed QVCO has no tail current source that eliminates a big phase-noise contributor. Noise sources in active devices consist of thermal noise and flicker noise in energy compensation transistors (NM1, NM2, PM1, PM2, NM5, NM6 and PM5, PM6) and coupling transistors (NM3, NM4, PM3, PM4, NM7, NM8 and PM7, PM8). They are the main contributors to phase noise of this QVCO.

A parasitic resistor in low quality on chip planar inductors (L_1, L_2) is an important parameter for LC VCO design. The bigger the parasitic resistor, the larger the energy loss. Then more power from the supply is needed to compensate the loss, which could degrade the phase noise if the VCO operates under a voltage limited region. A small inductor is preferred as it shows little parasitic resistor and wide tuning range. However, a small inductor will degrade the phase noise and increase the power consumption of the VCO, which is verified in Ref. [9]. Therefore, tradeoffs between phase noise, power consumption and tuning range can be reached by optimizing the inductance of the planar inductor.

All the transistors in this QVCO are chosen to be the minimum length to minimize parasitic capacitances for high frequency operation and large tuning range, although References [15, 16] propose a non-minimum length to suppress flicker noise in those transistors. Transistors NM1, NM2 (NM5, NM6) and PM1, PM2 (PM5, PM6) are designed to guarantee safety start-up over process and temperature corners for a given current budget. Coupling transistors NM3, NM4 (NM7, NM8) and PM3, PM4 (PM7, PM8) operate in the triode region, then their W/L is designed to be larger than the negative resistor transistors to meet an optimum coupling ratio $G_{\rm mc}/G_{\rm m} = 0.47$[13]. In this circuit, $g_{\rm NM3} = g_{\rm PM3}$, $g_{\rm NM4} = g_{\rm PM4}$ are chosen to achieve a symmetric waveform to suppress flicker noise upconversion. NM1, PM1 (NM2, PM2) and their coupling transistors NM3, PM3 (NM4, PM4) in the QVCO are put in fast switching, therefore their flicker noise will be removed[17]. Simulation shows that the flicker noise of NM1, 2 is still the main contributor to phase noise in the $1/f^3$ region in this circuit as the waveform is not perfectly symmetrical. The phase noise in the $1/f^2$ region is determined by the loaded quality factor (Q) of the tank and thermal noise in transistors NM1, NM2 and PM1, PM2 under the given current budget.

To further suppress flicker noise upconversion from NM1, NM2, a capacitance connected to sources of NM1, NM2 are

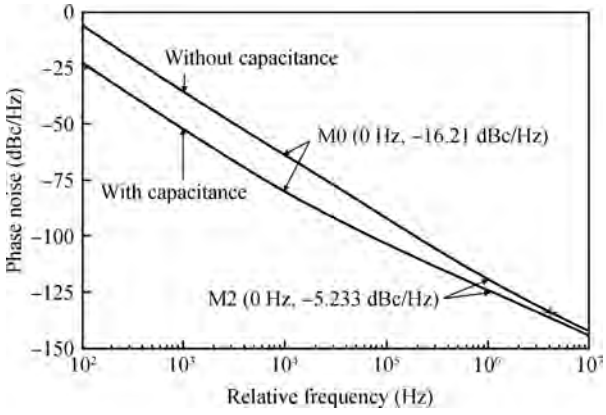

Fig. 2. Simulated phase noise with and without source connected capacitance.

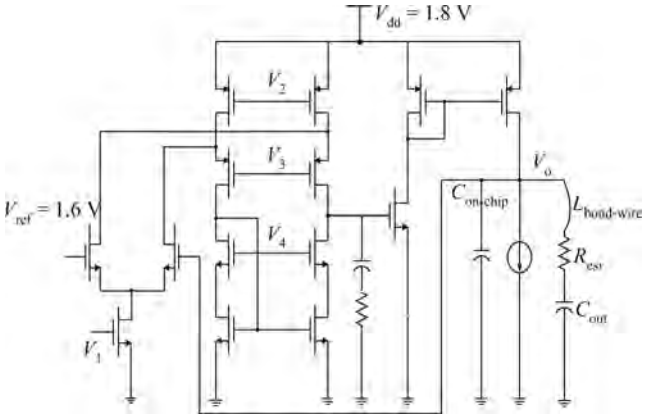

Fig. 3. Schematic of the LDO.

added. Similar capacitance was also added by Ismail[3], but the mechanism was totally different. Since coupling transistors NM3, NM4 are added, there mainly exists a fundamental frequency component in the sources of NM1 and NM2. However, in Ref. [3], the capacitance is used to suppress the second harmonic frequency voltage. The capacitors consist of two MIM capacitors C_{d1}, C_{d2} (C_{d3}, C_{d4}) with an inverse connection to suppress unsymmetrical which is introduced by parasitic capacitance of the MIM CAP. Simulated phase noise with and without the capacitance is shown in Fig. 2. 16.2 dB and 5.2 dB phase noise reduction at 10 kHz and 1 MHz offset are achieved with the proposed source connected capacitor, demonstrating its effectiveness in improving phase noise, especially in the $1/f^3$ region.

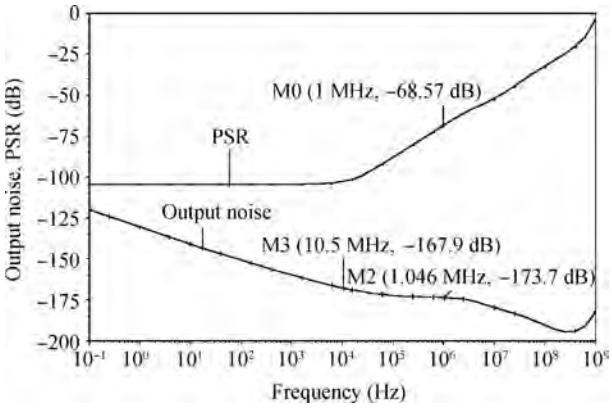

Fig. 4. Simulated output noise and PSR of the LDO.

2.2. Tuning range design

Small tuning sensitivity of the VCO is desired in PLL, as noise from the blocks in the PLL preceding the VCO feed to its control line and degrade the overall phase noise performance of the PLL through this K_{vco}. In addition, the smaller the K_{vco}, the bigger the charge pump current (I_{cp}) is under a given loop bandwidth. Then the phase noise contribution from the PFD/CP will be suppressed, which is the main contributor of in-band phase noise. However, wide frequency tuning is always preferred in modern communication systems. In this paper, a switched capacitor array[18] is used to cover the required frequency tuning range and PVT variations with reasonable K_{vco}. Finally, we adopted a differential switched capacitor in Ref. [19], which is better quality than its single ended counterpart. The width of this switch also shows a tradeoff between the quality of the loaded tank (then phase noise performance) and the tuning range, which had been optimized by simulation. In this paper, the switch is split into two transistors with an inverse connection of source and drain to guarantee symmetry, as shown in Fig. 1(b). An accumulation MOS (AMOS) varactor is used for continuous frequency tuning of the VCO. Although the varactor shows high quality, MIM capacitor tapping is still added to further improve the quality of the fine tune branch. Another advantage of this tapping is the reduced voltage swing across the varactor, which will linearize the $C-V$ curve and reduce AM noise to FM noise conversion.

2.3. LDO design

The proposed QVCO without a tail current source is highly sensitive to supply noise, which is disastrous in a large mixed signal environment. A dedicated LDO with low noise and high power supply rejection (PSR) is designed in this paper to supply the QVCO. The schematic of the proposed LDO is shown in Fig. 3.

The diode connected transistor proposed in Ref. [20] is employed in this LDO to enhance its PSR. The resistor feedback network is eliminated to improve the PSR and reduce output noise. A large external ceramic capacitor is used to stabilize this LDO, but an on-chip MIM capacitor is also added to filter out high orders of harmonic frequency components, which can't be filtered by an off-chip capacitor due to bonding wire inductance and the limited self-resonance frequency of the ceramic capacitor. Since the open loop gain of the LDO determines the PSR at DC, a folded cascade error amplifier that shows large gain is employed. With the LDO to supply the QVCO, the supply pushing level of the QVCO is reduced from 87 MHz/V to 280 kHz/V. Co-simulation of the QVCO and LDO shows that the LDO has nearly no effect on the QVCO phase noise. Simulated PSR and noise performance of the LDO is shown in Fig. 4.

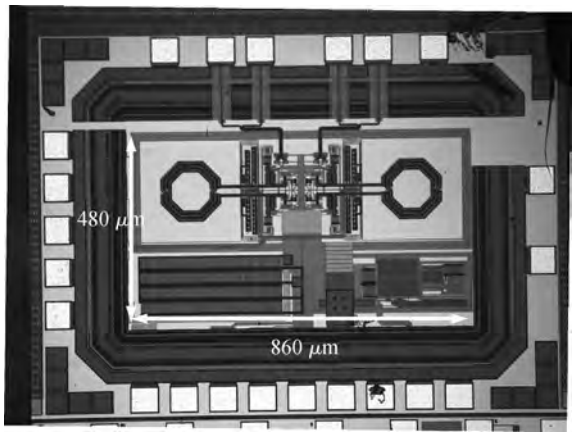

Fig. 5. Chip photograph of proposed QVCO.

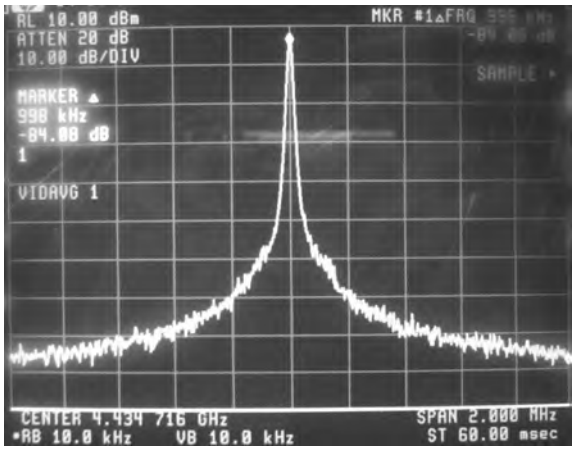

Fig. 6. Output spectrum of the QVCO at 4.43 GHz.

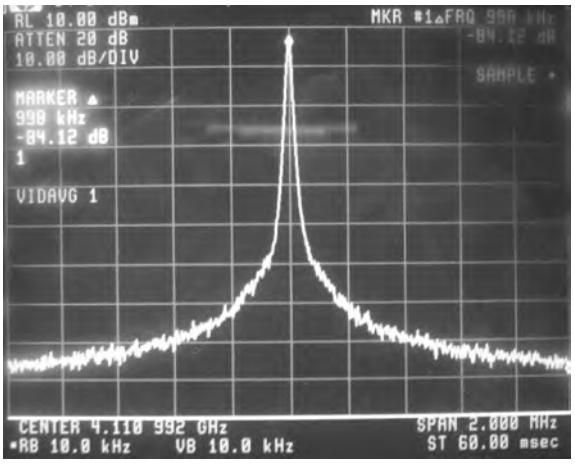

Fig. 7. Output spectrum of the QVCO at 4.11 GHz.

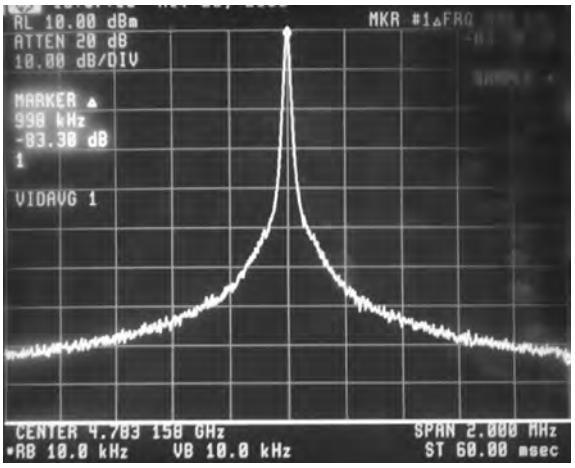

Fig. 8. Output spectrum of the QVCO at 4.78 GHz.

3. Measurement results

Prototypes of this QVCO are fabricated by SMIC 0.18 μm CMOS technology. The inductors in this circuit are implemented in thick top metal, which can be clearly identified in the die photograph in Fig. 5. All the NMOS transistors in the core of the QVCO are implemented by a triple well device to isolated noise coupling from the substrate. The core chip area is 0.48×0.86 mm^2. All the pads are electronic-discharge (ESD) protected. The RF output pads and DC pads are separated into two different pad rings to eliminate parasitic capacitive coupling.

The chip is directly bonded to a FR4 PCB without packaging. Differential signals are converted to a single ended signal by a discrete balun (BD3150N50100A00) and then amplified by an off-chip amplifier (MNA-7) to improve the measurement accuracy.

Figure 6 shows a typical output spectrum of this QVCO at 4.43 GHz. The measured phase noise is –124.1 dBc/Hz at 1 MHz offset from the carrier. Spectra at 4.11 GHz and 4.43 GHz are shown in Figs. 7 and 8. They measure –124.1 dBc/Hz at 1 MHz offset of 4.11 GHz and –123.3 dBc/Hz at 1 MHz offset of 4.78 GHz. All those spectra are measured with a $V_{\rm tune}$ setting to 0.9 V, which is the middle of each sub-band tuning curve. The power consumption of this QVCO is 6 mA at a 1.8 V supply, excluding the output buffer. The overall measured power consumption is 11.2 mA at a 1.8 V supply, where the output buffer consumes 5.2 mA.

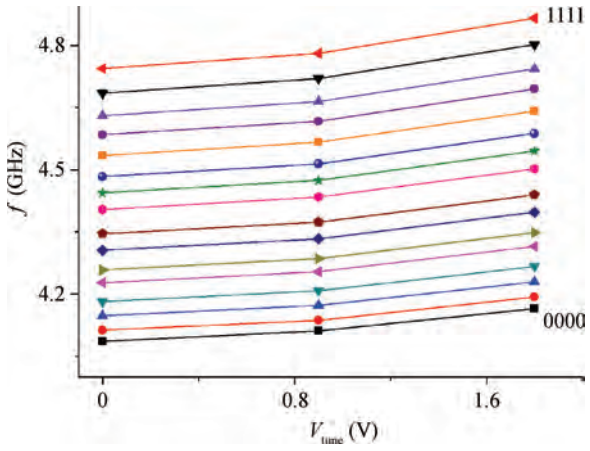

Fig. 9. Measured tuning range of the QVCO.

Figure 9 shows the measured and simulated $f-V$ curves. The frequency tuning range spans from 4.09 to 4.87 GHz (17.5%), which consists of sixteen overlapping sub-bands. The $K_{\rm vco}$ of the QVCO spans from 44.5 to 66.7 MHz/V.

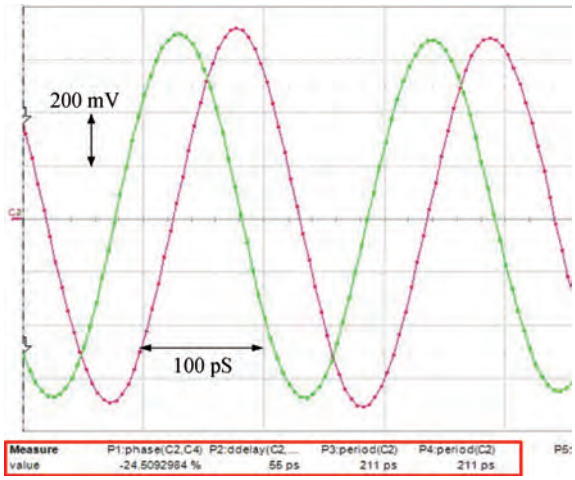

Fig. 10. Measured quadrature signals of the QVCO.

Figure 10 shows the transient waveform of the QVCO measured by Lecroy's sampling oscillograph. The phase error is estimated by statically analyzing the waveform, and the averaged phase error is 1.8 degrees while post layout simulation shows a phase error of less than one degree across the tuning range. The direct transient measurement of the phase error is not accurate as the time delay of high frequency IQ signals is sensitive to the bondwire length and transmission line length mismatch.

To compare with other published state of art, three commonly used figures of merit, FOM, $\mathrm{FOM_A}$[5] and $\mathrm{FOM_T}$[21], are used. They are defined as

$$\mathrm{FOM} = -L(f_0, \Delta f) + 20\lg\frac{f_0}{\Delta f} - 10\lg\frac{P}{1\,\mathrm{mW}},$$

$$\mathrm{FOM_A} = \mathrm{FOM} - 10\lg\frac{A}{1\,\mathrm{mm^2}},$$

$$\mathrm{FOM_T} = \mathrm{FOM} + 20\lg\frac{\mathrm{FTR}}{10},$$

where $L(f_0, \Delta f)$ is the single side band phase noise of f_0 at Δf offset. P is the power consumption of the circuit in mW, A is the chip area in $\mathrm{mm^2}$ and FTR is the frequency tuning range in percent. For this QVCO, the calculated FOM, $\mathrm{FOM_A}$ and $\mathrm{FOM_T}$ are 186.6 dB, 190.5 dB and 191.5 dB, respectively. A performance comparison with previous published work is shown in Table 1.

4. Conclusion

We have presented a fully integrated high performance QVCO in this paper. It is fabricated by a SMIC 0.18 μm CMOS process with chip area of 0.41 $\mathrm{mm^2}$. The QVCO can be tuned from 4.09 to 4.87 GHz (17.5%). The measured phase noise across the tuning range varied from –123.3 to –124.1 dBc/Hz at 1 MHz offset. The oscillator consists of the QVCO and LDO drawing 6 mA from a 1.8 V supply. We have compared this QVCO with published state of the art from different aspects. The achieved FOM, $\mathrm{FOM_A}$ and $\mathrm{FOM_T}$ are 186.6, 190.5 and 191.5, respectively, which are comparable to the published state of the art.

Table 1. Comparison with previous state of the art.

Reference	Ref. [5]	Ref. [9]	Ref. [12]	Ref. [22]	This work
Tech (μm)	0.25[a]	0.25	0.25	0.18	0.18
f_0 (GHz)	2.07	1.8	4.9	5.1	4.78
PN @ 1 MHz (dBc/Hz)	–124.4	–135	–124	–132.6	–123.3
P (mW)	3	20	22	27.7	10.8
FTR (%)	18	17[b]	13	19	17.5
Area ($\mathrm{mm^2}$)	0.625	1.05[c]	NA[d]	3.42	0.41
FOM (dB)	186	185.5	185.1	192	186.6
$\mathrm{FOM_A}$ (dB)	188	184.8	NA	186.6	190.5
$\mathrm{FOM_T}$ (dB)	191.1	189.1	187.4	197.6	191.5

[a] BICMOS technology. [b] Differentially tuning. [c] Including test pads. [d] Five inductors are used in this chip.

References

[1] Rael J J, Abidi A A. Physical processes of phase noise in differential LC-oscillators. Proc IEEE Custom Integrated Circuits Conf, 2000: 569

[2] Hajimiri A, Lee T H. A general theory of phase noise in electrical oscillators. IEEE J Solid-State Circuits, 1998, 33(2): 179

[3] Ismail A, Abidi A A. CMOS differential LC oscillator with suppressed up-converted flicker noise. IEEE Int Solid-State Circuits Conf Dig Tech Papers, 2003: 98

[4] Soltanian B, Kinget P R. Tail current-shaping to improve phase noise in LC voltage-controlled oscillators. IEEE J Solid-State Circuits, 2006, 41(8): 1792

[5] Soltanian B, Kinget P. A low phase noise quadrature LC-VCO using capacitive common-source coupling. Proc ESSCIRC, 2006: 436

[6] Jerng A, Sodini C G. The impact of device type and sizing on phase noise mechanisms. IEEE J Solid-State Circuits, 2005, 40(2): 360

[7] Levantino S, Samori C, Bonfanti A, et al. Frequency dependence on bias current in 5-GHz CMOS VCOs: impact on tuning range and flicker noise upconversion. IEEE J Solid-State Circuits, 2002, 37(8): 1003

[8] Levantino S, Zanuso M, Samori C, et al. Suppression of flicker noise upconversion in a 65nm CMOS VCO in the 3.0-to-3.6 GHz band. IEEE International Solid-State Circuits Conference, 2010: 50

[9] Tiebout M. Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS. IEEE J Solid-State Circuits, 2001, 36(7): 1018

[10] Rofougaran A, Rael J, Rofougaran M, et al. A 900 MHz CMOS LC-oscillator with quadrature outputs. IEEE ISSCC Dig Tech Papers, 1996: 392

[11] Van der Tang J, van de Ven P, Kasperkovitz D, et al. Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator. IEEE J Solid-State Circuits, 2002, 37(5): 657

[12] Gierkink S L, Levantino S, Frye R C, et al. A low-phase-noise 5-GHz CMOS quadrature VCO using super-harmonic coupling. IEEE J Solid-State Circuits, 2003, 38(7): 1148

[13] Andreani P, Bonfanti A, Romanò L, et al. Analysis and design of a 1.8-GHz CMOS LC quadrature VCO. IEEE J Solid-State Circuits, 2002, 37(12): 1737

[14] Chang J H, Youn Y S, Park M Y, et al. A new 6 GHz fully integrated low power low noise CMOS LC Quadrature VCO. Proc IEEE RFIC Symp, 2003: 307

[15] Berny A D, Niknejad A M, Meyer R G. A wideband low-phase-noise CMOS VCO. Proc IEEE Custom Integrated Circuits

Conf, 2003: 555
[16] Berny A D, Niknejad A M, Meyer R G. A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration. IEEE J Solid-State Circuits, 2005, 40(4): 909
[17] Klumperink E A M, Gierkink S L J, van der Wel A P, et al. Reducing MOSFET $1/f$ noise and power consumption by switched biasing. IEEE J Solid-State Circuits, 2000, 35(7): 994
[18] Kral A, Behbahani F, Abidi A A. RF-CMOS oscillators with switched tuning. Proc IEEE Custom Integrated Circuits Conf, 1998: 555
[19] Sjöland H. Improved switched tuning of differential CMOS VCOs. IEEE Trans Circuits Syst II, Analog Digit. Signal Process, 2002, 49(5): 352
[20] Hoon S K, Chen S, Maloberti F, et al. A low noise, high power supply rejection low dropout regulator for wireless system-on-chip applications. Proc IEEE Custom Integr Circuits Conf, 2005: 754
[21] Kim J, Plouchart J O, Zamdmer N, et al. Power-optimized widely-tunable 5-GHz monolithic VCO in a digital SOI CMOS technology on high resistivity substrate. Proc Int Symp Low Power Electronics and Design, 2003: 434
[22] Yao C W, Willson A N. A phase noise reduction technique for quadrature LC-VCO with phase-to-amplitude noise conversion. IEEE ISSCC Dig Tech Papers, 2006: 196