A novel power amplifier structure for RFID tag applications*

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Abstract: A novel matching method between the power amplifier (PA) and antenna of an active or semi-active RFID tag is presented. A PCB dipole antenna is used as the resonance inductor of a differential power amplifier. The total PA chip area is reduced greatly to only 240 × 70 μm^2 in a 0.18 μm CMOS process due to saving two on-chip integrated inductors. Operating in class AB with a 1.8 V supply voltage and 2.45 GHz input signal, the PA shows a measured output power of 8 dBm at the 1 dB compression point.

Key words: power amplifier; CMOS; class AB; RFID

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1. Introduction

Radio frequency identification (RFID) tags are a rapidly growing field with many emerging technologies and applications. An RFID tag can be divided into three categories: the active tag, the passive tag and the semi-active tag. Active tags use a battery to power the circuits and actively send RF signals through a power amplifier (PA). Passive tags can receive power from the antenna from the interrogator and communicate through backscatter, but the identification distance is short. Semi-active tags have the advantages of both passive tags and active tags; they operate in passive mode when they are close to the transceiver and in active mode when far from the transceiver[1, 2].

Therefore, an RFID tag with a power amplifier is a good solution for improving identification distance. Many fully integrated CMOS PAs have been developed with high linearity. However, too many on-chip RF inductors are used in the designs[3, 4]. Since an on-chip RF inductor always occupies a very large area, the manufacturing cost increases as a result. Some other PAs take advantage of off-chip inductors and obtain a good performance[5, 6], but that leads to a low integration density. This paper demonstrates a novel differential PA design, using a PCB antenna as one part of the PA circuit. Based on this kind of structure, the use of on-chip RF inductors is avoided, which enables the PA to be fabricated in CMOS process without inductors. Moreover, only a differential PA can output to a dipole antenna directly. Table 1 shows a brief PA performance comparison.

The PA was fabricated in a 0.18 μm 1P6M CMOS process. Measurements show that it satisfies EPC global Class-1 Gen-2 with a linear output power of 8 dBm.

2. Circuit implementation

In the design, a class-AB differential PA is adopted to satisfy the linearity demand from the EPC global Class 1 Generation 2 Protocol[7, 8]. The implemented PA is shown in Fig. 1.

M1–M4 and C_{O1}–C_{O2} are all on-chip components. On the basis of antenna design theory, the input impedance of the PCB antenna is designed to provide inductance and resistance in series[9]. Figure 2(a) shows the dipole antenna equivalent circuit.

Table 1. Performance comparison of PAs.

Inductor type of PA	Supply voltage (V)	$P_{1\text{-dB}}$ (dBm)	Chip area (mm^2)
On-chip[3]	3.3	24.8	1.4 × 0.75
Off-chip[4]	3.3	10.6	1.5 × 1
This work	1.8	8	0.24 × 0.70

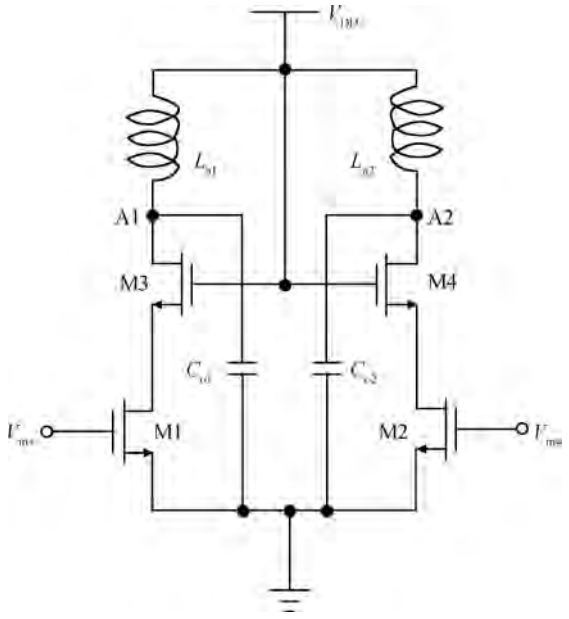

Fig. 1. Schematic of PA.

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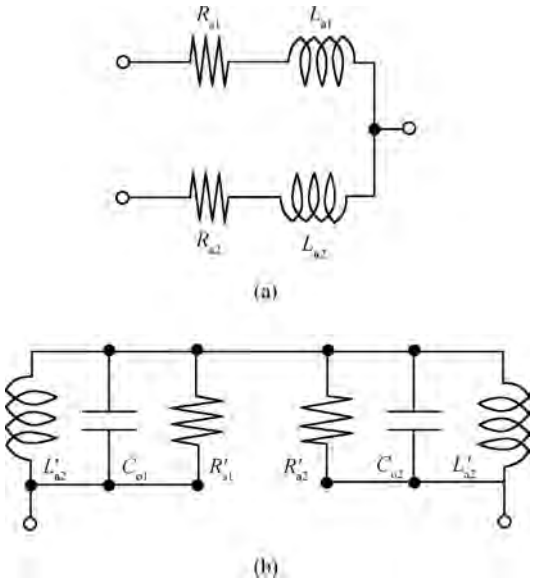

Fig. 2. (a) Equivalent circuit of the dipole antenna. (b) Equivalent RLC resonant circuit.

L_{a1} and L_{a2} are the equivalent inductances; R_{a1} and R_{a2} are the equivalent radiation resistances. Together with the on-chip capacitors, C_{O1} and C_{O2}, they form RLC resonant circuits, which resonate in the operating frequency to filter the second harmonic and above. Figure 2(b) shows the equivalent RLC resonant circuit. Assume that $L_{a1} = L_{a2} = L_a$ (R_a, C_O, L'_a and R'_a are the same), then:

$$R'_a = R_a(Q^2_{RLC} + 1), \tag{1}$$

$$L'_a = L_a \frac{Q^2_{RLC} + 1}{Q^2_{RLC}}. \tag{2}$$

Q_{RLC} represents the Q value of the resonant circuit.

$$Q_{RLC} = \frac{R'_a}{\sqrt{L'_a/C_O}}. \tag{3}$$

The maximum output power $P_{OUT\,max}$ of the PA is determined as follows by load impedance R'_a and the supply voltage V_{DD}.

$$P_{OUT\,max} = \frac{V^2_{DD}}{2R'_a} \times 2. \tag{4}$$

To work at 2.45 GHz and obtain an appropriate Q_{RLC}, the L_a of 5 nH is designed. The on-chip capacitance is 650 fF in consideration of parasitic capacitance. R_a is 26 Ω since the expected maximum total output power of the PA is 10 dBm with the supply voltage of 1.8 V.

A differential structure and a cascode configuration have been used in the design. Due to the symmetry of the differential structure, the noise coupling through the power supply and ground connections to chips can be suppressed effectively. Also, a differential structure can reduce the sensitivity of the power amplifier to package parasitics.

According to Ref. [4], oxide breakdown is a serious issue in the design of power amplifiers in submicron CMOS. A cascode topology is chosen to improve output voltage swing of the power amplifier. As shown in Fig. 1, transistors M1–M2 act as a common source (CS) and transistors M3–M4 act as a common gate (CG). The differential RF signal is applied to V_{in+} and V_{in-}. The gates of M3 and M4 are RF grounded with supply voltage V_{DD}. The maximum voltage that CG transistors can withstand is $V_{DGC(MAX)}$.

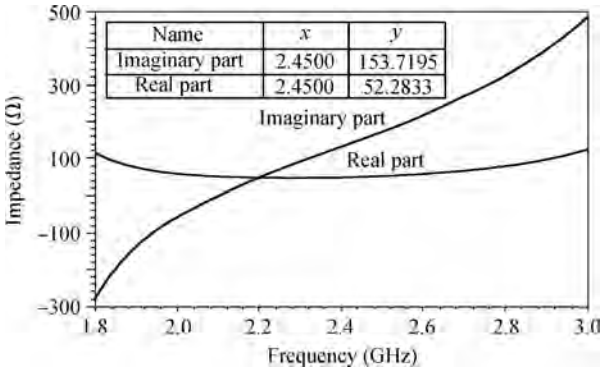

Fig. 3. Dipole antenna impedance.

$$V_{DGC(MAX)} = V_{OUT(MAX)} - V_{DD}. \tag{5}$$

$V_{OUT(MAX)}$ is the maximum output voltage of PA. The voltage that CS transistors are able to withstand is V_{DGS}.

$$V_{DGS} = V_{CASC} - V_{IN}. \tag{6}$$

V_{CASC} is the source voltage of the CG transistors. V_{IN} is the input voltage. V_{CASC} increases as V_{IN} decreases. When V_{CASC} increases to $V_{DD} - V_T$, the CG transistors are off. So the maximum voltage that CS transistors can withstand is $V_{DGS(MAX)}$.

$$V_{DGS(MAX)} = V_{DD} - V_T - V_{IN(MIN)}. \tag{7}$$

Usually, $V_{DGS(MAX)}$ is less than the gate oxide breakdown voltage ($> 2V_{DD}$) of the transistor. To prevent the transistors from breakdown,

$$V_{DGC(MAX)} = V_{DD} + 2V_{DD} = 3V_{DD}. \tag{8}$$

So the maximum output voltage is $3V_{DD}$ after using the cascade topology. While the maximum output voltage is only $2V_{DD} + V_{IN(MIN)}$ without the use of the cascode topology. $V_{IN(MIN)}$ is close to 0 or even negative.

3. Simulation and measurement results

Simulations and measurements were performed to find the antenna impedance, 1 dB compression point and spectral characteristic. The simulations were performed with Ansoft HFSS, Cadence, and the measurements with an Agilent-frequency spectrograph.

Figure 3 shows the dipole antenna impedance. The figure reveals that the real part is about 52 Ω and the imaginary part is 154 Ω, which means R_a is 26 Ω and L_a is 5 nH.

The chip was fabricated in a 0.18 μm single poly 6-metal layer (1P6M) CMOS process. A microphotograph of the PA is shown in Fig. 4. The total chip area excluding the bonding wire pads is just 240 × 70 μm^2.

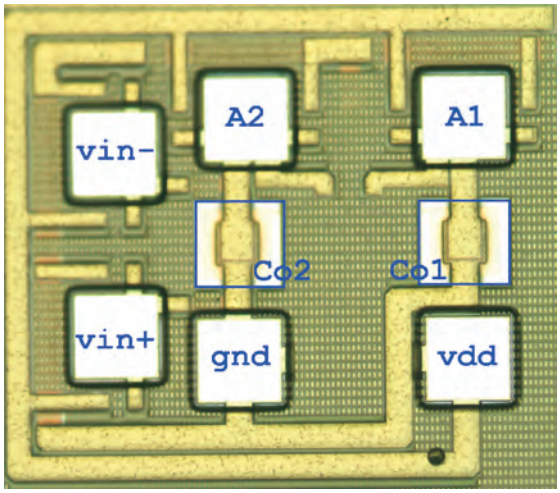

Fig. 4. Die photo of power amplifier.

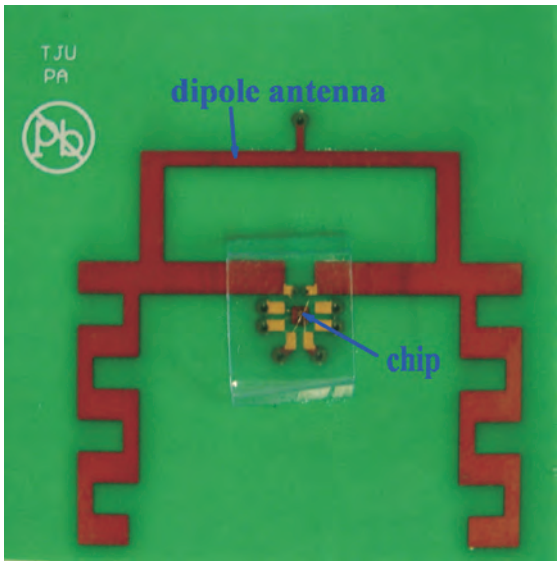

Fig. 5. One side of the PCB.

The chip was glued directly onto the PCB board using an electrically and thermally conductive adhesive. The pads were wire bonded to the gold-plated metal lines on the PCB. As shown in Fig. 5, the bare copper strip is the designed dipole antenna. An input balun transformer is appended to the circuit to generate differential input signals. To reduce the impact on antenna impedance, balun and copper traces are placed on the other side of the PCB.

The measured output power of the PA is shown in Fig. 6. The frequency of the input signal generated by the network analyzer is 2.45 GHz. The output signals are received by an Agilent E4402B frequency spectrograph. With a supply voltage of 1.8 V and gate bias voltages of 0.6 V, the PA provides an output $P_{1\mathrm{dB}}$ of 8 dBm. The post layout simulated results are also illustrated in Fig. 6. The difference between the measured and simulated power is 5 dBm, which results from the insufficient accuracy of the RF transistor models and transmission loss. The simulation results do not take process deviation into account. The characteristic impedance of the spectrum analyzer probe is 50 Ω, but output impedance matching network for test is not

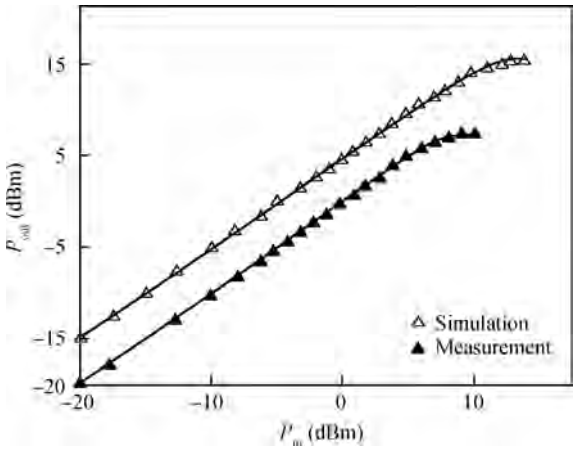

Fig. 6. Measured and simulated output power at 2.45 GHz.

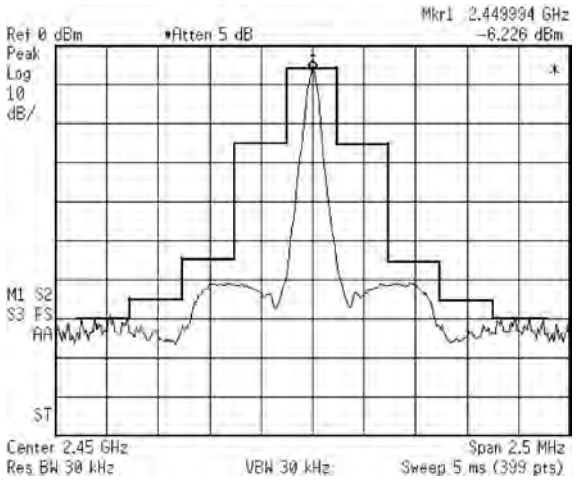

Fig. 7. Measured output spectrum and spectral mask for a multiple reader environment.

designed, which increases the power loss. This also leads to bad power added efficiency (PAE). So the measured PAE is not shown in Fig. 6. Further work is needed to improve measured characteristic.

Other important characteristics of a PA are the transmitted spectral requirements. A single carrier signal is applied to the PA. The measured result shows that the spectrum at the PA output satisfies the require spectrum mask in the multiple-reader environment condition of the EPC global Class 1 Generation 2 standard.

4. Conclusion

In this paper, a novel power amplifier design has been proposed. Associated with the design of PCB antenna, on-chip RF integrated inductors are not applied. The outputs of the PA are directly applied to a symmetrical dipole antenna with a differential structure. Based on this technique, a new matching method between the PA and antenna of an active or semi-active RFID tag is established. The total chip area is also reduced greatly to only 240 × 70 μm^2. The function of the PA is verified with 0.18 μm 1P6M CMOS process. Measurements show that the PA can provide an output power of 8 dBm at the 1 dB

compression point. Finally, the spectrum is tested for the specified EPC global Class 1 Generation 2 Standard Protocol.

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