Analysis and optimization of current sensing circuit for deep sub-micron SRAM*

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Abstract: A quantitative yield analysis of a traditional current sensing circuit considering the random dopant fluctuation effect is presented. It investigates the impact of transistor size, falling time of control signal CS and threshold voltage of critical transistors on failure probability of current sensing circuit. On this basis, we present a final optimization to improve the reliability of current sense amplifier. Under 90 nm process, simulation shows that failure probability of current sensing circuit can be reduced by 80% after optimization compared with the normal situation and the delay time only increases marginally.

Key words: current sensing; mismatch; yield and speed optimization

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1. Introduction

Memory capacities of SRAMs have been quadrupling almost every three years over the last two decades[1], which makes the capacitances of the bitlines and datalines increase significantly. The increasing bitline capacitance results in increasing time to develop enough differential bitline voltage, which degrades the performance of traditional voltage sense amplifier. This bottleneck of speed makes current sense amplifiers promising in place of voltage sense amplifiers because current sense amplifiers sense differential current instead of different voltage, which minimize the influence of large parasitical capacitance on the bitlines and improve the sensing speed. Recently a number of crosscoupled positive feedback current sense amplifiers have been proposed[2−4]. Since the sensing speed of this kind of current sensing circuit is almost independent of the capacitances of the bitlines, it really improves the performance of SRAMs with large capacities.

However, through the scaling down of CMOS technology, process variations during fabrication, including geometry variations, random dopant fluctuations and oxide thickness variations in deep sub-micron technology, have become unacceptable[5]. In addition, negative bias temperature instability effect and channel hot carrier effect induce larger mismatch during operation. These two roots make the probability of malfunction in sense amplifiers increase considerably. Although a lot of researches on the reliability of latch type voltage sense amplifier have been proposed[6−8], the reliability studies of current sensing circuits in deep submicron technology are much less comparatively. This paper addresses the design for reliability of a traditional crosscoupled type current sensing circuits. This paper analyzes holistic failure mechanism of current sense amplifiers under random V_t variation and design parameter options including transistor size, falling time of control signal CS and threshold voltage of critical transistors for reducing failure probability of current sensing circuit. The overall optimization result of current sensing circuit is also given.

2. Holistic failure analysis

Figure 1 shows the simplified read-cycle-only memory system within traditional current sense amplifier[1,3]. It is composed of three parts: crosscoupled positive feedback current sensing circuit, current manipulation circuit and global sensing circuit. Crosscoupled positive feedback current sensing circuit consists of transistors P3–P6 and N1–N2, current manipulation circuit is made up of current mirror sense amplifier and global sensing circuit is always built up by latch type sense amplifier.

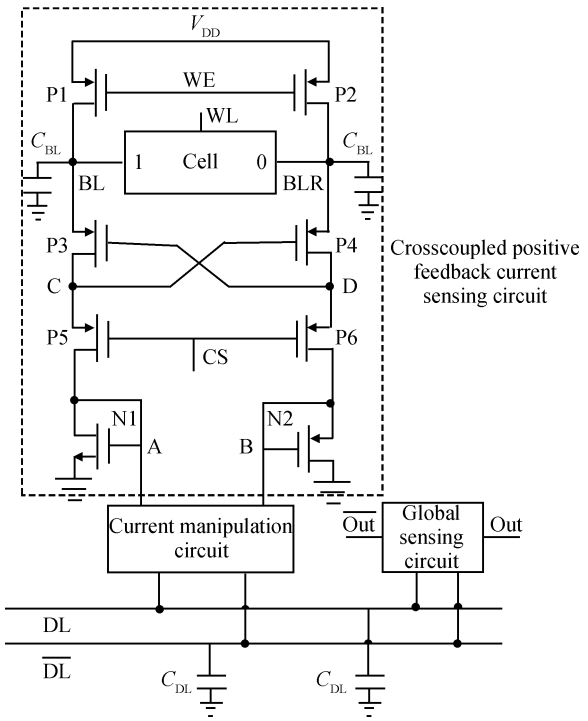

Fig. 1. Simplified read-cycle-only memory system within traditional current sense amplifier.

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Compared to voltage sense amplifier, current sensing circuit senses the small differential current on bitlines. Then the small differential current is amplified to large differential current by current manipulation circuit, which is converted to a differential voltage on the datalines. In the end, global sensing circuit magnifies the differential signal on the datalines to full CMOS logic level.

As current sensing is almost independent of the capacitances of bitlines and datalines, the responsive speed is very fast in the ideal condition. Nevertheless, process variations, especially threshold voltage variations, in deep sub-micron technology make the common-mode currents through P3 and P4 different. If differential signal due to process variation submerge differential signal due to cell current, the wrong signal is amplified by current manipulation circuit and latched by global sensing circuit.

We could educe that the crosscoupled positive feedback current sensing circuit is vital to the holistic yield of the simplified read-cycle-only memory system within traditional current sense amplifiers for two reasons: the first one is that correctness of signals amplifying the next stage; the robustness of current manipulation circuit made of current mirror sense amplifier with large dimension is another factor we should take into account.

Although current manipulation circuit and global sensing circuit are also important to the holistic reliability, we don't enable the global sensing circuit until the differential voltage on the datalines reaches to certain value to assure reliability.

Additionally, the current manipulation circuit and the global sensing circuit is optional and relatively immune to process variations for larger transistor size, so we just analyze the yield of crosscoupled positive feedback current sensing circuit in particular. To estimate failure probability of the current sensing circuit, we use HSPICE to perform Monte–Carlo simulations in 90 nm technology, where global process variations are determined by random distributions and passive mismatch is determined by random distributions with a unique set of values for each instance of the model. Simulations are repeated 1000 times and we define the failure probability of current sensing circuit as

$$P(\mathrm{F}) = \frac{\text{number of faulty cases}}{\text{total number of simulations}}. \tag{1}$$

Although current sensing circuit senses differential current on the bitlines, current manipulation circuit senses differential voltage on the nodes A and B (Fig. 1). Unlike voltage sense amplifier, the output signals of crosscoupled positive feedback current sensing circuit cannot reach to full CMOS logic level finally during sensing. So we define faulty cases in Eq. (1) as the cases of wrong sign of the potential difference of nodes A and B (Fig. 1) at 1 ns after the word line is started up, which insures the nodes A and B almost stable. Besides we add a capacitance of 10 fF on the nodes A and B each instead of the load capacitance of current manipulation circuit, and add a capacitance of 2 pF on the bitlines as C_{BL}. We also define the delay of the crosscoupled positive feedback current sensing circuit as the space of time between the start-up of wordline to the potential difference of nodes A and B reaching to 100 mV, because this potential differential can guarantee reliability for next stage sensing.

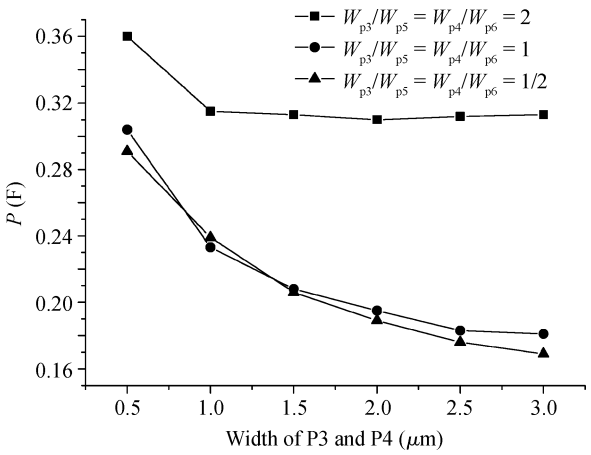

Fig. 2. Impact of the width of P3 and P4 on failure probability.

3. Design options for yield

In order to improve the robustness of crosscoupled positive feedback current sensing circuit, we consider three design options and investigate the impact of design options on the reliability and delay of current sensing circuit. They are: (a) transistor size, (b) falling time of control signal CS, (c) threshold voltage of critical transistors.

3.1. Transistor size

Due to random dopant fluctuation effect in deep submicron technology, threshold voltages of transistors have Gaussian distributed random variations (δV_{t}) with mean = 0 and a variance given by[9]

$$\begin{aligned}\sigma_{V_{\mathrm{t}}} &= \frac{qT_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}}\sqrt{\frac{N_{\mathrm{a}}W_{\mathrm{d}}}{3L_{\min}W_{\min}}}\sqrt{\frac{L_{\min}W_{\min}}{LW}} \\ &= \sigma_{\mathrm{V_{t0}}}\sqrt{\frac{L_{\min}W_{\min}}{LW}},\end{aligned} \tag{2}$$

where N_{a} is effective channel doping, W_{d} is the depletion region width, T_{ox} is the oxide thickness, and $L_{\min}$ and $W_{\min}$ are the minimum channel length and width, respectively. From Eq. (2) we could expect that the shift of threshold voltage due to random dopant fluctuations decreases with an increase in transistor size.

For the above reason the smaller V_{t} variations in the larger width of transistors P3–P6 reduce the failure probability as shown in Fig. 2. Additionally, larger width of transistors P3–P6 also develops more effective differential current[10], which prevent the wrong differential signal due to process variation in the highest flight. On the other hand, $W_{\mathrm{p3}}/W_{\mathrm{p5}}$ and $W_{\mathrm{p4}}/W_{\mathrm{p6}}$ also have effect on the reliability of current sensing circuit. Figure 2 also shows three situations: (a) $W_{\mathrm{p3}}/W_{\mathrm{p5}} = W_{\mathrm{p4}}/W_{\mathrm{p6}} = 2$, (b) $W_{\mathrm{p3}}/W_{\mathrm{p5}} = W_{\mathrm{p4}}/W_{\mathrm{p6}} = 1$, (c) $W_{\mathrm{p3}}/W_{\mathrm{p5}} = W_{\mathrm{p4}}/W_{\mathrm{p6}} = 1/2$. The current conveyor, composed of P3-P6, causes a virtual short circuit across the complementary bitlines and this virtual short circuit makes plausible the appearance of a very low input impedance Z_{i} [11].

$$Z_{\mathrm{i}} = \frac{2(g_{\mathrm{m5,6}} - g_{\mathrm{m3,4}})}{g_{\mathrm{m}}^2}. \tag{3}$$

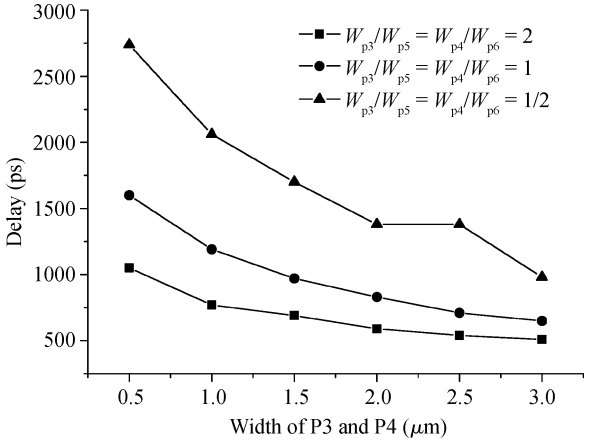

Fig. 3. Impact of the width of P3 and P4 on sensing delay.

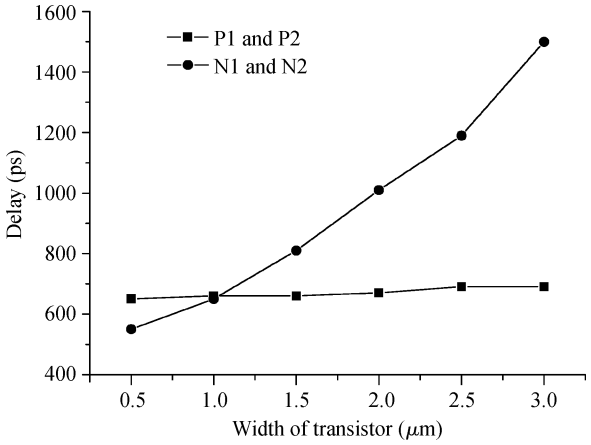

Fig. 5. Impact of the width of P1–P2 and N1–N2 on sensing delay.

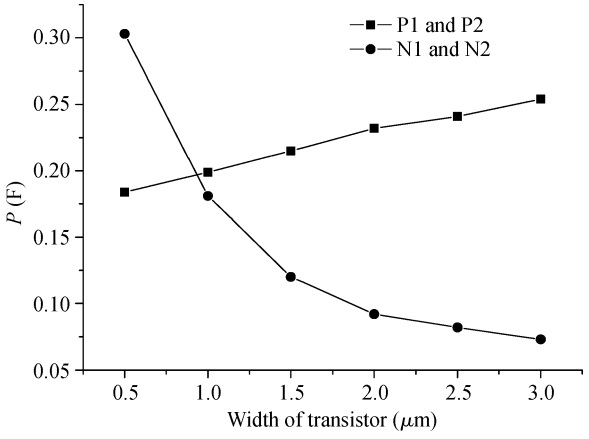

Fig. 4. Impact of the width of P1–P2 and N1–N2 on failure probability.

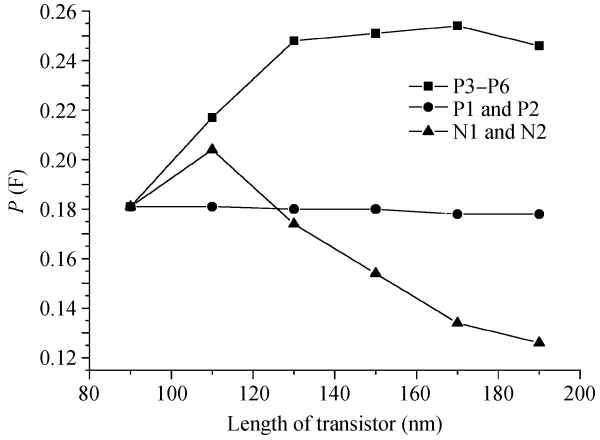

Fig. 6. Impact of the length of transistors on failure probability.

Here, g_m is the common transconductance of all devices at the fully balanced ideal state of the circuit and indices 3, 4, 5 and 6 designate the g_m in transistors P3, P4, P5 and P6. We can see from Eq. (3) that Z_i is negative if $g_{m3} = g_{m4} > g_{m5} = g_{m6}$ and a negative Z_i may cause instability, which explains why failure probability of situation (a) is much larger than the other two situations. Since larger Z_i increases the delay of the current sensing, the delay of situation (c) is longer than the other two situations as shown in Fig. 3. Additionally larger width of P3–P6 reduces the delay of current sensing for developing more effective differential current.

Figure 4 shows that the larger width of P1 and P2 increases the failure probability of current sensing circuit a little, because the decreasing differential voltage on the bitlines following the upsizing of P1 and P2 induces less effective differential current[10], which makes current sensing vulnerable to the differential current due to process variations of P3–P6 and N1–N2. That explains why smaller V_t variability in the larger size do not decrease the failure probability of current sensing. Less effective differential current also results in longer delay time of current sensing. However it is not obvious as shown in Fig. 5 as current conveyor made of P3 and P4 amplifies the small differential current quickly.

It is observed in the Fig. 4 that increasing width of N1 and N2 leads to considerable reduction in failure probability. For V_t variations of transistors N1 and N2 make the voltages of the node A and B different initially, which is converted into the differential voltage of node C and D wrongly during reading, the wrong differential signal is induced to prevent the differential current due to cell current from amplifying correctly. Unlike P1 and P2, the size of N1 and N2 have no effect on the effective differential current, so smaller V_t variations due to larger width of N1 and N2 reduce failure probability obviously. Unfortunately, the delay time increases following the increasing width of N1 and N2 as showed in Fig. 5, since the increasing width prevents the voltages of nodes A and B from being boosted up quickly. Hence we must choose an offset point of width of transistors N1 and N2 for balancing the yield and speed of the current sensing circuit.

The impact of length of transistors is shown in Figs. 6 and 7. Increasing length of N1 and N2 effectively reduces the failure probability of current sensing due to smaller V_t variations in larger size. Fortunately increasing length of transistors N1 and N2 also reduces the delay of current sensing as increasing length can boost up the voltages of nodes A and B quickly. Whereas failure probability and delay of current sensing circuit increase evidently following the increasing length of P3–P6, as larger length of P3–P6 reduce the effective differential current on the bitlines. It is observed that the failure probability and delay are less sensitive to length of P1 and P2.

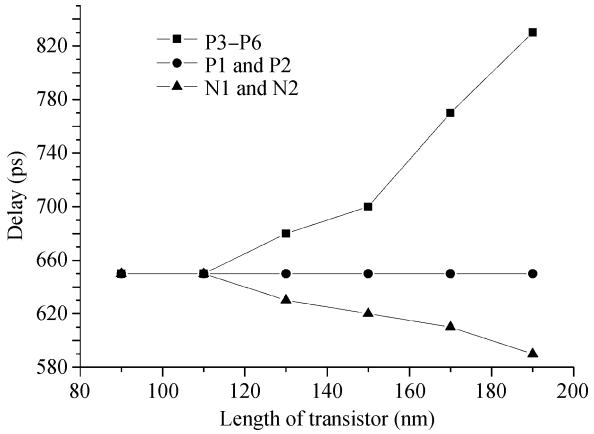

Fig. 7. Impact of length of transistors on sensing delay.

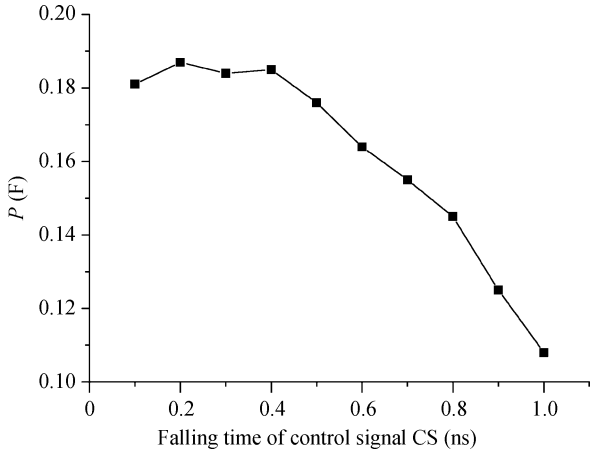

Fig. 8. Impact of falling time of control signal CS on failure probability.

In summary, we choose large width of P3–P6, moderate width of N1 and N2, and small width of P1 and P2 as the width sizing strategy, and select large length of N1 and N2, small length of P3–P6 as the length sizing strategy. The sizing strategy considers the balance of yield and speed of current sensing circuit, and the size of transistors can be arranged appropriately to optimize the whole performance.

3.2. Falling time of control signal CS

For prolonging rising time of sense amplifier enable signal as an offset compensation technique has been introduced in voltage sense amplifier[12], we consider the impact of falling time of control signal CS on failure probability and delay of current sensing circuit here.

As shown in Fig. 8, failure probability decreases as the falling time of control signal CS increases. When the falling time of control signal CS is extended, the start-up of transistors P5 and P6 will be postponed, which induces larger differential voltage on the BL and BLR. Larger differential voltage enhances the effective differential current due to the current flowing into the cell where a "0" is stored, which really improves the robustness of current sensing.

To be universally known, the postponed start-up of transistors P5 and P6 will increase the delay time before current sensing starts up. However the entire delay time of current sensing holds the line basically before falling time of control signal CS reaches to 0.7 ns as shown in Fig. 9. That is because the enlarged differential voltage accelerates the current sensing process, unless the falling time of CS is too long to be offset by the speedup. So we can choose 0.4–0.6 ns as falling time of control signal CS.

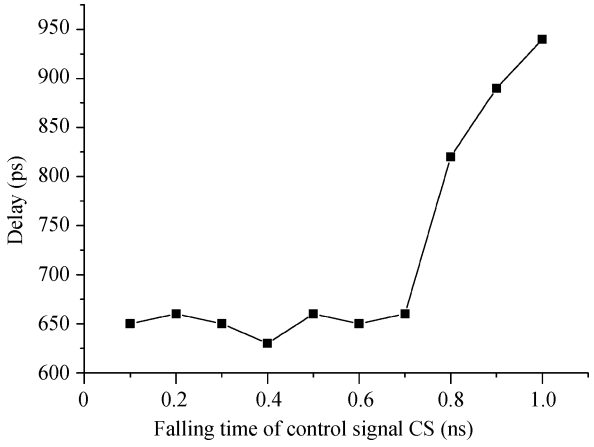

Fig. 9. Impact of falling time of control signal CS on sensing delay.

Table 1. Comparison of different situations.

Parameter	Normal situation	Situation (1)	Situation (2)
P1, P2	Typical	Body contact linked to power supply	Typical
P3, P4	Typical	Typical	Typical
P5, P6	Typical	Typical	Typical
N1, N2	Typical	Typical	Low V_t
P(F)	0.181	0.136	0.118
Delay time (ps)	650	620	640

3.3. Threshold voltage of critical transistor

We also develop an optimizing method by setting the threshold voltage of critical transistors. As shown in Table 1, situation (1) with connecting the body contact of P3 and P4 with power supply not only decreases the failure probability, but also decreases the delay time of current sensing. That can be explained as follows: since the voltage on the BLR become smaller than that on the BL when a cell is accessed, the threshold voltage of P6 becomes larger than that of P5 due to body effect, which forms the positive feedback to enlarge effective differential current. Additionally, the enlarged effective differential current also accelerates the current sensing.

In situation (2) we replace typical V_t transistors N1 and N2 with transistors with low threshold voltage, and the failure probability decreases obviously as shown in Table 1. As the low V_t transistors, which have smaller N_a than typical transistors, have smaller V_t variation as proved in Eq. (1), the differential current due to V_t variations is decreased and the failure probability of current sensing is reduced.

Table 2. Final optimization setting

Parameter	Width (μm)	Length (nm)	Threshold voltage
P1, P2	3	90	Typical
P3, P4	0.5	90	Typical
P5, P6	3	90	Typical
N1, N2	1	190	Low V_t
P(F)	0.049	0.049	0.049
Delay time (ps)	700	700	700

4. Final optimization

Eventually we do the final optimization by adopting the above technologies. According to the first strategy, we make the width of P1, P2, P5 and P6 large, and make the width of P3 and P4 small. Besides, we make the length of P1–P6 smallest and make the length of N1 and N2 large. For the second strategy, we can choose 0.4–0.6 ns as falling time of control signal CS. In the last strategy, we choose N1 and N2 as low V_t transistor. The failure probability of current sensing is about 0.25 in normal setting. After final optimization shown in Table 2, the failure probability can decrease to 0.049 and the delay time of current sensing only marginally increases to 700 ps.

5. Conclusion

A quantitative yield analysis of current sensing circuit in sub-100 nm technologies has been presented in this paper. We investigate the impact of three design options, including transistor size, falling time of control signal CS and threshold voltage setting of critical transistors, on the failure probability. It is found that proper sizing of transistors is necessary to minimize the failure probability of current sensing. A moderately long falling time of control signal CS can decrease failure probability on the basis of speed guarantee and specific threshold voltage setting of critical transistors is also helpful to improve the yield of the current sensing circuit.

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