Impact of parasitic resistance on the ESD robustness of high-voltage devices*

Lin Lijuan(林丽娟)†, Jiang Lingli(蒋苓利), Fan Hang(樊航), and Zhang Bo(张波)

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology, Chengdu 610054, China

Abstract: The impacts of substrate parasitic resistance and drain ballast resistance on electrostatic discharge (ESD) robustness of LDMOS are analyzed. By increasing the two parasitic resistances, the ESD robustness of LDMOS are significantly improved. The proposed structures have been successfully verified in a 0.35 μm BCD process without using additional process steps. Experimental results show that the second breakdown current of the optimal structure increases to 3.5 A, which is about 367% of the original device.

Key words: electrostatic discharge; high-voltage device; LDMOS; parasitic resistance

DOI: 10.1088/1674-4926/33/1/014005 **EEACC:** 2560

1. Introduction

With the thriving applications of automotive electronics, display drivers, power supplies and power management, the demands of high-voltage (HV) ICs are rapidly increasing[1, 2]. When fabricating devices to sustain a high operating voltage, not only the process complexity but also the difficulty to guarantee the reliability of HV devices is increased. Among the reliability issues of ICs, electrostatic discharge (ESD) is an important and inevitable event to the circuits and systems of microelectronics products during fabrication, packaging and assembling processes[3]. With the improvement of semiconductor manufacturing technologies, the ESD robustness of ICs has been lowered. In addition, there are some special issues making the design of HV devices more difficult, such as soft leakage, finger dependence and so on, all of which are challenging for designers.

Compared with low-voltage devices for ESD protection, HV devices have two differences. Firstly, the holding voltage $V_{\rm H}$ is much larger, so the power dissipation is much greater. Secondly, the holding voltage $V_{\rm H}$ of the high-voltage devices is always lower than the trigger voltage $V_{\rm t1}$, so the devices have serious problems in uniformly turning on. These two differences keep the HV devices from higher $I_{\rm t2}$ and lead to much difficulty in the design of HV protection devices. Therefore, not all the improvement methods in the low-voltage devices are applicable in the HV devices.

To improve the ESD robustness of HV n-channel metal–oxide–semiconductors (NMOSs), a number of different approaches have been proposed. Some ESD protection designs use the lateral or vertical bipolar transistors as ESD protection devices in smart power technology[4, 5]. However, fabrication cost and process complexity are increased by adding bipolar modules. Besides, a silicon controlled rectifier (SCR) has a high ESD robustness at the cost of small silicon area. Accordingly, latchup is a serious reliability issue of HV SCRs. Even if the ICs have passed the quasi-static latchup test[6], the external noises coupled into ICs can also induce so-called transient-induced latchup (TLU)[7]. In addition, to improve the turn-on speed of MOS transistors under ESD stress, gate-driven and substrate-triggered technologies have been used in the HV process[1]. However, in such cases, an additional ESD protection circuit is needed and more layout area is required for the additional ESD protection circuit. Furthermore, this circuit may be triggered by mistake.

In this paper, the influence of substrate parasitic resistance $R_{\rm B}$ and drain ballast resistance $R_{\rm D}$ on the ESD robustness of an HV n-channel lateral DMOS (nLDMOS) is investigated firstly in 0.35 μm 40 V BCD process. Several methods are proposed to improve the ESD robustness of the nLDMOS by increasing these two parasitic resistances. The proposed structures have little risk in IC design and do not need any additional process steps and mask layers. These proposed structures have been verified in a 0.35 μm BCD process.

2. LDMOS in ESD protection operation

The LDMOS used as an ESD protection element in this paper is shown in Fig. 1(a). The drain is made up of $\rm N^+$-LVNW-HVNW, while the channel is formed by LVPW under the gate and the source is composed of an $\rm N^+$ implant in the LVPW region. In addition, L_1 labeled in Fig. 1(a) is 5 μm, which describes the distance between the edge of the field oxide and the drain contact of the $\rm N^+$ implant. When used as an ESD protection device, the device is connected as a GGNMOS (gate-ground NMOS) structure, whose drain goes to an I/O pad and the gate, source and bulk are shortened together to ground.

To investigate device behavior during ESD stress, the transmission line pulsing (TLP) technique has been used to measure the trigger voltage ($V_{\rm t1}$) and the second breakdown current ($I_{\rm t2}$) of ESD devices. A TLP tester employs a rectangular pulse with energy ranges similar to those used in HBM (human body model) ESD qualification testing. The pulse width of the TLP is chosen to provide the same current-amplitude damage level (electrical) as is found in HBM ESD stress testing. This allows for correlation between TLP (with rectangular pulse widths of 75–200 ns) and HBM (with a 150-ns,

* Project supported by the National Natural Science Foundation of China (No. 60906038).
† Corresponding author. Email: linlij100@163.com
Received 17 May 2011, revised manuscript received 9 August 2011
© 2012 Chinese Institute of Electronics

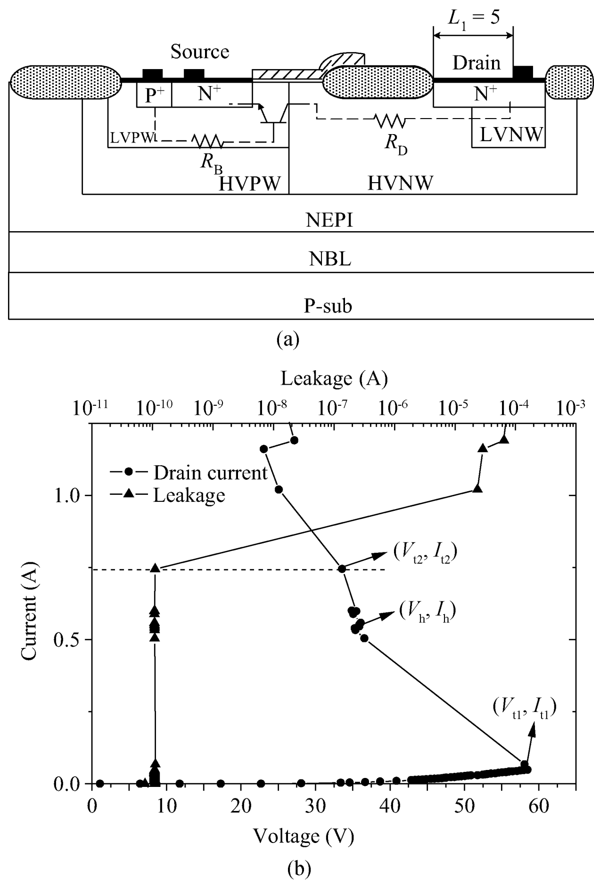


Fig. 1. (a) Cross section of the LDMOS in this paper. (b) The TLP-measured I–V characteristics of the original LDMOS structure.

double-exponential pulse width). The correlation is established through the TLP current and the assumed HBM peak current, i.e. V_{HBM} [V] $\approx I_{t2}$ [A] $\times$ 1500 Ω. The TLP-measured I–V characteristics of the original structure (Fig. 1(a)) with channel width $W = 75\ \mu m \times 2$ finger are depicted in Fig. 1(b).

When the LDMOS operates in ESD protection mode, it discharges ESD current through the parasitic NPN as shown in Fig. 1(a), which is constituted by N^+-LVNW-HVNW/ HVPW-LVPW/N^+. As a positive ESD transient appears at the drain (collector of the parasitic NPN), the collector junction is reverse-biased and goes to break down when the voltage is high enough. Avalanche multiplication takes place and electron–hole pairs are generated. Electron current flows into the drain, becoming a part of the collector current of the parasitic NPN. Hole current flows into the ground though the lateral parasitic resistance R_B, and thus builds up a potential, V_R. Since the source and bulk regions are shortened together, V_R actually appears across the emitter junction of the NPN positively, so it is also called V_{BE}. When V_{BE} increases to the turn-on voltage of the parasitic NPN, V_{on}, the emitter junction will turn on. Eventually the parasitic lateral NPN transistor will be triggered. This voltage in the drain is called trigger voltage V_{t1}, as shown in Fig. 1(b). Once the NPN turns on, an emitter current takes over the role of V_{CB} in maintaining the multiplication[8]. Collector voltage V_C starts to decrease and the device operates in snapback region, forming a low-impedance path to discharge ESD current. V_{t1} determines the speed which responds to the ESD pulse of the device, so it must be low enough. However, V_{t1} should be still higher than the circuit power supply voltage and retain some margin to ensure that the device would not be triggered under the normal working condition.

After snapback, collector voltage of the parasitic NPN is clamped to a low holding voltage level V_H which is presumably low enough to avoid dielectric rupture, as shown in Fig. 1(b). The current density continues to increase along with the collector voltage, which results in the movement of carriers in the electric field accelerating and sharply raises the lattice temperature by collision[9]. The current and voltage of the device are no longer stable, and finally thermal breakdown occurs, which is also called the second breakdown. The voltage and current of the second breakdown are labeled as V_{t2} and I_{t2}, as shown in Fig. 1(b). Generally, the ESD protection performance level, i.e., ESDV value, is typically represented by the second breakdown current I_{t2}. So, the sticking point to optimize the ESD robustness of devices is to enhance its I_{t2}.

According the principle above, V_{t1} and I_{t2} of this device as shown in Fig. 1(b) are about 58 V and 0.75 A, respectively.

3. Impact of R_B to ESD robustness of LDMOS

According to the working principle of the device, the voltage drop across the resistor (V_{BE}) increases with the parasitic resistance R_B, and the relationship between them follows the equation:

$$V_{BE} \cong R_B I_D. \tag{1}$$

Obviously, if increasing the R_B, a smaller I_D is needed to push the voltage V_{BE} increase to V_{on}, and a lower trigger voltage V_{t1} can be obtained.

The increase of R_B not only reduces the trigger voltage V_{t1}, but also has an impact on the second breakdown current of the device. After triggering the device, I_E can be expressed as follows according to E–M equation.

$$I_E = I_{ES}\left(\exp\frac{qV_{BE}}{kT} - 1\right) - \alpha_R I_{CS}\left(\exp\frac{qV_{BC}}{kT} - 1\right). \tag{2}$$

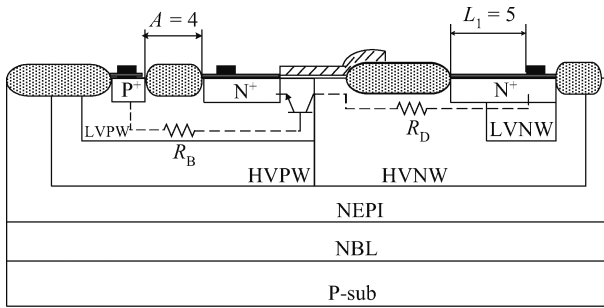
I_E increases as V_{BE} increases. That is, with the increase of R_B, the device will get higher current in the case of same drain voltage. In this situation, the current amplification factor β of the parasitic NPN increases accordingly.

$$\beta(M - 1) = k, \tag{3}$$

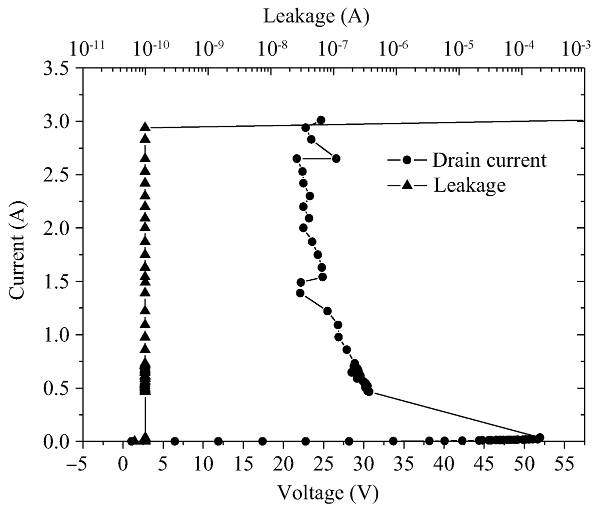
where $1 \leqslant k \leqslant 2$ is a correction factor[10, 11]. This equation shows that M decreases with the increase of β, which means that in the case of a larger R_B, it is no longer to require a higher M to generate electron-hole pairs in the same discharge current.

Combining the two reasons above, a larger R_B not only leads to larger current amplification of the parasitic NPN, but also to a smaller M value of avalanche breakdown. It means that lower voltage stress is needed to produce the same current, which reduces the amount of heat generated, and higher second breakdown current I_{t2} can be obtained.

Based on the discussions above, several structures are proposed to verify the theory.

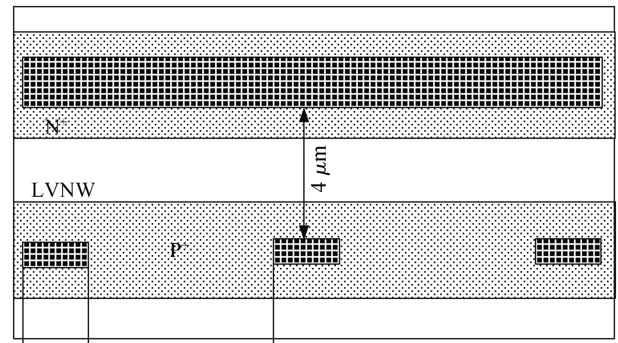


(a)

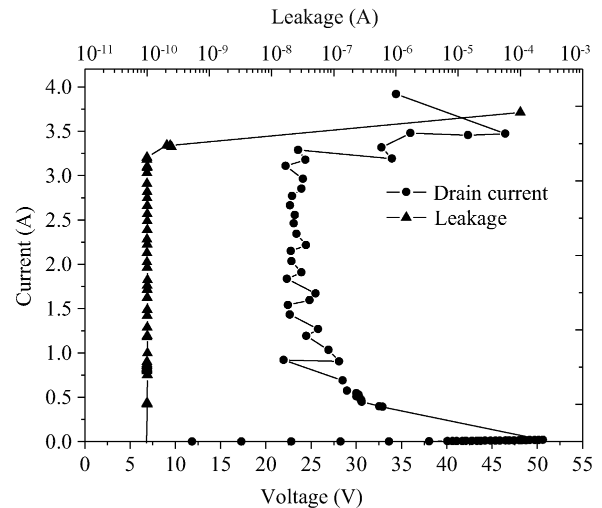


(b)

Fig. 2. (a) Cross section of LDMOS of structure A with optimized R_B. (b) The TLP-measured I–V characteristic of the structure A.



(a)



(b)

Fig. 3. (a) Layout of LVNW contacting for the structure B. (b) The TLP-measured I–V characteristic of the structure B.

3.1. Structure A with increased R_B

The cross section of structure A is given in Fig. 2(a). Compared with the original structure, it just extends the space between the source implant and the P^+ implant, $A = 4$ μm, and all other parameters remain unchanged. This approach increases the distance of the avalanche hole flow which thereby increases the R_B of the device.

The TLP-measured I–V characteristic of this structure is shown in Fig. 2(b). The channel width of this structure is the same as original one. It is given in Fig. 2(b) that V_{t1} is about 52 V instead of 58 V in Fig. 1(b), and I_{t2} is about 3 A which is 300% of the original one. In other words, the ESD robustness of this device is improved effectively.

3.2. Structure B with increased R_B

Structure B is based on structure A, and reduces the area of the P^+ implant active region to 1/3 of the original one. Figure 3 (a) illustrates the schematic layout of the source of this device.

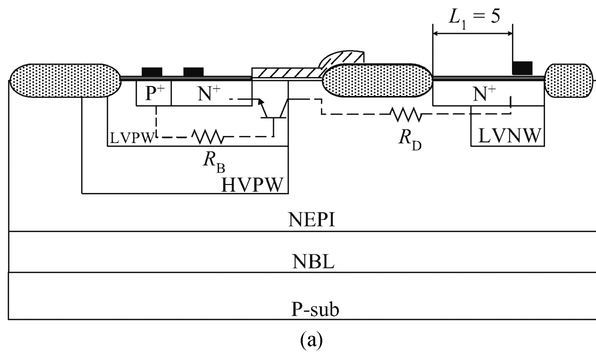
Similar to structure A, structure B extends the space between the source and P^+ implant to increase the distance of that the avalanche holes go through. In addition, area reduction in the P^+ implant active region is used to cut down the area of receiving holes. With these two approaches applied, R_B can be effectively increased.

Figure 3(b) shows the TLP-measured I–V characteristic of this structure. The channel width of this structure is the same as original one. It is given in Fig. 3(b) that V_{t1} is about 51.5 V which is 6.5 V lower than the original structure and I_{t2} is about 3.3 A which increases the ESD discharge current more than 300% of the original one.

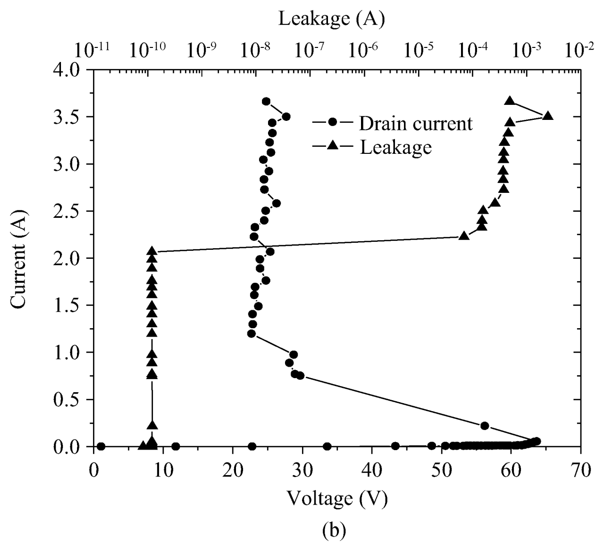
The test results for the two structures above show that increasing the resistance R_B can effectively reduce the trigger voltage of the device, and greatly increase the device ESD discharge current I_{t2}. However, increasing R_B has its side effects, such as increasing the layout area of the device.

4. Impact of R_D to ESD robustness of LDMOS

Increasing the drain ballast resistor is another effective way to improve the device's second breakdown current I_{t2}. The current can be avoided to focus on a certain filament by increasing the drain ballast resistor, which makes the ESD discharge current more uniform. Generally, increasing the ballast resistor can be achieved by increasing the gate to drain contact space (GDCS) or by increasing the average resistivity of the path current flowing through. The former greatly increases the area of the layout; therefore a trade-off must be made between layout area and the device's ESD robustness. However, the second method does not have this problem, so it saves layout area and

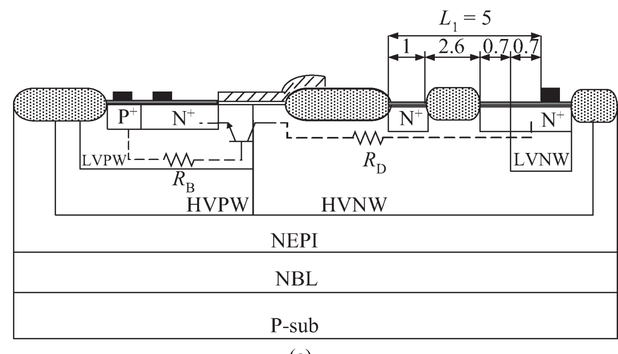


(a)

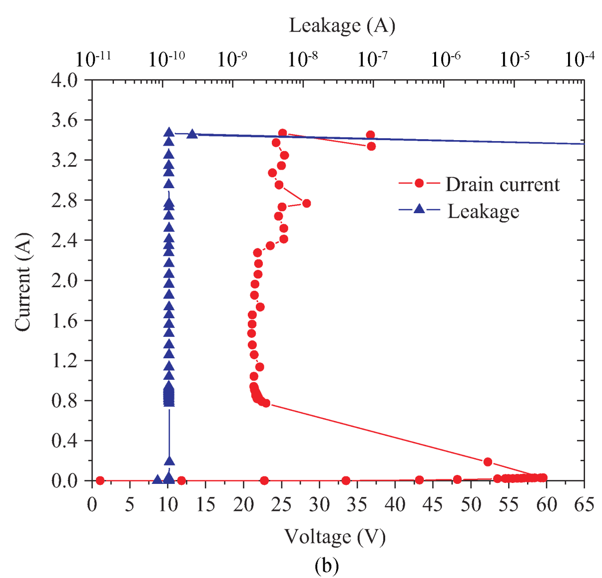


(b)

Fig. 4. (a) Cross section of LDMOS of the structure C with optimized RD. (b) The TLP-measured I–V characteristic of the structure C.



(a)



(b)

Fig. 5. (a) Cross section of LDMOS for the structure on D. (b) The TLP-measured I–V characteristic of the structure D.

reduces the cost. The test structure in this paper is achieved by the second method.

4.1. Structure C with increased R_D

The cross section of the structure C is shown in Fig. 4(a). The test structure keeps its width at 75 μm $\times$ 2 finger. Figure 4(b) illustrates the TLP-measured I–V characteristic of the device. Compared with the original structure, this device removes the HVNW, as shown in Fig. 4(a), which makes the avalanche electrons must go through the high resistivity N-epi layer to reach the drain, and thus increases the R_D.

As shown in Fig. 4(b), this structure is sufficient to improve the discharge current of the device, for the I_{t2} of the structure is about 2 A. Compared with the original structure 0.75 A, it has been greatly improved, but the trigger voltage V_{t1} of the structure is up to 64 V, so it is not suitable as a 40 V ESD protection device.

4.2. Structure D with increased R_D

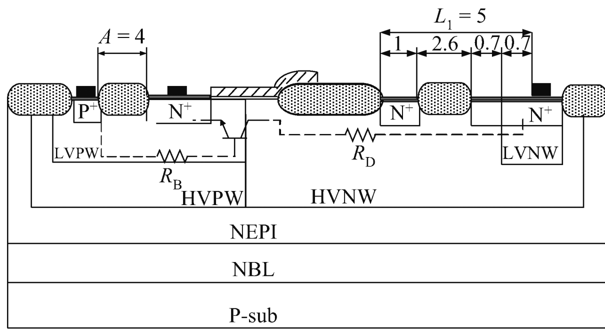
Figure 5(a) shows the cross section of structure D. This structure uses a field oxide to isolate the N$^+$ implant in the drain to achieve the purpose of increasing R_D without increasing the layout area of the device, where the length of field oxide is 2.6 μm, the distance between LVNW and N$^+$ active is 0.7 μm, and the distance between the edge of LVNW and the N$^+$ contact is 0.7 μm. The structure not only increases the current flowing path, but also reduces the drain area to receive electrons, which increases the ballast resistor R_D and thus increases the device's ESD robustness.

Figure 5(b) illustrates the TLP-measured I–V characteristic of this structure. The channel width of this structure is the same as original one. It is shown in Fig. 5(b) that I_{t2} is about 3.35 A, which increases the ESD discharge current more than 300% without increasing the trigger voltage V_{t1}.

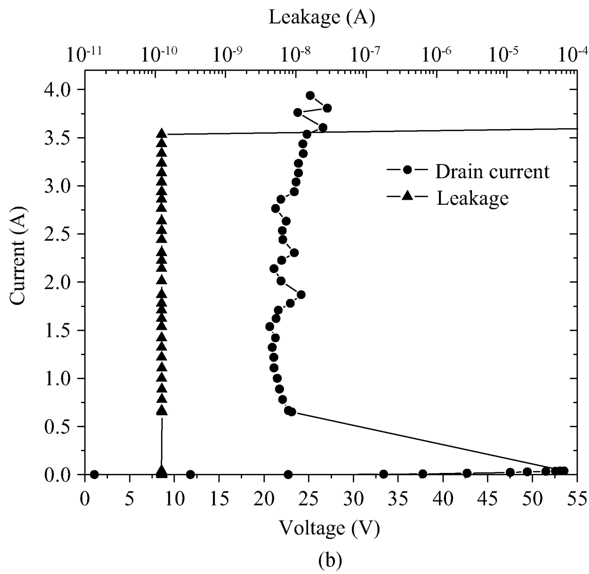
The result indicates that increasing the resistance R_D can effectively increase the I_{t2} of the device without taking an additional layout area, and it thereby enhances the device's ESD protection ability. However, excessive increase the R_D may result in some side effects: The bigger the R_D is, the more heat will be generated when the device discharges the ESD current. Consequently, I_{t2} may be decreased. Thus, the trade-off must be made in the design.

5. Structure E with optimized R_B and R_D

From the analysis of the two parts above, both R_B and R_D can improve the device's ESD robustness: increasing the resistance R_B can effectively reduce the trigger voltage of the device and greatly increase the device ESD discharge current I_{t2}, while increasing the resistance R_D can effectively increase I_{t2}



(a)



(b)

Fig. 6. (a) Cross section of LDMOS for the structure on E. (b) The TLP-measured $I-V$ characteristic of the structure E.

without wasting layout area. According these two conclusions, it can be deduced that: if the optimization of R_B and R_D can be combined, the improvement of the device's ESD robustness may be much greater.

Based on this deduction, a cross-section of the proposed device is shown in Fig. 6(a), which combines structure A with an optimized R_B ($A = 4$ μm) and structure D with its optimized R_D.

Figure 6(b) illustrates the TLP-measured $I-V$ characteristics of this structure. The structure E keeps its width as 75 μm $\times$ 2 finger. As shown in Fig. 6(b), structure E has the highest I_{t2} of 3.5 A and V_{t1}, which is about 53.5 V. The result indicates that structure E combines the advantages of the two methods mentioned above and is much better than other structures.

6. Conclusion

This paper describes the operation principle of high-voltage LDMOS under ESD stress, and analyzes the impact of parasitic resistance R_B and R_D on the ESD robustness of the device: firstly, increasing the resistance R_B can effectively reduce the trigger voltage of the device, and greatly increase the device second breakdown current I_{t2}; secondly, increasing the resistance R_D can effectively increase I_{t2} without enlarging the layout area. A variety of optimization structures have been proposed in this paper, which have been verified in a 0.35 μm BCD process. TLP test results show that increasing the R_B and R_D can effectively enhance the device's ESD robustness, while the best optimization structure combines the two methods to increase the I_{t2} from 0.75 to 3.5 A.

References

[1] Wang C T, Ker M D, Tang T H, et al. ESD protection design with lateral DMOS transistor in 40-V BCD technology. IEEE Trans Electron Devices, 2010, 57(12): 3395

[2] Knaipp M, Park J M, Vescoli V. Evolution of a CMOS based lateral high voltage technology concept. Microelectron J, 2006, 37(3): 243

[3] Chen W Y, Ker M D. Circuit and layout co-design for ESD protection in bipolar-CMOS-DMOS (BCD) high-voltage process. IEEE Trans Circuits Syst, 2010, 57(5): 1039

[4] De Heyn V, Groeseneken G, Keppens B, et al. Design and analysis of new protection structures forsmart power technology with controlled trigger and holding voltage. Proc IEEE Int Reliab Phys Symp, 2001: 253

[5] Bertrand G, Delage C, Bafleur M, et al. Analysis and compact modeling of a vertical grounded-base n–p–n bipolar transistor used as ESD protection in a smart power technology. IEEE J Solid-State Circuits, 2001, 36(9): 1373

[6] EIA/JEDEC Standard No. 78. IC latch-up test. Electronic Industries Association, 1997

[7] Ker M D, Lin K H. The impact of low-holding-voltage issue in high-voltage CMOS technology and the design of latchup-free powerrail ESD clamp circuit for LCD driver ICs. IEEE J Solid-State Circuits, 2005, 40(8): 1751

[8] Wang A Z H. On-chip ESD protection for integrated circuits. Massachusetts of USA: Kluwer Academic Publishers, 2003

[9] Amerasekera A, Duvvury C. ESD in silicon integrated circuits. New York: John Wiley & Sons, 2002

[10] Pinto-Guedes M, Chan P C. A circuit simulation model for bipolar-induced breakdown in MOSFET. IEEE Trans Comp Aid Des, 1988, 7(2): 289

[11] Ker M D, Lin K H. Double snapback characteristics in high-voltage nMOSFETs and the impact to on-chip ESD protection design. IEEE Electron Device Lett, 2004, 25(9): 640