

Graph theory for FPGA minimum configurations

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Abstract: A traditional bottom-up modeling method for minimum configuration numbers is adopted for the study of FPGA minimum configurations. This method is limited if a large number of LUTs and multiplexers are presented. Since graph theory has been extensively applied to circuit analysis and test, this paper focuses on the modeling FPGA configurations. In our study, an internal logic block and interconnections of an FPGA are considered as a vertex and an edge connecting two vertices in the graph, respectively. A top-down modeling method is proposed in the paper to achieve minimum configuration numbers for CLB and IOB. Based on the proposed modeling approach and exhaustive analysis, the minimum configuration numbers for CLB and IOB are five and three, respectively.

Key words: graph theory; minimum configuration number; FPGA; CLB; IOB

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1. Introduction

With the rapid development of programmable devices, field programmable gate arrays (FPGAs) are increasingly playing a critical role in digital circuit design. However, FPGA testing poses a challenge as integrated circuit manufacturing technologies advance and device scales increase. Therefore, investigations of FPGA testing has been a popular topic^[1–3]. The difficulty of FPGA testing is how to cover as many FPGA internal resources as possible with minimum testing configurations. Except for the bottom-up approaches studied in Refs. [4, 5], few investigations are involved in the arena. In these two papers, the authors studied the bottom-up method for minimum configuration numbers and applied the method to Xilinx Spartan, 3000 and 4000 series FPGA. Assume that there are n configuration bits in a logic block, 2^n testing configurations or the maximum configuration numbers are achieved. In order to get the minimum configuration numbers from the maximum configuration numbers, two procedures are required, or the boundary conditions of the testing configurations have to be found. The configurations of a single look-up table (LUT) and multiplexer in one logic block are analyzed at first. Then, the configurations of a network consisting of an array of LUTs and multiplexers are studied. Finally, the minimum configuration numbers and the corresponding test configurations in terms of the aforementioned boundary conditions can be obtained. These two papers concluded that the minimum configuration numbers for configurable logic blocks (CLBs) of Spartan, 4000 family and 3000 family FPGAs were 4, 5 and 4, respectively. However, the approach is limited if the CLB contains a large number of LUTs and multiplexers. Consequently, the boundary conditions of the testing configurations are not easily acquired.

As a branch of mathematics, the object of graph theory is graphs. A graph consists of some vertices and edges connecting pairs of vertices. In general, the graph is used to represent specific relationships between issues. The vertexes represent

the issues and the edges represent the relationships. Graph theory plays an important role in circuit analysis, and provides a simple and systematic modeling method which is effective for many issues. Many circuit problems may be transformed into graph issues by using some algorithms^[6, 7].

In this paper, input-output blocks (IOBs) and CLBs in XC4000 FPGAs are modeled by graph theory. In other words, an internal logic block and interconnections of a FPGA are considered as a vertex and an edge connecting two vertices in the graph, respectively. A tree is derived in terms of the IOB or CLB architecture. Then the theoretic minimum configuration numbers are available if we know the maximum indegree for each vertex. Afterwards we can compute the minimum configuration numbers along with the corresponding testing configurations based on the hierarchical relationship of the tree. Also this algorithm can be extended for other types of FPGAs. In fact, the technique we propose is a top-down one. As a result, the difficulty associated with searching the boundary conditions of testing configurations can be relieved even if the CLB contains a large number of LUTs and multiplexers.

Now graph theory has been applied to FPGA interconnect routing (IR) testing^[8, 9]. However, neither of the two papers demonstrates how to achieve the minimum configuration numbers for IRs.

2. Basics

2.1. Related knowledge on graph theory

A graph is a pair $G = (V, E)$ of sets. V is the set of vertices and E is the set of edges. The vertex set of a graph G is referred to as $V(G)$, and its edge set as $E(G)$.

A digraph (or directed graph) $D = (V_D, E_D)$ consists of vertices V_D and edges E_D . V_D is the set of vertices and E_D is the set of directed edges. We still write uv for (u, v) , but note that $uv \neq vu$. We shall always assume that $V \cap E = \emptyset$ ^[6, 7].

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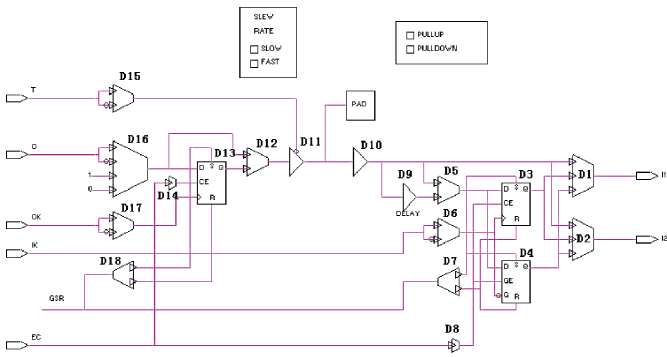


Fig. 1. Fundamental architecture of an IOB in XC4000 FPGAs.

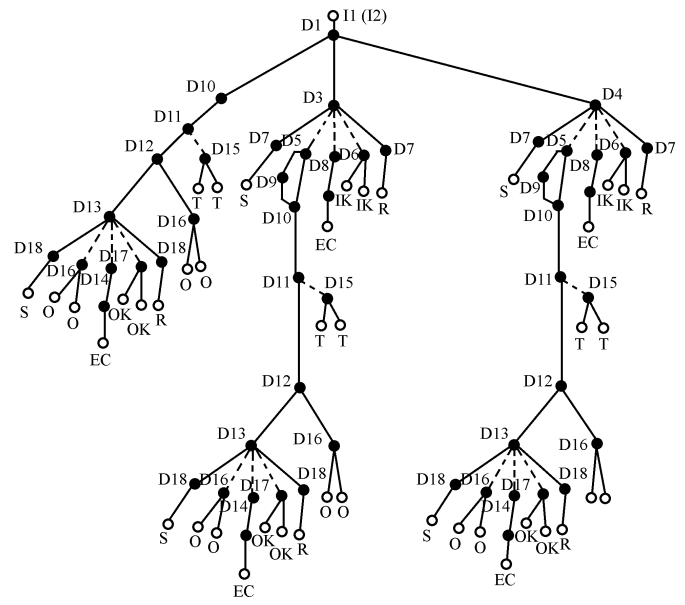


Fig. 3. IOB modeling by graph theory.

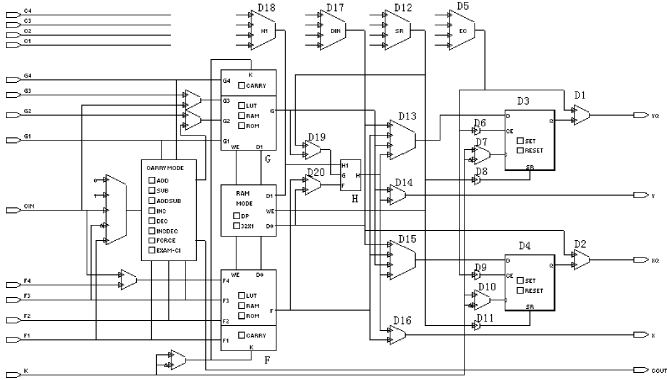


Fig. 2. Fundamental architecture of a CLB in XC4000 FPGAs.

Assuming that v is a vertex in digraph D , the outdegree (indegree) of v is the number of the edges which take v as the beginning (end) vertex, denoting for $d^+(v)$ and $d^-(v)$. The sum of the outdegree and indegree of v is called the degree of v , labeling as $d(v)$.

A graph is called acyclic, if it has no cycles. An acyclic graph is also called a forest. A tree is a connected acyclic graph. A directed graph D is a directed tree if the underlying graph of D is a tree. A rooted tree T is defined as follows: the indegree of only one vertex is 0, while the indegree of the other vertices is 1. In a rooted tree, a vertex u is the ancestor of v , if $u \neq v$ and $u \rightarrow v$, also v is the offspring of u . A vertex u is the father of v and v is the son of u if $\langle u, v \rangle$ is a directed edge. If n vertices are the sons of a father, we call them brothers.

2.2. Related knowledge on FPGA

As shown in Fig. 1, each IOB in XC4000 FPGA consists of two D flip-flops (D-FFs), one D latch, one tri-gate and some multiplexers, etc.

As shown in Fig. 2, each CLB is composed of two 4-input LUTs, one 3-input LUTs, two D flip-flops, carry logic and some multiplexers, etc.

3. Modeling with graph theory

In Fig. 1, 18 components are labeled with symbols D1, D2, D3...D18, and considered as 18 vertices in a graph. Two vertices are linked with a line if the two corresponding compo-

nents are connected in Fig. 1. In addition, different constraint conditions are required to apply for multiplexers, D-FFs and D latches. Only D1 is studied here because D1 and D2 are equivalent in the IOB circuit. Graph for IOB in Fig. 1 is illustrated in Fig. 3.

In Fig. 3, the solid circle vertices represent the devices in the IOB, while the edges denote that the adjacent devices are connected. Each edge is directed. The direction of the edges indicates that signals propagate from the bottom to the top. The hollow circle vertices represent the input and the output terminals in the IOB, among which I1 is the output terminal, S, O, EC, OK, R and T are the input terminals. The dashed edges mean that the wires can be configured simultaneously in one configuration. However, only one solid edge and more than one dashed edge are allowed for one solid circle vertex in one configuration.

A similar manipulation is carried out for CLB in Fig. 2 with labeling the 20 components as D1, D2, D3...D20. There are 13 input and 4 output terminals for a CLB. The CLB modeling by graph theory is illustrated in Fig. 4.

As shown in Fig. 4, solid diamonds F, G, H represent LUTs while solid circle D3 and D4 indicate D-FFs. The hollow circle vertices represent the input and output terminals in the CLB, among which symbols YQ, Y, XQ, X are the output terminals and C1, C2, C3, C4 are the input terminals. Except D-FFs denoted by D3 and D4, multiplexers are represented by solid circle vertices in Fig. 4. Three dashed edges and two solid edges are adjoined to D3 or D4, representing clock signal CLK, enable signal EN, data-input signal D, set signal S and reset signal R, respectively. The signals D and EN can be configured simultaneously while the signals S and R only can be configured alternatively. This constraint is based on the CLB characteristics. Similarly, only solid edges are met with the multiplexers. Of course, the dashed edges which connect the LUTs can be configured simultaneously.

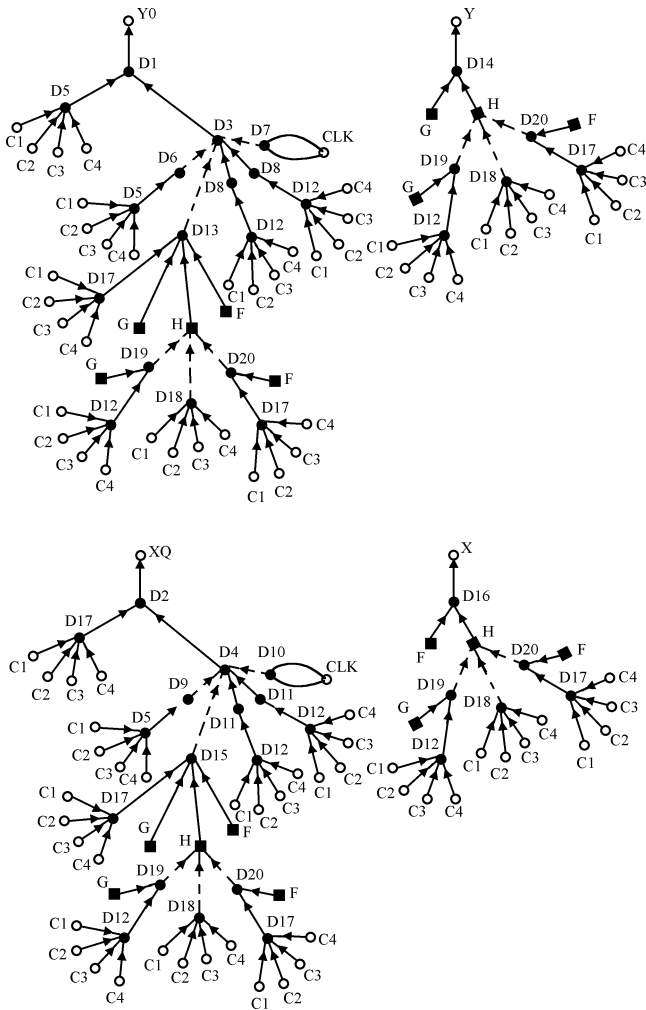


Fig. 4. CLB modeling by graph theory.

4. Minimum configuration numbers and the corresponding test configurations

4.1. Analysis on CLB

In Fig. 4, we can obtain that the depth, breadth and indegree of each tree is 7, 4 and 4, respectively. An algorithm, called the depth-first search is employed to study the minimum testing configuration. One search process translates to one configuration in our study. The algorithm defines that each vertex in a graph is searched only once. However, some vertices in a CLB or IOB graph maybe covered more than once due to the characteristics of FPGA. Therefore, we must ensure that each vertex in the CLB graph is covered at least once.

From Fig. 4, we can obtain that the relation between the theoretic minimum configuration number N_C and the maximum indegree of each vertex d_{max} is:

$$N_C \geq d_{max} = 4.$$

The expression translates to that least four test configurations are required to get access to all resources in the CLB. Furthermore, application of the depth-first search algorithm can lead to following procedures:

(1) A vertex in a tree is not necessary to be searched if the vertex has been searched in another tree.

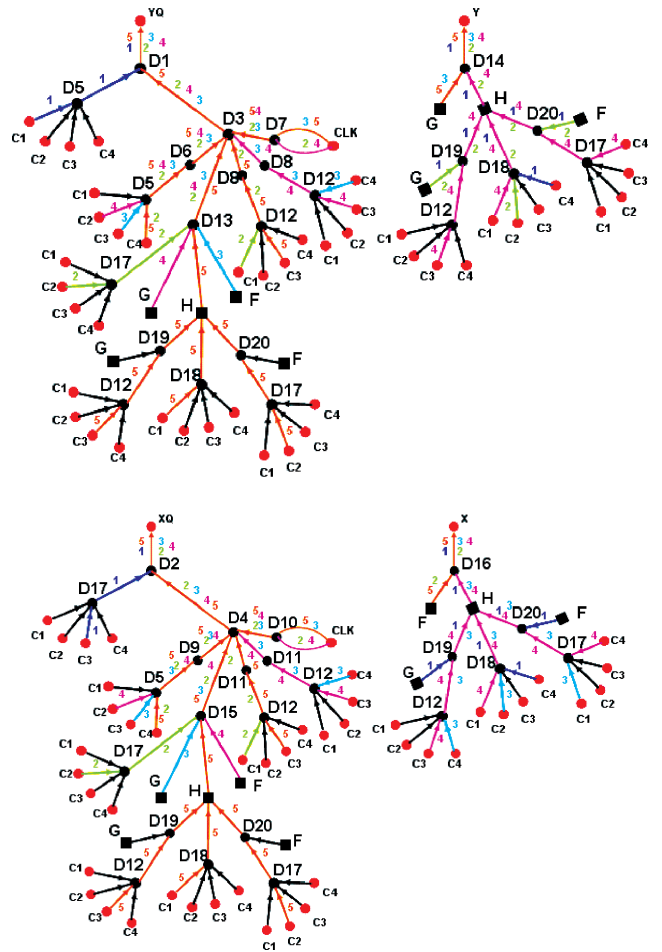


Fig. 5. Configuration graph of the CLB.

(2) The searching process should be continued if the vertex has off-springs.

(3) In the searching process, the black edges under the same vertex only can be chosen once at the same time, but the red edges under the same vertex can be chosen simultaneously.

(4) For multiplexers D5, D12, D17, D18 in the four trees, the identical offspring in their corresponding trees are required to be chosen in each search process.

The minimum configuration number of CLB is 5 in terms of the algorithm. The detailed searching procedures are listed as follows:

(1) The first search:

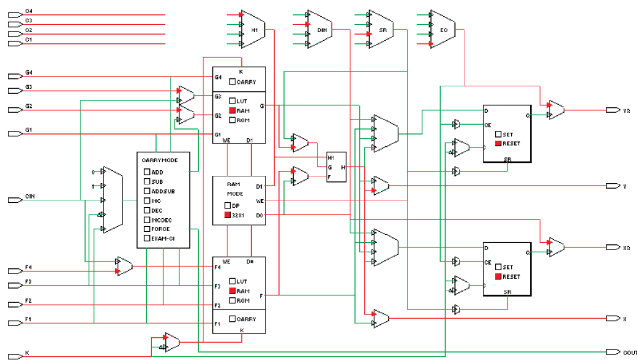
- Tree YQ: D1, D5, C1;
- Tree Y: D14, H, D19, G, D18, C4, D20, F;
- Tree XQ: D2, D17, C3;
- Tree X: D16, H, D19, G, D18, C4, D20, F.

(2) The second search:

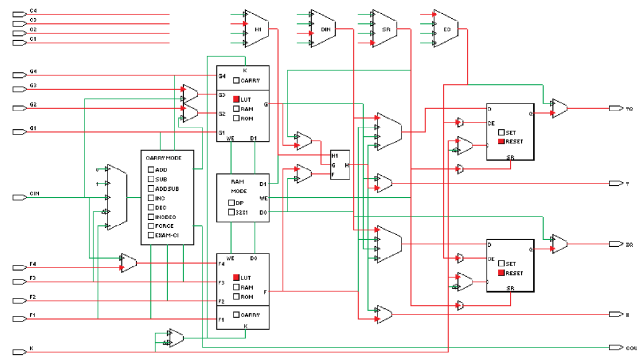
- Tree YQ: D1, D3, D6, D5, C4, D13, D17, C2, D8, D12, C1, D7;
- Tree Y: D14, H, D19, G, D18, C2, D20, F;
- Tree XQ: D2, D4, D9, D5, C4, D15, D17, C2, D11, D12, C1, D10;
- Tree X: D16, F.

(3) The third search:

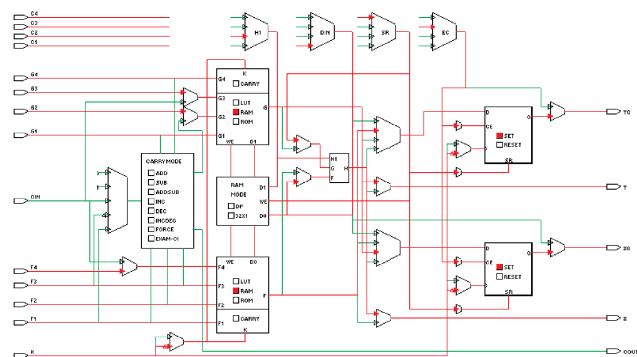
- Tree YQ: D1, D3, D6, D5, C3, D13, D17, C2, D8, D12, C4;



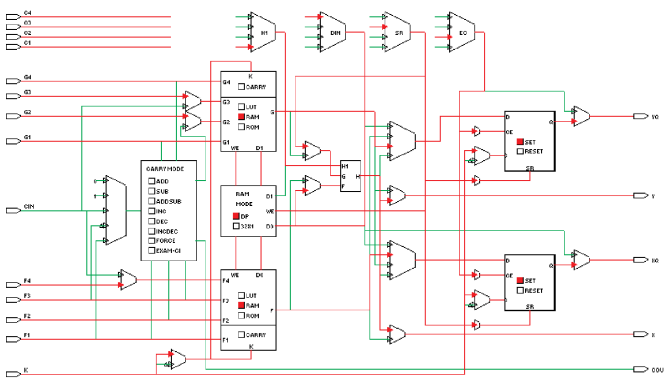
Circuit diagram of the first configuration



Circuit diagram of the second configuration



Circuit diagram of the third configuration



Circuit diagram of the fourth configuration

Fig. 6. Circuit diagrams corresponding to the 5 test configurations.

Tree Y: D14, G;
 Tree XQ: D2, D4, D9, D5, C3, D15, G, D11, D12, D10;
 Tree X: D16, H, D19, D12, C4, D18, C2, D20, D17, C1.
 (4) The fourth search:

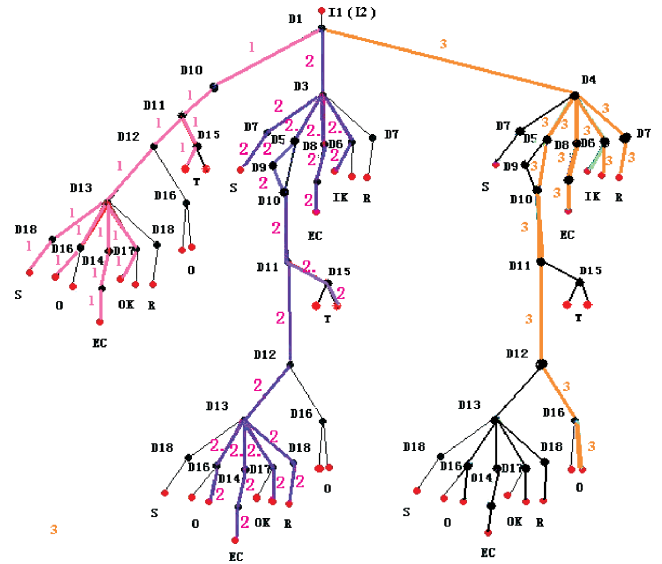


Fig. 7. Configuration graph of the IOB.

Tree YQ: D1, D3, D6, D5, C2, D13, G, D8, D12, C3, D7;
 Tree Y: D14, H, D19, D12, C3, D18, C1, D20, D17, C4;
 Tree XQ: D2, D4, D9, D5, C2, D15, F, D11, D12, C3, D10;
 Tree X: D16, H, D19, D12, C3, D18, C1, D20, D17, C4.

(5) The fifth search:

Tree YQ: D1, D3, D6, D5, C4, D13, H, D19, D12, C2, D18, C3, D20, D17, C3, D8, D12, C2, D7;
 Tree Y: D14, G;
 Tree XQ: D2, D4, D9, D5, C4, D15, H, D19, D12, C2, D18, C3, D20, D17, C3, D20, D11, D12, C2, D10;
 Tree X: D16, F.

All resources of the CLB are examined exhaustively in five configurations, as shown in Figs. 5 and 6. Figure 5 is the configuration graph and Figure 6 is the circuit diagram corresponding to the 5 configurations. In Fig. 5, the digital 1 with edges1, digital 2 with edges2, digital 3 with edges3, digital 4 with edges4, and digital 5 with edges5 represent each configuration.

After the five search processes for the graph, we can see from Figs. 5 and 6 that each vertex and edge have been searched at least once, which means that the CLB is tested fully. In other words, apart from the carry logic in the CLB, the minimum testing configuration numbers of CLB is five.

4.2. Analysis on IOB

The identical depth-first search algorithm and search procedures are applied for IOB investigation. Since trees I1 and I2 have symmetrical structures, so the configuration of I1 is studied.

(1) The first search:

I1: D1, D10, D11, D12, D13, D18, S, D16, O, D14, EC, D17, OK, D15, T;
 I2: D1, D10, D11, D12, D13, D18, S, D16, O, D14, EC, D17, OK, D15, T.

(2) The second search:

I1: D1, D3, D7, S, D5, D9, D10, D11, D12, D13, D16, O, D14, EC, D17, OK, D18, R, D15, T, D8, EC, D6, IK;
 I2: D1, D3, D7, S, D5, D9, D10, D11, D12, D13, D16, O, D14, EC, D17, OK, D18, R, D15, T, D8, EC, D6, IK;

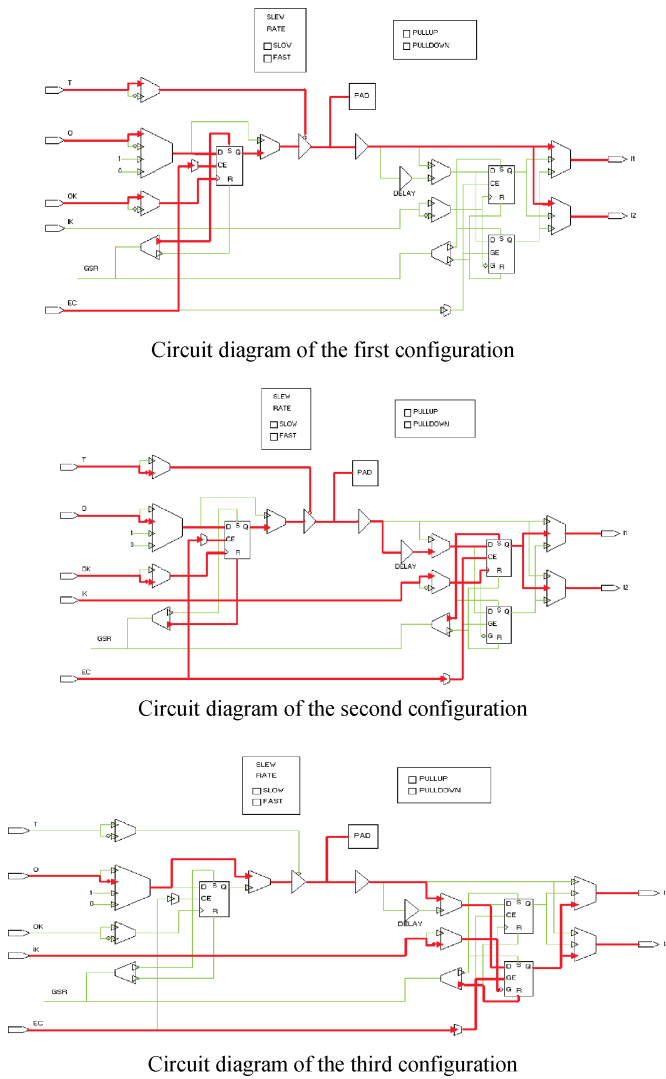


Fig. 8. Circuit diagram corresponding to the 3 test configurations.

- (3) The third search:
 I1: D1, D4, D5, D10, D11, D12, D16, O, D8, EC, D6, IK, D7, R;
 I2: D1, D4, D5, D10, D11, D12, D16, O, D8, EC, D6, IK, D7, R;
 All resources of the IOB are examined exhaustively in

three configurations as shown in Figs. 7 and 8. Figure 7 is configuration graph and Figure 8 is the circuit diagram corresponding to the 3 configurations. In Fig. 5, the digital 1 with edges1, digital 2 with edges2, digital 3 with edges3 represent each configuration.

After the three search processes for the graph, we can see from Figs. 7 and 8 that each vertex and edge have been searched once at least, which means that the IOB is tested fully. In other words, the minimum testing configuration numbers of IOB is five.

5. Conclusion

A modeling technique in Graph Theory utilized for CLB and IOB configurations of FPGA is presented in this paper. As shown in the paper, the minimum testing configuration numbers for CLB and IOB are 5 and 3, respectively.

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